ICM105C
Color VGA CMOS Image Sensor

Outline Specifications

V1.2

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Features

- 307,200 (640x480) pixels, VGA format, used with 1/4" optical system
- Progressive readout
- Output data format: 8-bit raw data
- Control interface: SIF
- Electronic exposure control
- On-chip 9-bit ADC
- Correlated double sampling
- Separate RGB gain
- Dead column removal
- Power down mode
- Automatic optical black compensation
- Support both master and slave mode
- Horizontal and vertical images
- Dual power supply 3.0V & 3.3V

General Description

ICM-105C is a single-chip digital color imaging device. It incorporates a 640x480 sensor array (650x490 in physical layout) operating at 1 ~ 30 frames per second in progressive manner. Each pixel is covered by a color filter, which formed a so-called Bayer pattern. Correlated double sampling is performed by the internal ADC and timing circuitry. The raw data can be adjusted by the digital gain. The output format is 8-bit raw data which can be fed to other DSP, color processing, or compression chips.

Application

- Digital camcorder
- Digital still camera
- Video phone
- Video conferencing
- Video mail
- Video cellular phone
- PC camera
- Security system
- Visual toy
- Industrial image capture/analysis
- Environment monitor system

Key Parameters

- Number of Active Pixels: 640x480
- Number of Physical Pixels: 650x490
- Frame Rate: 30/20/15/12/10/6/5/4/3/2/1 fps
- Pixel Size: 6.0 μm x 6.0 μm
- Sensor Area: 3.84 mm x 2.88 mm
- Main Clock Frequency: 24 MHz
- Exposure Time: 64 μs (@ 30 fps, 1 line, 24 MHz) ~ 126 s (@ 1 fps, 65535 lines, 24 MHz)

 9/30/2003

- Digital Gain: 1 ~ 64 x
- Sensitive to infrared illumination source
- Power Supply: 3.0V & 3.3V
- Power Requirement: 45 mA (@ 30fps, 24 MHz)
- Package: PLCC48

1. Pin Assignment

Pin #	Name	Class*	Function
14	CLKSEL	D, I, N	Clock source selection. 0: internal oscillator, 1: CLKIN
11	CLKIN	D, I, N	External clock source
12	XIN	A, I	Oscillator in
13	XOUT	A, O	Oscillator out
34	PCLK	D, O	Pixel clock output
36	OEN	D, I, N	Output enable. 0: enable, 1: disable
32	SIFCID	D, I, N	Lsb of SIF slave address
33	SIFCMS	D, I, U	SIF master/slave selection. 0: slave, 1: master (auto load from EEPROM after reset)
2	SCL	D, I/O	SIF clock
1	SDA	D, I/O	SIF data
10	POWERDN	D, I, U	Power down control, 0: power down, 1: active
16	RSET	A, I	Resistor to ground = 47 KΩ @ 24 MHz main clock, 51 KΩ @ 24 MHz
8	RSTN	D, I, U	Chip reset, active low
48	DOUT[7]	D, O	Data output bit 7
47	DOUT[6]	D, I/O	Data output bit 6; if pulled up/down, the initial value of TIMING_CONTROL_LOW[2] (VSYNC polarity) is 1/0
46	DOUT[5]	D, I/O	Data output bit 5; if pulled up/down, the initial value of TIMING_CONTROL_LOW[1] (HSYNC polarity) is 1/0
44	DOUT[4]	D, I/O	Data output bit 4; if pulled up/down, the initial value of AD_IDL[3] (Sub ID) is 1/0
41	DOUT[3]	D, I/O	Data output bit 3; if pulled up/down, the initial value of AD_IDL[2] (Sub ID) is 1/0
39	DOUT[2]	D, I/O	Data output bit 2; if pulled up/down, the initial value of AD_IDL[1] (Sub ID) is 1/0
38	DOUT[1]	D, I/O	Data output bit 1; if pulled up/down, the initial value of AD_IDL[0] (Sub ID) is 1/0
37	DOUT[0]	D, I/O	Data output bit 0; if pulled up/down, the synchronization mode is in master/slave mode which requires HSYNC and VSYNC operating in output/input mode
3	HSYNC	D, I/O	Horizontal sync signal
5	VSYNC	D, I/O	Vertical sync signal
35	FLASH	D, O	Flash light control
15	RAMP	A, O	Analog ramp output
7, 31	VDDA	P	Sensor analog power
9, 30	GNDA	P	Sensor analog ground
19	VDDD	P	Sensor digital power
17	GNDD	P	Sensor digital ground
4, 43	VDDK	P	Digital power
6, 45	GNDK	P	Digital ground
40	VDDO	P	Pad power
42	GNDO	P	Pad ground
18	GNDS	P	Substrate ground

Class Code: A – Analog signal, D – Digital signal, I – Input, O – Output, P – Power or ground, U – Internal pull-up, N – Internal pull-down

2. Functional Description

ICM-105C is a single-chip digital color imaging device. It includes a 640x480 sensor array, 640 column-level ADC, and correlated double sampling circuitry. All the programmable parameters are set by writing into the SIF interface which can address the register file consisting of 8-bit registers. The output format is 8-bit raw data, together with horizontal and vertical sync signals.

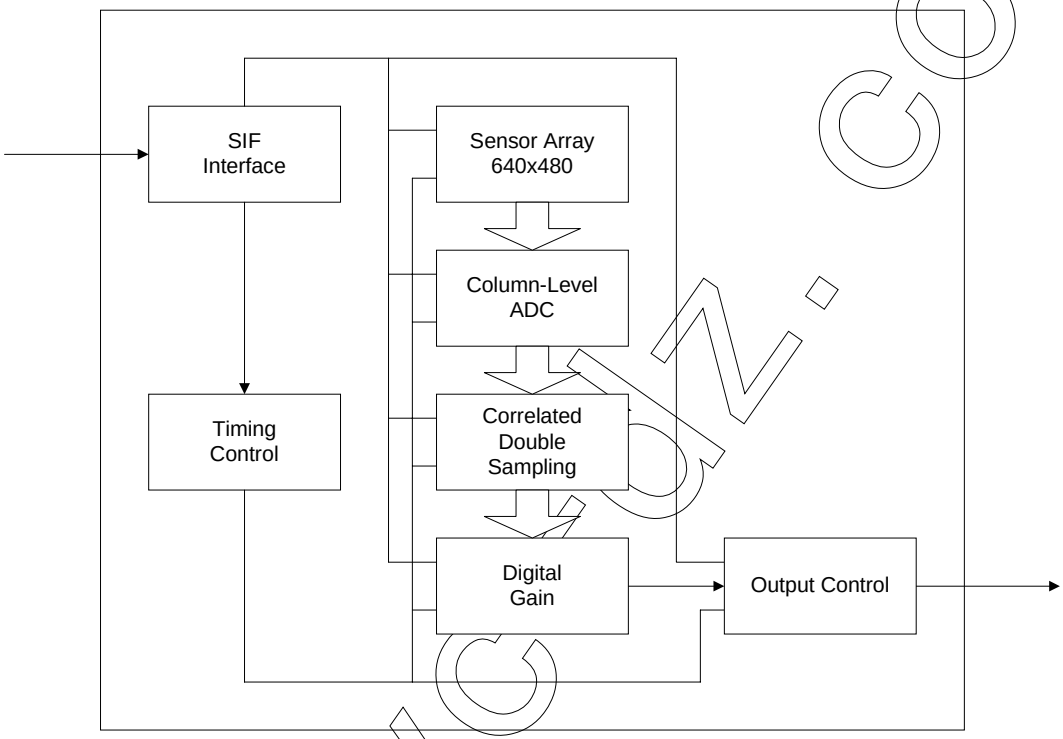
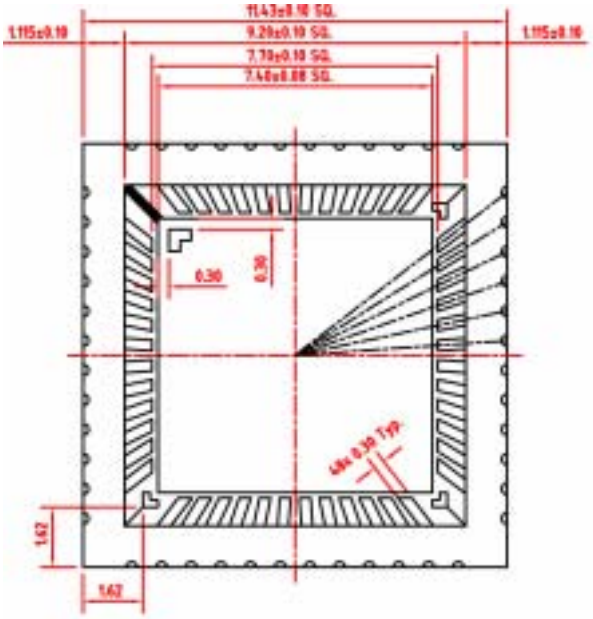
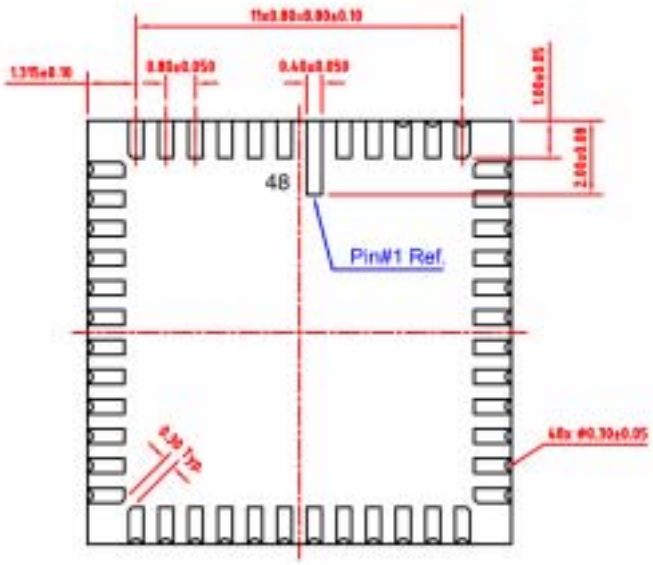


Figure 1. Block diagram

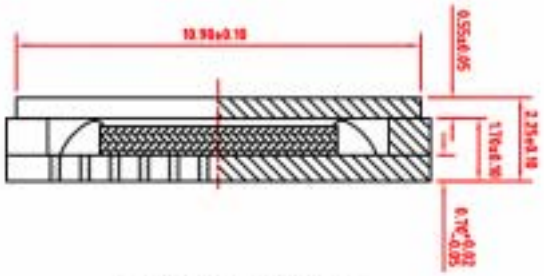
3. Mechanical Information



Unit Top View

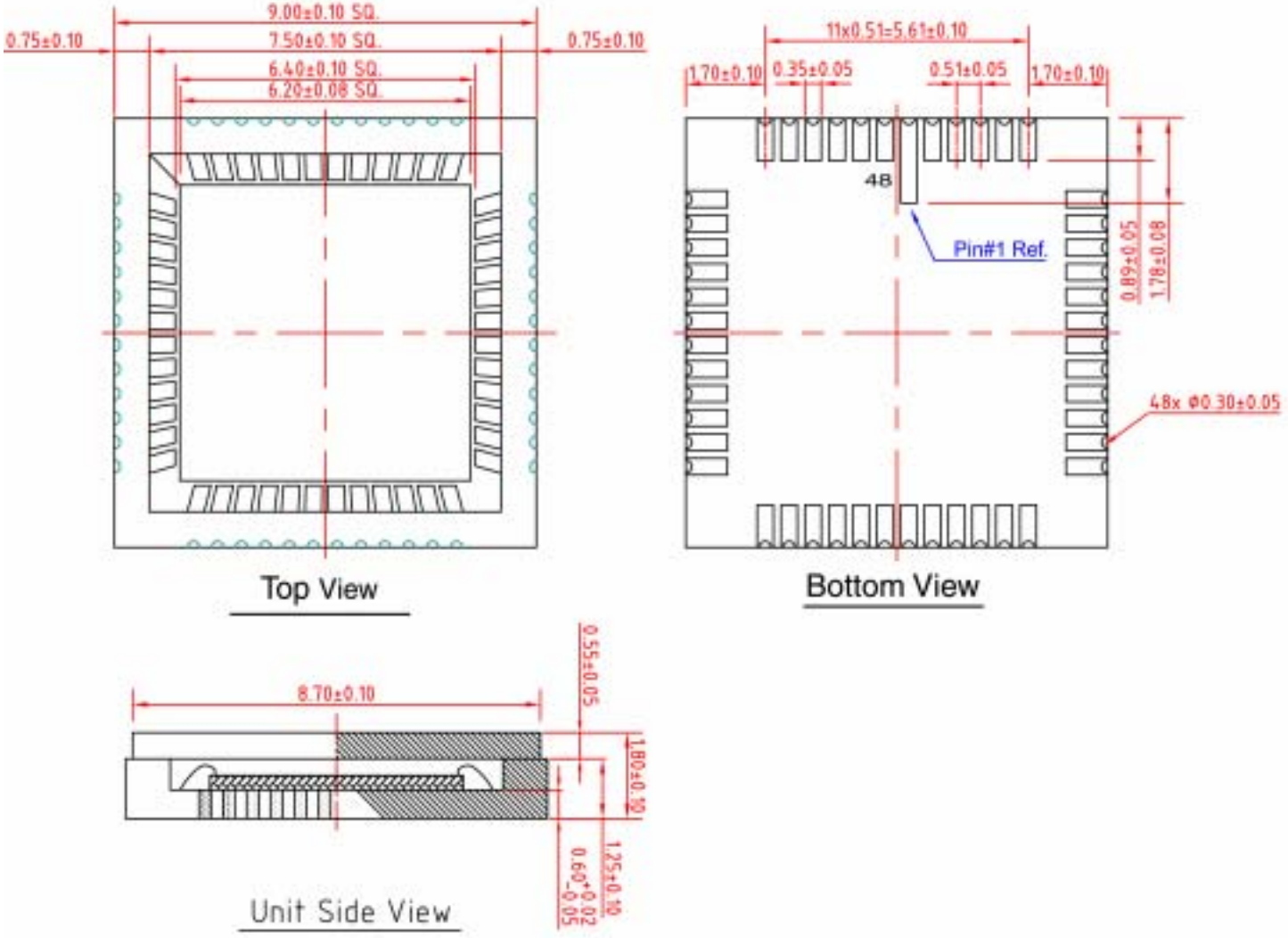


Unit Bottom View



Unit Side View

11.43 x 11.43 mm “S” Shrunk Plastic LCC48 Packaging



9 x 9 mm "T" Plastic LCC48 Packaging

4. Ordering Information

Description	*Package Size*	*Part Number*
VGA resolution sensor (3.3V), "S" PLCC48 Packaged	11.43 x 11.43 mm	ICM-105Csa
VGA resolution sensor (3.3V), "T" PLCC48 Packaged	9 x 9 mm	ICM-105Cta

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