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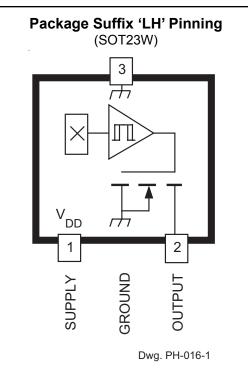
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# A3212

## MICROPOWER, ULTRA-SENSITIVE HALL-EFFECT SWITCH



Pinning is shown viewed from branded side.

#### **ABSOLUTE MAXIMUM RATINGS**

Supply Voltage, $V_{DD}$
Magnetic Flux Density, B Unlimited
Output Off Voltage, $V_{OUT}$ 5 V
Output Current, I <sub>OUT</sub> 1 mA
Junction Temperature, $T_J$
Operating Temperature, T <sub>A</sub>
Range 'E-'40°C to +85°C
Range 'L-'40°C to +150°C
Storage Temperature Range,

The A3212 integrated circuit is an ultra-sensitive, pole independent Halleffect switch with a latched digital output. This sensor is especially suited for operation in battery-operated, hand-held equipment such as cellular and cordless telephones, pagers, and palmtop computers. A 2.5 volt to 3.5 volt operation and a unique clocking scheme reduce the average operating power requirements to less than 15  $\mu$ W with a 2.75 volt supply.

Unlike other Hall-effect switches, either a north <u>or</u> south pole of sufficient strength will turn the output on; in the absence of a magnetic field, the output is off. The polarity independence and minimal power requirement allow these devices to easily replace reed switches for superior reliability and ease of manufacturing, while eliminating the requirement for signal conditioning.

Improved stability is made possible through chopper stabilization (dynamic offset cancellation), which reduces the residual offset voltage normally caused by device overmolding, temperature dependencies, and thermal stress.

This device includes on a single silicon chip a Hall-voltage generator, small-signal amplifier, chopper stabilization, a latch, and a MOSFET output. Advanced BiCMOS processing is used to take advantage of low-voltage and low-power requirements, component matching, very low input-offset errors, and small component geometries.

Three package styles provide a magnetically optimized package for most applications. Package suffixes 'EH' and 'LH' are for miniature low-profile (lead-less and leaded, respectively) surface-mount packages while suffix 'UA' is for a three-lead SIP for through-hole mounting. Each package is available in a lead (Pb) free version (suffix, -T) with 100% matte tin plated leadframe.

#### FEATURES

- Micropower Operation
- Operation with North or South Pole
- 2.5 V to 3.5 V Battery Operation
- Chopper Stabilized Superior Temperature Stability Extremely Low Switch-Point Drift Insensitive to Physical Stress
- ESD Protected to 5 kV
- Solid-State Reliability
- Small Size
- Easily Manufacturable with Magnet Pole Independence





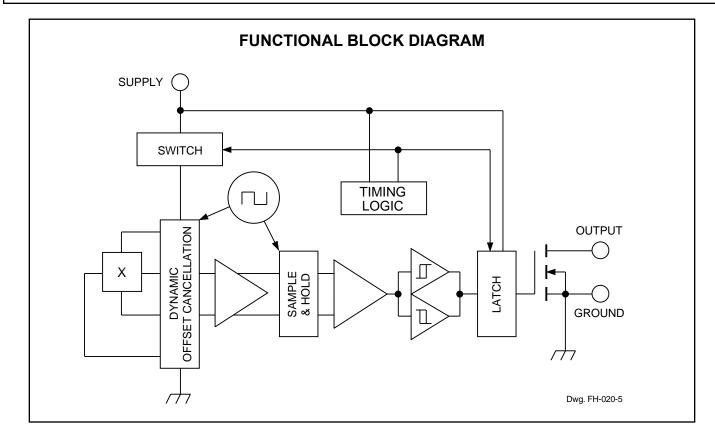
## **Product Selection Guide**

Use complete part numbers when ordering

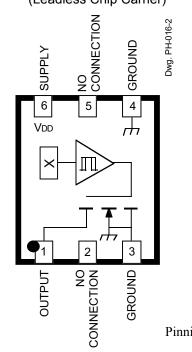
Part Number	Pb-free	Packing* (Units/Pack)	Package	Ambient Temperature T <sub>A</sub> (°C)	
A3212EEHLT	-	Tape and Reel (3000)	Leadless Surface Mount		
A3212EEHLT-T	Yes	Tape and Reel (3000)			
A3212ELHLT	-	Tape and Reel (3000)	3-Pin Surface Mount	-40 to 85	
A3212ELHLT-T	Yes	Tape and Reel (3000)	3-PIT Surface Mount	-40 10 65	
A3212EUA	-	Bulk Pack (500)	SIP-3 Through Hole, Straight Lead		
A3212EUA-T	Yes	Bulk Pack (500)	SIF-3 Through Hole, Straight Lead		
A3212LLHLT	_	Tape and Reel (3000)	3-Pin Surface Mount		
A3212LLHLT-T	Yes	Tape and Reel (3000)	3-PIT Surface Mount	40 to 150	
A3212LUA	_	Bulk Pack (500)	CID 2 Through Hole Straight Load	-40 to 150	
A3212LUA–T	Yes	Bulk Pack (500)	SIP-3 Through Hole, Straight Lead		

\*Contact Allegro for additional packaging and handling options.

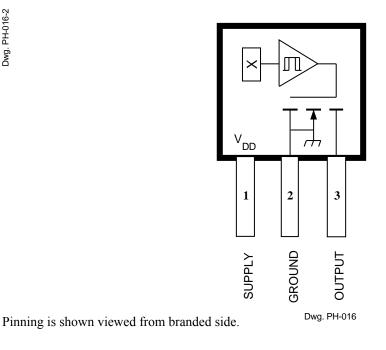




#### Package Suffix 'EH' Pinning (Leadless Chip Carrier)



Package Suffix 'UA' Pinning (SIP)



#### ELECTRICAL CHARACTERISTICS over operating voltage and temperature range (unless otherwise specified).

			Limits			
Characteristic	Symbol	Test Conditions	Min.	Тур.	Max.	Units
Supply Voltage Range	V <sub>DD</sub>	Operating <sup>1</sup>	2.5	2.75	3.5	V
Output Leakage Current	I <sub>OFF</sub>	V <sub>OUT</sub> = 3.5 V, B <sub>RPN</sub> < B < B <sub>RPS</sub>	-	<1.0	1.0	μA
Output On Voltage	V <sub>OUT</sub>	I <sub>OUT</sub> = 1 mA, V <sub>DD</sub> = 2.75 V	-	100	300	mV
Awake Time	t <sub>awake</sub>		-	45	90	μs
Period	t <sub>period</sub>		-	45	90	ms
Duty Cycle	d.c.		-	0.1	_	%
Chopping Frequency	f <sub>C</sub>		-	340	_	kHz
Supply Current	I <sub>DD(EN)</sub>	Chip awake (enabled)	-	_	2.0	mA
	I <sub>DD(DIS)</sub>	Chip asleep (disabled)	-	_	8.0	μA
	I <sub>DD(AVG)</sub>	V <sub>DD</sub> = 2.75 V	-	5.1	10	μA
		V <sub>DD</sub> = 3.5 V	-	6.7	10	μA

NOTES: 1. Operate and release points will vary with supply voltage.

2.  $B_{OPx}$  = operate point (output turns on);  $B_{RPx}$  = release point (output turns off).

3. Typical Data is at  $T_A = +25^{\circ}C$  and  $V_{DD} = 2.75$  V and is for design information only.

#### MAGNETIC CHARACTERISTICS over operating voltage and temperature range (unless otherwise specified).

			Limits			
Characteristic	Symbol	Test Conditions	Min.	Тур.	Max.	Units
Operate Points	B <sub>OPS</sub>	South pole to branded side	-	37	55	G
	B <sub>OPN</sub>	North pole to branded side	-55	-40	_	G
Release Points	B <sub>RPS</sub>	South pole to branded side	10	31	_	G
	B <sub>RPN</sub>	North pole to branded side	_	-34	-10	G
Hysteresis	B <sub>hys</sub>	B <sub>OPx</sub> - B <sub>RPx</sub>	_	5.9	_	G

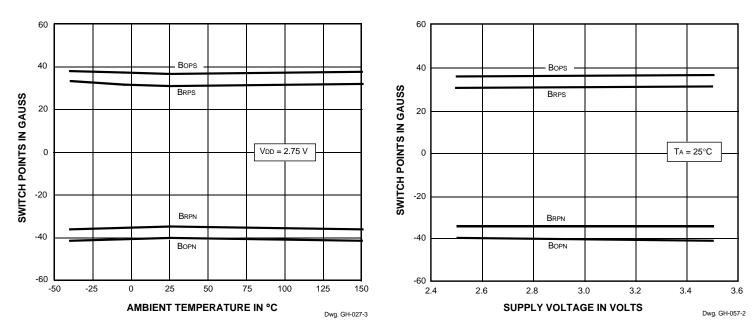
NOTES: 1. Negative flux densities are defined as less than zero (algebraic convention), i.e., -50 G is less than +10 G.

2.  $B_{OPx}$  = operate point (output turns on);  $B_{RPx}$  = release point (output turns off). 3. Typical Data is at  $T_A$  = +25°C and  $V_{DD}$  = 2.75 V and is for design information only.

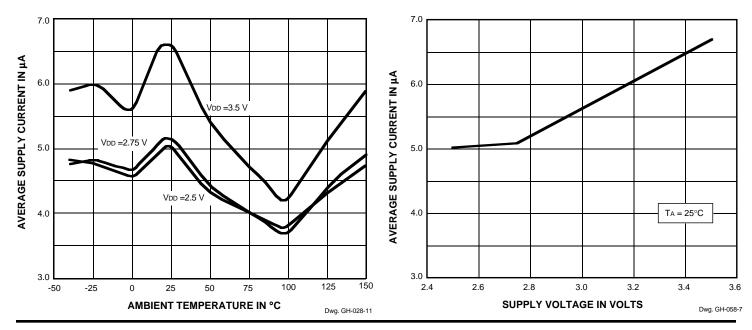
4. 1 gauss (G) is exactly equal to 0.1 millitesla (mT).



#### **TYPICAL OPERATING CHARACTERISTICS**



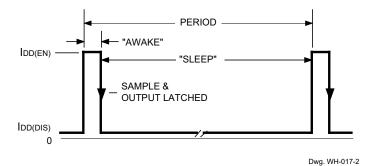
#### SWITCH POINTS



SUPPLY CURRENT

#### FUNCTIONAL DESCRIPTION

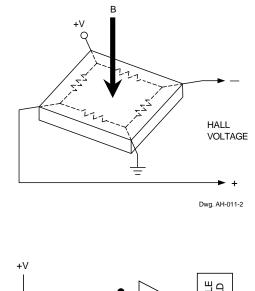
**Low Average Power.** Internal timing circuitry activates the sensor for 45  $\mu$ s and deactivates it for the remainder of the period (45 ms). A short "awake" time allows for stabilization prior to the sensor sampling and data latching on the falling edge of the timing pulse. The output during the "sleep" time is latched in the last sampled state. The supply current is not affected by the output state.

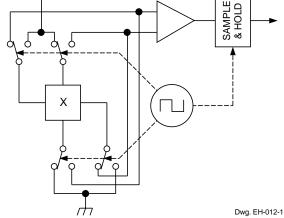


**Chopper-Stabilized Technique.** The Hall element can be considered as a resistor array similar to a Wheatstone bridge. A large portion of the offset is a result of the mismatching of these resistors. These devices use a proprietary dynamic offset cancellation technique, with an internal high-frequency clock to reduce the residual offset voltage of the Hall element that is normally caused by device overmolding, temperature dependencies, and thermal stress. The chopper-stabilizing technique cancels the mismatching of the resistor circuit by changing the direction of the current flowing through the Hall plate using CMOS switches and Hall voltage measurement taps, while maintaing the Hallvoltage signal that is induced by the external magnetic flux. The signal is then captured by a sample-and-hold circuit and further processed using low-offset bipolar circuitry. This technique produces devices that have an extremely stable quiescent Hall output voltage, are immune to thermal stress, and have precise recoverability after temperature cycling. A relatively high sampling frequency is used for faster signal processing capability can be processed.

More detailed descriptions of the circuit operation can be found in: Technical Paper STP 97-10, *Monolithic Magnetic Hall Sensor Using Dynamic Quadrature Offset Cancellation* and Technical Paper STP 99-1, *Chopper-Stabilized Amplifiers With A Track-and-Hold Signal Demodulator*.







#### FUNCTIONAL DESCRIPTION (cont'd)

**Operation.** The output of this device switches low (turns on) when a magnetic field perpendicular to the Hall sensor exceeds the operate point  $B_{OPS}$  (or is less than  $B_{OPN}$ ). After turn-on, the output is capable of sinking up to 1 mA and the output voltage is  $V_{OUT(ON)}$ . When the magnetic field is reduced below the release point  $B_{RPS}$  (or increased above  $B_{RPN}$ ), the device output switches high (turns off). The difference in the magnetic operate and release points is the hysteresis ( $B_{hys}$ ) of the device. This built-in hysteresis allows clean switching of the output even in the presence of external mechanical vibration and electrical noise.

As used here, negative flux densities are defined as less than zero (algebraic convention), i.e., -50 G is less than +10 G.

**Applications.** Allegro's pole-independent sensing technique allows for operation with either a north pole or south pole magnet orientation, enhancing the manufacturability of the device. The state-of-the-art technology provides the same output polarity for either pole face.

It is strongly recommended that an external bypass capacitor be connected (in close proximity to the Hall sensor) between the supply and ground of the device to reduce both external noise and noise generated by the chopper-stabilization technique. This is especially true due to the relatively high impedance of battery supplies.

The simplest form of magnet that will operate these devices is a bar magnet with either pole near the branded surface of the device. Many other methods of operation are possible. Extensive applications information for Hall-effect sensors is available in:

• Hall-Effect IC Applications Guide, Application Note 27701;

• Hall-Effect Devices: Soldering, Gluing, Potting, Encapsu-

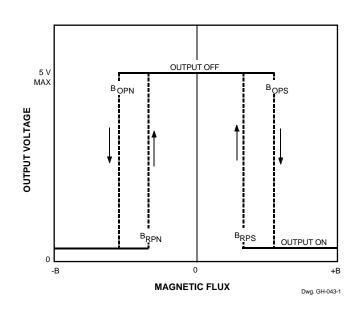
lating, and Lead Forming, Application Note 27703.1;

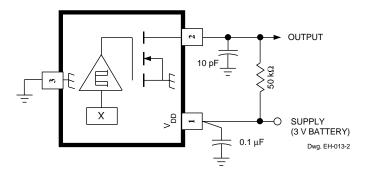
• *Soldering of Through-Hole Hall-Sensor Dervices*, Application Note 27703; and

• Soldering of Surface-Mount Hall-Sensor Devices, Application Note 27703.2.

All are provided at

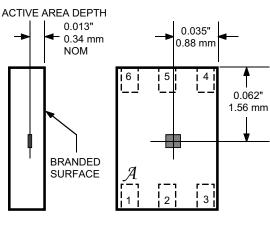
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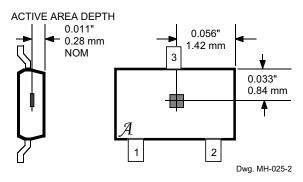
#### SENSOR LOCATIONS

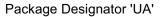
Package Designator 'EH'

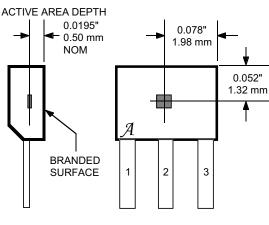


Dwg. MH-030

Package Designator 'LH'





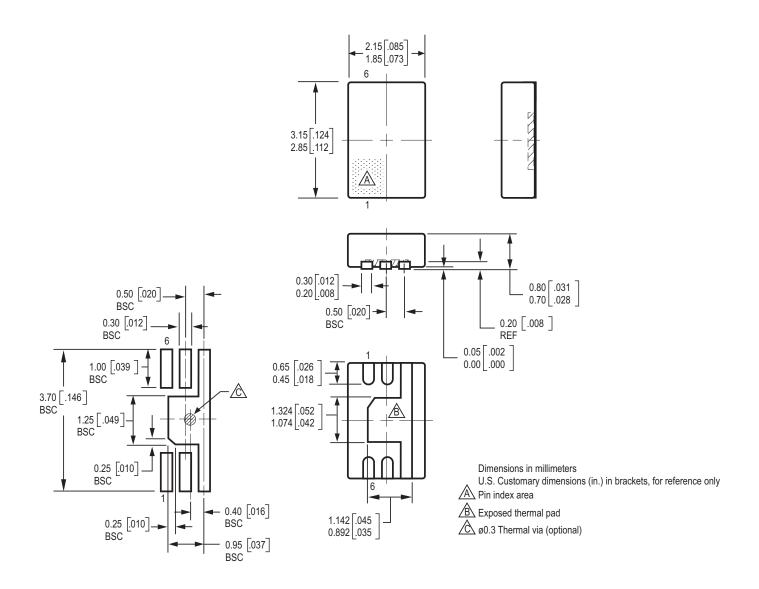


Dwg. MH-011-13

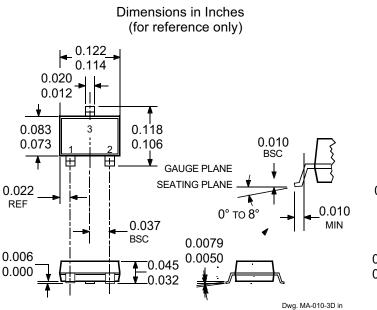


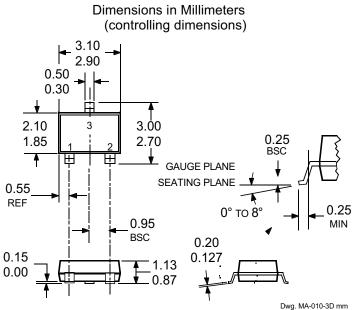
#### PACKAGE DESIGNATOR 'EH'

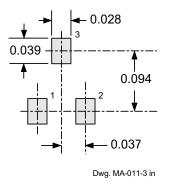
(Reference MO-229C WCED-1)

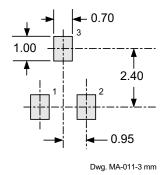


#### PACKAGE DESIGNATOR 'LH' (SOT23W, fits SC-59A solder-pad layout)



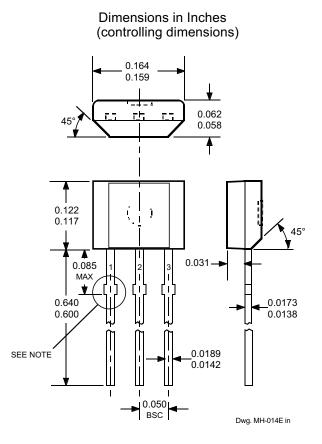






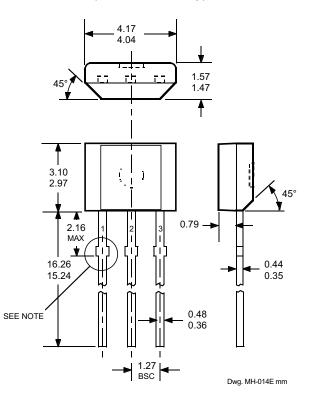
NOTES: 1. Tolerances on package height and width represent allowable mold offsets. Dimensions given are measured at the widest point (parting line).

- 2. Exact body and lead configuration at vendor's option within limits shown.
- 3. Height does not include mold gate flash.
- 4. Where no tolerance is specified, dimension is nominal.



#### PACKAGE DESIGNATOR 'UA'

Dimensions in Millimeters (for reference only)



- NOTES: 1. Tolerances on package height and width represent allowable mold offsets. Dimensions given are measured at the widest point (parting line).
  - 2. Exact body and lead configuration at vendor's option within limits shown.
  - 3. Height does not include mold gate flash.
  - 4. Recommended minimum PWB hole diameter to clear transition area is 0.035" (0.89 mm).
  - 5. Where no tolerance is specified, dimension is nominal.



The products described herein are manufactured under one or more of the following U.S. patents: 5,045,920; 5,264,783; 5,442,283; 5,389,889; 5,581,179; 5,517,112; 5,619,137; 5,621,319; 5,650,719; 5,686,894; 5,694,038; 5,729,130; 5,917,320; and other patents pending.

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