

## **SPLB20D Confirmation Sheet**

V1.9 01/15/2002

Project title			
Working Voltage			
ROSC on EMU board:  LCD Matrix: COM SEG Duty  Release code file (fill "00H" for unused area)  Binary filename:  LCD Display RAM: 64 bytes, \$00 ~ \$3F  CPU RAM: 128 bytes, \$80~\$FF  Data RAM: 2K bytes, \$1000~\$17FF  Program ROM: 30K bytes, \$8800-\$FFFF  Check  Fill Interrupt Vector: \$FFFA-\$FFFF  Mask option  32768Hz OSC. (mask option)  LOD Disable  By checking the enable box, users understand:  When system enters Low Voltage Mode:			
ROSC on EMU board:  LCD Matrix: COM SEG Duty  Port \$76 = (set as low as possible)  Release code file (fill "00H" for unused area)  Binary filename:  LCD Display RAM: 64 bytes, \$00 ~ \$3F  Check  CPU RAM: 128 bytes, \$80~\$FF  Data RAM: 2K bytes, \$1000~\$17FF  Check  Program ROM: 30K bytes, \$8800-\$FFF  Check  Fill Interrupt Vector: \$FFFA-\$FFFF  Mask option  32768Hz OSC. (mask option)  Low Voltage Power Down (mask option) □ Rable  By checking the enable box, users understand:  When system enters Low Voltage Mode:			
Release code file (fill "00H" for unused area)  Binary filename:  LCD Display RAM: 64 bytes, \$00 ~ \$3F  CPU RAM: 128 bytes, \$80~\$FF  Data RAM: 2K bytes, \$1000~\$17FF  Program ROM: 30K bytes, \$8800-\$FFF  Check  Fill Interrupt Vector: \$FFFA-\$FFFF  Mask option  32768Hz OSC. (mask option)  Low Voltage Power Down (mask option)			
Release code file (fill "00H" for unused area)  Binary filename:  LCD Display RAM: 64 bytes, \$00 ~ \$3F  CPU RAM: 128 bytes, \$80~\$FF  Data RAM: 2K bytes, \$1000~\$17FF  Program ROM: 30K bytes, \$8800-\$FFF  Gleck  Fill Interrupt Vector: \$FFFA-\$FFF  Mask option  32768Hz OSC. (mask option)  Low Voltage Power Down (mask option)   Binary file check sum:  Check  Check  Mask option  32768Hz OSC. (mask option)  Disable  By checking the enable box, users understand:  When system enters Low Voltage Mode:			
Binary file check sum:  LCD Display RAM: 64 bytes, \$00 ~ \$3F  CPU RAM: 128 bytes, \$80~\$FF  Data RAM: 2K bytes, \$1000~\$17FF  Program ROM: 30K bytes, \$8800-\$FFFF  Check  Fill Interrupt Vector: \$FFFA-\$FFFF  Mask option  32768Hz OSC. (mask option)  Low Voltage Power Down (mask option) □ Enable  By checking the enable box, users understand:  When system enters Low Voltage Mode:			
LCD Display RAM: 64 bytes, \$00 ~ \$3F			
CPU RAM: 128 bytes, \$80~\$FF			
Data RAM: 2K bytes, \$1000~\$17FF			
Program ROM: 30K bytes, \$8800-\$FFFF			
Fill Interrupt Vector: \$FFFA-\$FFFF			
Mask option  32768Hz OSC. (mask option)			
32768Hz OSC. (mask option)  Low Voltage Power Down (mask option)   By checking the enable box, users understand:  When system enters Low Voltage Mode:			
32768Hz OSC. (mask option)			
Port A \$73 (checked by "✓" or "≭" )			
b7 b6 b5 b4 b3 b2 b1 b0			
Input			
Output Part 275			
PortX-Y\$74         PortZ \$75           Segment 56 \$3         Segment 52 ~ 49         Segment 60 ~ 57			
Segment 56         53         Segment 52 ~ 49         Segment 60 ~ 57           b7         b6         b5         b4         b3         b2         b1         b0         b7 (C8)         b6 (C7)         b3         b2         b1         b0			
Select one only			
LCD 1/8 duty: C7 and C8 must be Output. 60 Segments: PortX, Y, Z must be Output.			
Port \$77 (Segment 1 ~ Segment 8)       Port \$78 (Segment 9 ~ Segment 16)         Used as key scan output       □Yes □No         Used as key scan output       □Yes □No			

TEL: 886-3-5786005 FAX: 886-3-5784418

## **SPLB20D Confirmation Sheet**



V1.9 01/15/2002

Hardware /Software			
All Instructions used are valid 6502 codes as specified by SUNPLUS (x2s.exe)			
The R1 (PortA key-scan pull resistor) on (\$7E.b2=1) consumes more power; normally, R1 should be set off.			
Program Tested by EPROM on Emulation Board (CPU internal) (If watchdog is code enabled, make sure the EMU board is also enabled)			
The b6 of P_7AH_SystemCtrl (\$7A) cannot be set to "1" if 32768Hz X'TAL is applied. In such case, write "1" to b7 to stop ROSC clock. See programming guide for more information.			
Test Program			
The following test program area and test program vectors are reserved for SUNPLUS. The user's program or data must not be in these ROM areas.			
Test Program Area \$8000 ~ \$87FF		Check	
Test Program Vector \$FFF2 ~ \$FFF7		Check	
General prograr	nming checklist		
The general programming checklist intends to provide some general characteristics about SUNPLUS devices. It is the			
customer's responsibility to check all the information in the list. No responsibility is assumed by SUNPLUS for any non-			
checked box even this confirmation sheet has been approved by SUNPLUS. Make sure the following conditions are			
met and verified:		Check	
CPU stack pointer must be reset after system power-on and wake-up.			
All RAM must be initialized after power on.			
Timer content must be initialized before timer interrupt is enabled.			
Do not enable interrupt before initializing RAM.  Check  The instructions of "SFI" and "CLI" must be removed from the IRQ and NMI service routines.			
The instructions of "SEI" and "CLI" must be removed from the IRQ and NMI service routines.			
Sleep port must be cleared and re-initialized before entering sleep mode.			
The used RAM not over the stack reserved area.			
Correct RAM/ROM size and start addresses.			
No current drain on I/O in sleep mode.  No I/O remains floating in sleep mode.			
Non-used I/O ports should be masked off (for input process).			
Example (suppose PortA [7:4] are invalid):			
LDA PortA ; read I/O port A Data			
AND #0FH ; mask off high nibble			
Document version			
Programming guide title and version:			
User's guide title and version:			
Other documents (if any):			
onor dodamento (ii dity).			
Development tool / board version			
EV board version:			
EV chip version:			
Piggyback / demo board version:			
Software / Hardware tools version:			
	SUNDLUS moto		
Customer note	SUNPLUS note		
Name(print): Tel:	Name(print): Tel:		
Signature:	Signature:		

Note: Please send/fax this form to SUNPLUS. SUNPLUS will return it back with signature.

TEL: 886-3-5786005 FAX: 886-3-5784418