

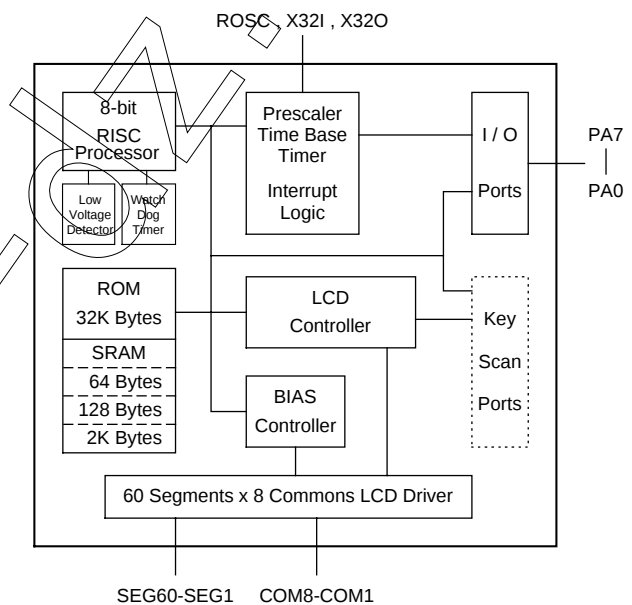
GENERAL DESCRIPTION

SPLB20D, an 8-bit CMOS microcontroller with advanced processing technology and mechanism by Sunplus, contains tons of functionalities in a compact package such as SRAM, ROM, I/Os, an interrupt controller, a timer and a LCD controller/driver. The amount of 30K bytes of ROM is able to provide proper space for LCD graphical data. The 128 bytes of CPU working SRAM are totally free to users. In addition, 8 I/Os, timer, LCD driver, NMI controller, Watch-Dog Timer, Low Voltage Power Down and other features increase the capability of driving sophisticated functions and displaying remarkable LCD graphics. SPLB20D is a high-end micro-controller that filled with modern technology and strong backup from Sunplus. Obviously, it is the most suitable product for your solution.

FEATURES

- 8-bit CPU (CPU14B)
- 30K bytes ROM
- 60 * 8 dual port SRAM for LCD display buffer
- 128 bytes SRAM for CPU working space
- 2K bytes SRAM for data
- 8 I/O ports
- LCD controller/driver (1/4 bias, $V_{op} = V_{DD}$, Type-B)
 - . 60 * 8 (480 dots)
 - . 60 * 6 (360 dots)
 - . 48 * 8 (384 dots)
 - . 48 * 6 (288 dots)
- Built-in R-oscillator and 32.768KHz crystal oscillator
- 8-bit Reloadable timer/counter with pre-scaler
- NMI controller with following sources
 - . 2Hz for RTC
 - . 128Hz
 - . Key(PA7-PA0)
 - . Counter overflow
- Halt and Standby mode
- Watch Dog Timer (WDT)
- Low Voltage Power Down (LVPD)
- Wide operating range: 2.4V – 5.5V @ 1.0MHz

BLOCK DIAGRAM



FUNCTION DESCRIPTION

■ ROM AREA

\$0000	LCD display buffer (64 bytes)
\$003F	
\$0040	Unused
\$006F	
\$0070	I/O Port / Registers
\$007F	
\$0080	CPU working SRAM (128 bytes)
\$00FF	
\$0100	Reserved
\$01FF	
\$1000	Data SRAM (2K bytes)
\$17FF	
\$8000	Test program ROM (2K bytes)
\$87FF	
\$8800	Program ROM (30K bytes)
\$FFFF	

The data SRAM address map : (2K bytes)

\$0200-\$07FF are mapping to SRAM \$1200-\$17FF

\$2000-\$27FF are mapping to SRAM \$1000-\$17FF

\$3000-\$37FF are mapping to SRAM \$1000-\$17FF

\$4000-\$47FF are mapping to SRAM \$1000-\$17FF

\$5000-\$57FF are mapping to SRAM \$1000-\$17FF

\$6000-\$67FF are mapping to SRAM \$1000-\$17FF

\$7000-\$77FF are mapping to SRAM \$1000-\$17FF

Note : \$FFF2-\$FFF7 are reserved for testing .

■ LCD MAPPING AND SPECIFICATION

\$00H - \$3F SRAM space is allocated for LCD display buffer. To display a pattern on LCD, user just write the corresponding bits of display buffer. The following table shows the mapping between LCD and display buffer.

	SEG8 - SEG1 (b7 - b0)	SEG16 - SEG9 (b7 - b0)	SEG24 - SEG17 (b7 - b0)	SEG32 - SEG25 (b7 - b0)	SEG40 - SEG33 (b7 - b0)	SEG48 - SEG41 (b7 - b0)	SEG56 - SEG49 (b7 - b0)	SEG60 - SEG57 (b7 - b0)
COM1	07H	06H	05H	04H	03H	02H	01H	00H
COM2	0FH	0EH	0DH	0CH	0BH	0AH	09H	08H
COM3	17H	16H	15H	14H	13H	12H	11H	10H
COM4	1FH	1EH	1DH	1CH	1BH	1AH	19H	18H
COM5	27H	26H	25H	24H	23H	22H	21H	20H
COM6	2FH	2EH	2DH	2CH	2BH	2AH	29H	28H
COM7	37H	36H	35H	34H	33H	32H	31H	30H
COM8	3FH	3EH	3DH	3CH	3BH	3AH	39H	38H

The SPLB20D supports LCD's with following characteristics:

Duty: 1/6 or 1/8

Bias: 1/4; $V_{LCD} = VDD$

$$V1 = VDD * 3/4$$

$$V2 = VDD * 2/4$$

$$V3 = VDD * 1/4$$

$$V_{EE} = GND$$

■ MASK OPTIONS:

1. 32K from Crystal / R-osc with prescaler

The system time base, LCD timing and auto-strobe signals are generated from 32.768KHz crystal oscillator. To support those systems without 32.768KHz crystal, this option is provided. When non-crystal mode is selected, the signals and timing listed above will be generated from prescaler. By programming register \$007C, users can get a suitable clock to replace 32.768KHz clock. Register \$007A:B5 can be used to turn off this clock.

2. DOGEN (WDT Enable) / DOGDIS (WDT Disable)

There is an on-chip WDT available on SPLB20D. The WDT is designed for recovering from system crash. If the system is hanged, WDT will generate a system reset to restart system after 1 second. If WDT is enabled, the WDT should be cleared every 0.5 seconds to avoid accidental reset. The WDT can be cleared by writing to \$007F. Note that the WDT only works when 32768 crystal is available.

3. Low Voltage Power Down (LVPD) Enable/Disable

Low Voltage Power Down circuit will be enabled only when 32768 signal is available. If LVPD circuit sensed $VDD \leq 2.2V$, the system will enter Low Voltage (standby) mode after R-osc stops. In Low Voltage mode current consumption will be minimized. This feature can be used to avoid possible data loss during battery replacement.

PIN DESCRIPTION

Mnemonic	PIN No.	Type	Description
VDD	25	I	Power supply input
VSS	52	I	Ground input
RESET	27	I	System reset input (internal pull-high), low active
TEST	21	I	Test input (internal pull-low), high active
X32I	29	I	32.768 KHz crystal input
X32O	28	O	32.768 KHz crystal output
ROSC	26	I	R-oscillator input, connect a resistor to VDD through a resistor
PA7 – PA0	37-30	I/O	Input / output port
COM8 – COM6 COM5 – COM3 COM2 – COM1	38-40 24-22 20-19	O	LCD common output
SEG60 – SEG50 SEG49 – SEG19 SEG18 – SEG1	41-51 53-83 1-9	O	LCD segment output.

Note 1: All of the SEG16 – SEG1 can be used as key strobe output pins by software programming register (\$007E). There are two kinds of combinations for key scan option.

No. of selected key scan port	The option for key scan port	(\$ 007E) bit 2, bit 1, bit 0
$No. \leq 8$	SEG8 – SEG1 or SEG16 – SEG9	1, 0, 1 1, 1, 0
$9 \leq No. \leq 16$	SEG16 - SEG1	1, 1, 1

Note 2: When the ROSC is selected, it is in the R-oscillator mode. Then the pin X32I should be connected to VSS and the pin X32O should be floating.

ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Ratings
DC Supply Voltage	V_{DD}	< 6V
Input Voltage Range	V_{IN}	-0.5V to $V_{DD} + 0.5V$
Operating Temperature	T_A	0°C to +60°C
Storage Temperature	T_{STO}	-50°C to +150°C

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

DC CHARACTERISTICS ($T_A = 25^\circ\text{C}$, $V_{DD} = 3V$)

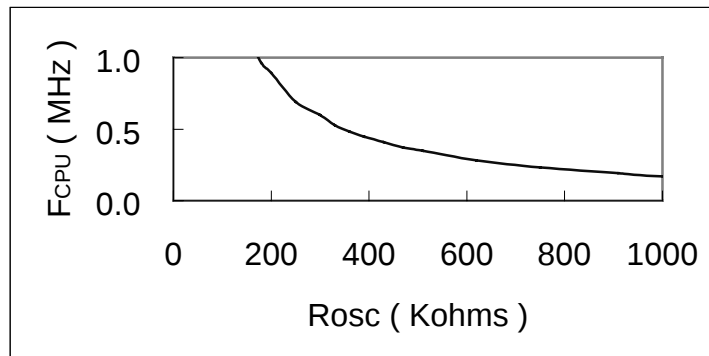
Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	V_{DD}	2.4	-	3.4	V	For 2-battery
Operating Current	I_{OP}	-	160	-	μA	$F_{CPU} = 500\text{KHz}$ @ 3V, no load
Standby Current	I_{STBY}	-	-	1.0	μA	$V_{DD} = 3V$, 32768Hz OFF
Input High Level	V_{IH}	2.0	-	-	V	$V_{DD} = 3V$
Input Low Level	V_{IL}	-	-	0.8	V	$V_{DD} = 3V$
Output High I (PA5 – PA0)	I_{OH}	-	1.0	-	mA	$V_{DD} = 3V$ $V_{OH} = 2V$
Output Sink I (PA5 – PA0)	I_{OL}	-	1.0	-	mA	$V_{DD} = 3V$ $V_{OL} = 1V$
Output High I (PA7 – PA6)	I_{OH}	-	2.5	-	mA	$V_{DD} = 3V$ $V_{OH} = 2V$
Output Sink I (PA7 – PA6)	I_{OL}	-	2.5	-	mA	$V_{DD} = 3V$ $V_{OL} = 1V$
OSC Resistor	R_{OSC}	-	350	-	Kohm	$F_{CPU} = 500\text{KHz}$ @ 3V
CPU Clock	F_{CPU}	-	-	1.0	MHz	$V_{DD} = 3V$

DC CHARACTERISTICS (TA = 25 °C, VDD = 4.5V)

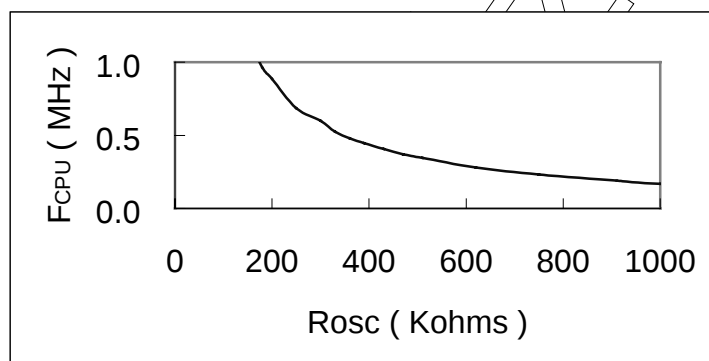
Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	V _{DD}	3.6	-	5.5	V	For 3-battery
Operating Current	I _{OP}	-	400	-	μA	F _{CPU} = 500KHz @ 4.5V, no load
Standby Current	I _{STBY}	-	-	1.0	μA	VDD = 4.5V, 32768Hz OFF
Input High Level	V _{IH}	3.0	-	-	V	VDD = 4.5V
Input Low Level	V _{IL}	-	-	0.8	V	VDD = 4.5V
Output High I (PA5 – PA0)	I _{OH}	-	-1.0	-	mA	VDD = 4.5V V _{OH} = 3.5V
Output Sink I (PA5 – PA0)	I _{OL}	-	1.0	-	mA	VDD = 4.5V V _{OL} = 0.8V
Output High I (PA7 – PA6)	I _{OH}	-	-3.0	-	mA	VDD = 4.5V V _{OH} = 3.5V
Output Sink I (PA7 – PA6)	I _{OL}	-	3.0	-	mA	VDD = 4.5V V _{OL} = 0.8V
OSC Resistor	R _{osc}	-	350	-	Kohm	F _{CPU} = 500KHz @ 4.5V
CPU Clock	F _{CPU}	-	-	1.0	MHz	VDD = 4.5V

The relationships between the R_{osc} and the F_{osc}

VDD = 3V, $T_a = 25^\circ\text{C}$



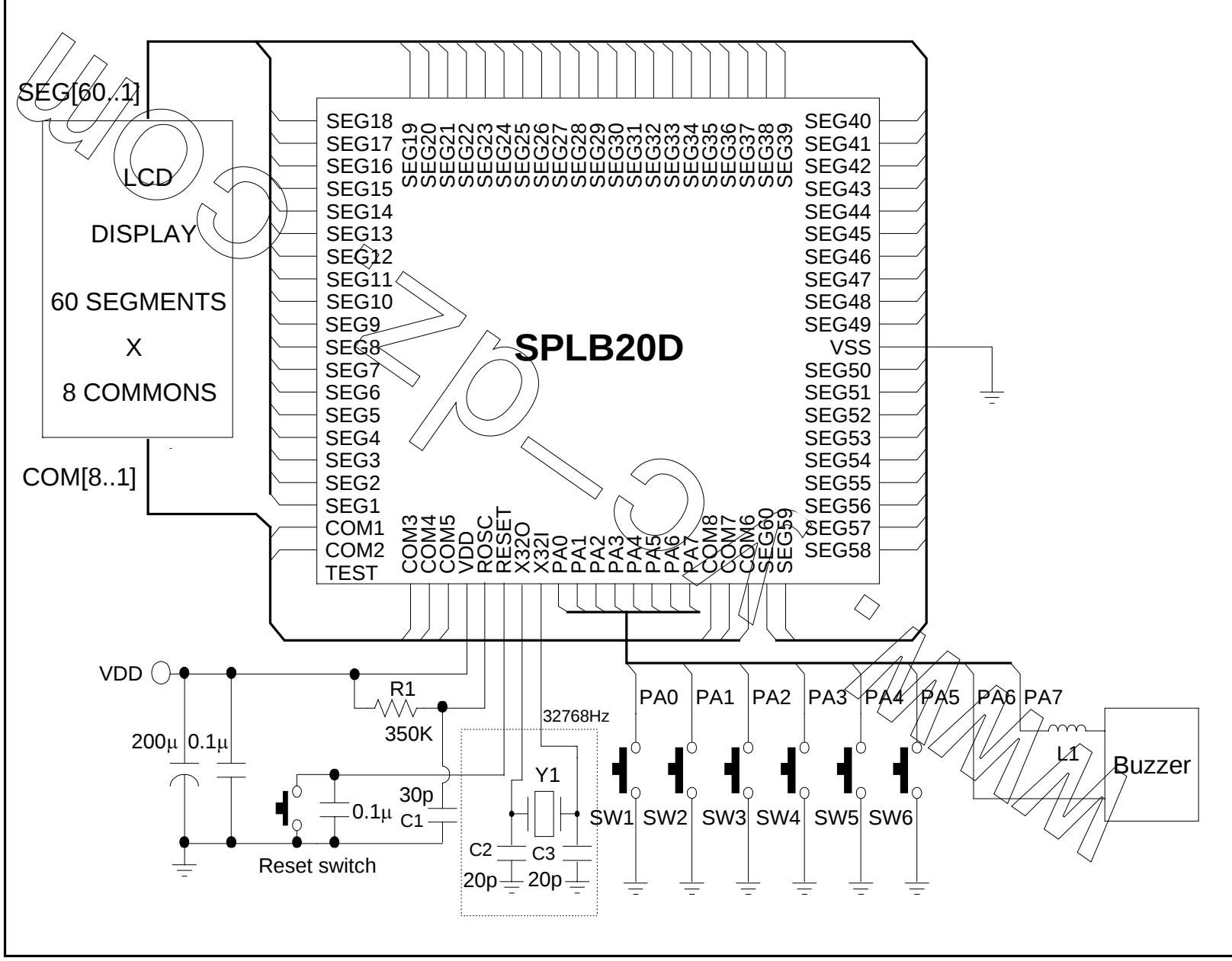
VDD = 4.5V, $T_a = 25^\circ\text{C}$

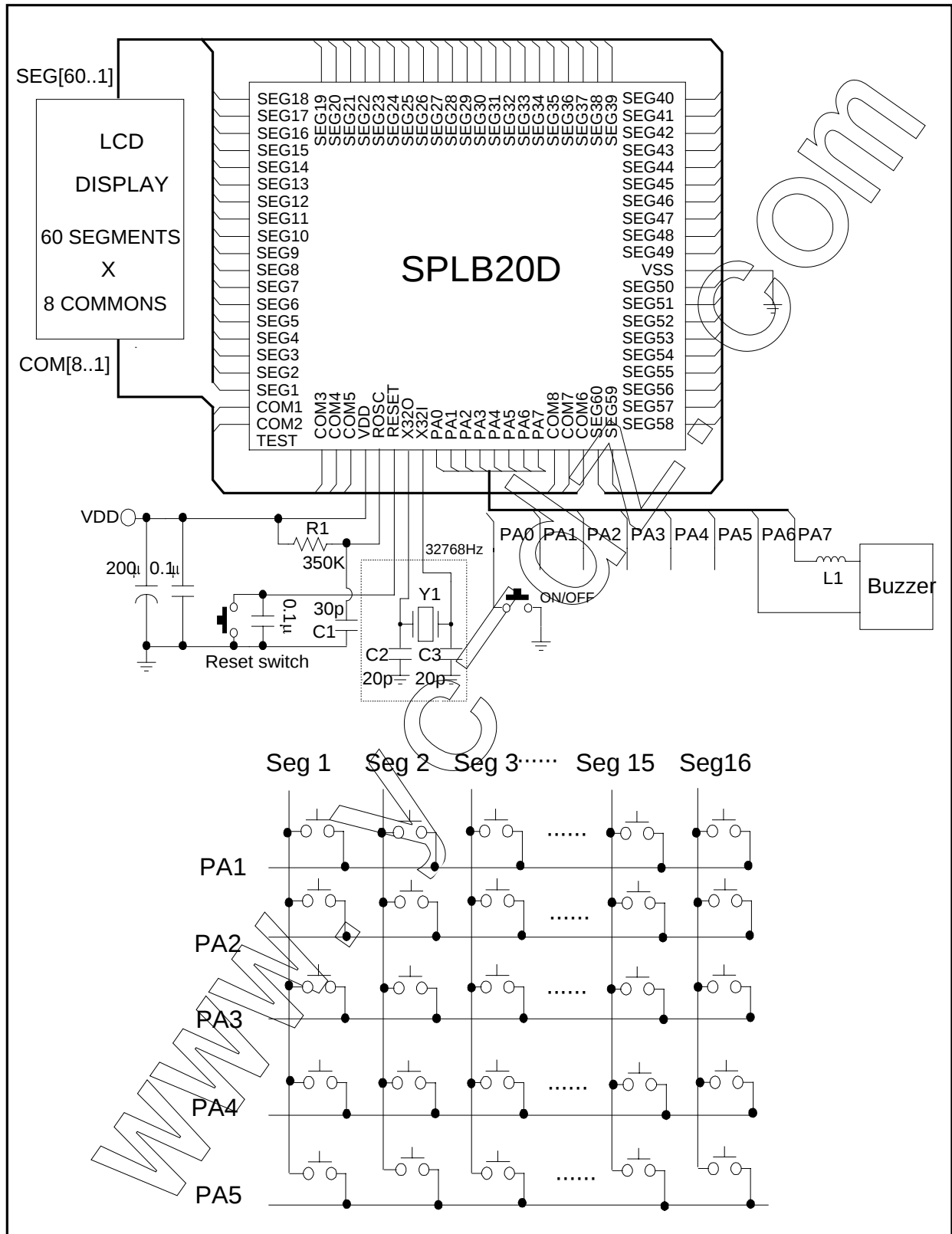




APPLICATION NOTES

■ SPLB20D Application Circuit





Note: 1. In the CRYSTAL mode, the accurate time base is generated from the 32768Hz crystal oscillator, the 32768Hz crystal oscillator should be installed.

2. In the ROSC mode, a suitable time base is generated from the R-Oscillator. The 32768Hz crystal oscillator is unnecessary to be installed.

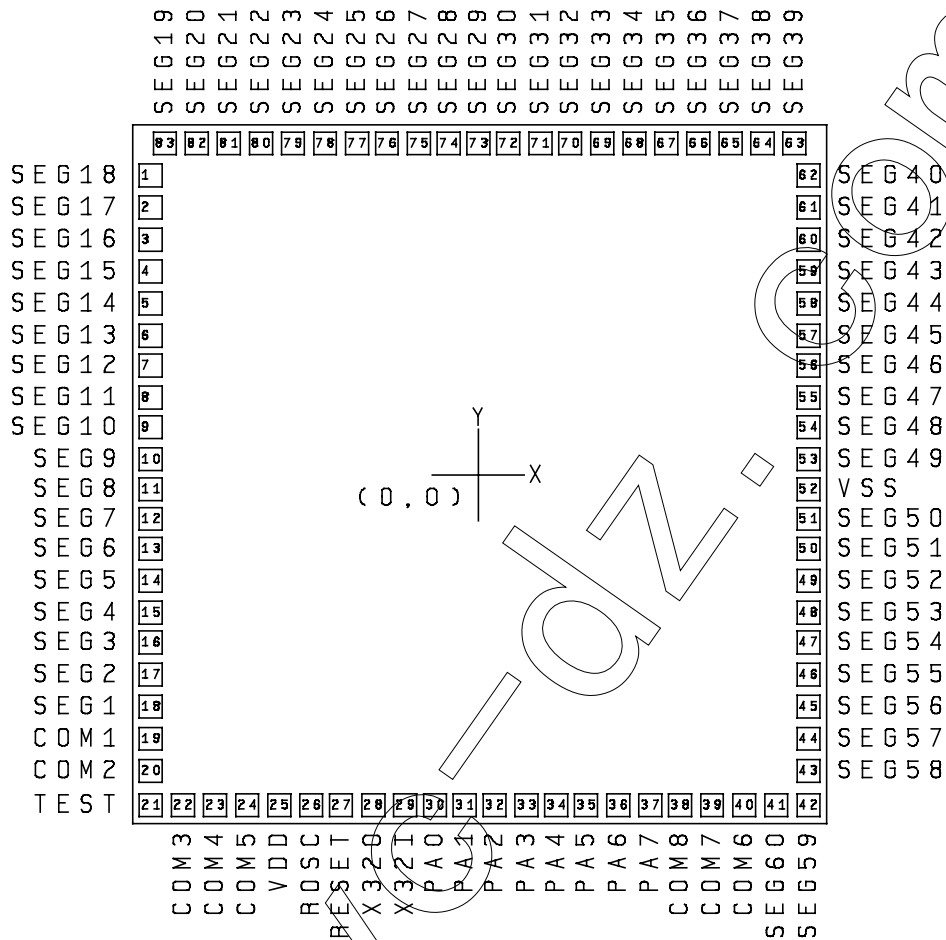
3. To avoid the noise interference on PCB around R-Oscillator and crystal circuit, following rules are suggested:

(1) R1 and C1 should be placed near to ROSC pin as possible.

(2) C2, C3 and crystal should be placed near to X32I and X32O as possible. A shielding by ground is suggested.

PAD ASSIGNMENT AND LOCATIONS

■ PAD Assignment



Note: To ensure that the IC functions properly, please bond all of VDD, VSS, AVDD and AVSS pins.

Ordering Information

Product Number	Package Type
SPLB20D-nnnnV-C	Chip form

Note1: Code number (nnnnV) is assigned for customer.

Note2: Code number (nnnn = 0000 - 9999); version (V = A - Z).

NOTE: SUNPLUS TECHNOLOGY CO., LTD reserves the right to make changes at any time without notice in order to improve the design and performance to supply the best possible product.

■ PAD Locations

Pad No	Pad Name	X	Y	Pad No	Pad Name	X	Y
1	SEG18	-1438	1306	33	PA3	202	-1448
2	SEG17	-1438	1166	34	PA4	334	-1448
3	SEG16	-1438	1026	35	PA5	469	-1448
4	SEG15	-1438	886	36	PA6	604	-1448
5	SEG14	-1438	746	37	PA7	741	-1448
6	SEG13	-1438	609	38	COM8	878	-1448
7	SEG12	-1438	472	39	COM7	1018	-1448
8	SEG11	-1438	337	40	COM6	1158	-1448
9	SEG10	-1438	202	41	SEG60	1300	-1448
10	SEG9	-1438	70	42	SEG59	1438	-1448
11	SEG8	-1438	-62	43	SEG58	1438	-1298
12	SEG7	-1438	-194	44	SEG57	1438	-1158
13	SEG6	-1438	-329	45	SEG56	1438	-1018
14	SEG5	-1438	-464	46	SEG55	1438	-878
15	SEG4	-1438	-601	47	SEG54	1438	-738
16	SEG3	-1438	-738	48	SEG53	1438	-601
17	SEG2	-1438	-878	49	SEG52	1438	-464
18	SEG1	-1438	-1018	50	SEG51	1438	-329
19	COM1	-1438	-1158	51	SEG50	1438	-194
20	COM2	-1438	-1298	52	VSS	1438	-62
21	TEST	-1438	-1448	53	SEG49	1438	70
22	COM3	-1298	-1448	54	SEG48	1438	202
23	COM4	-1158	-1448	55	SEG47	1438	337
24	COM5	-1018	-1448	56	SEG46	1438	472
25	VDD	-878	-1448	57	SEG45	1438	609
26	ROSC	-738	-1448	58	SEG44	1438	746
27	RESET	-601	-1448	59	SEG43	1438	886
28	X32O	-464	-1448	60	SEG42	1438	1026
29	X32I	-329	-1448	61	SEG41	1438	1166
30	PA0	-194	-1448	62	SEG40	1438	1306
31	PA1	-62	-1448	63	SEG39	1374	1448
32	PA2	70	-1448	64	SEG38	1234	1448

Pad No	Pad Name	X	Y	Pad No	Pad Name	X	Y
65	SEG37	1094	1448	75	SEG27	-266	1448
66	SEG36	954	1448	76	SEG26	-401	1448
67	SEG35	814	1448	77	SEG25	-536	1448
68	SEG34	674	1448	78	SEG24	-673	1448
69	SEG33	537	1448	79	SEG23	-810	1448
70	SEG32	400	1448	80	SEG22	-950	1448
71	SEG31	265	1448	81	SEG21	-1090	1448
72	SEG30	130	1448	82	SEG20	-1230	1448
73	SEG29	-2	1448	83	SEG19	-1370	1448
74	SEG28	-134	1448				

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