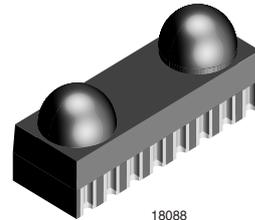


Low Profile 4 Mbit/s (FIR) Infrared Transceiver Module

Description

The Vishay TFBS6614 is a very low profile (2.7 mm) 4 Mbit/s Infrared Data Transceiver module. A PIN photodiode, an infrared emitter (IRED) and a low-power control IC are integrated in a single package that provides a total front-end solution.

V_{LOGIC} - allows a low-voltage controller to connect directly to TxD, RxD and SD/Mode logic signals of the transceiver hence eliminating the need for costly signal level converter and reducing power consumption.



Features

- Small size:
H 2.7 mm x W 3.33 mm x L 7.98 mm
- Typical 1.0 m link distance, typ. RC range 20 m
- Battery & power management features:
 - > Receive - 2 mA typical
 - > Shutdown - 10 nA typical
 - > Independent LED anode power supply
 - > Wide voltage range 2.7 V - 5.5 V
 - > High V_{CC} noise rejection > 100 mVPP
- The TxD-echo function is enabled
- V_{LOGIC} (1.5 V - 5.5 V) - Independent digital supply voltage
- Shutdown tri-states receiver output and disables TxD allowing bus interfacing
- High immunity to fluorescent light noise and AC field. No external shield required
- High DC ambient rejection - operates outdoors
- Directly interfaces with various super I/O and controller devices
- Lead(Pb)-free device
- Device in accordance to RoHS 2002/95/EC and WEEE 2002/96EC

Applications

- PDAs
- Mobile phones
- Notebook computers, desktop PCs
- Digital photo and video cameras
- External infrared adapters (Dongles)
- Diagnostics systems
- Medical and industrial data collection
- GPS

Ordering Information

Part Number	Description	Quantity / Reel
TFBS6614-TR3	Oriented in carrier tape for side view surface mounting	2500 pcs

Functional Block Diagram

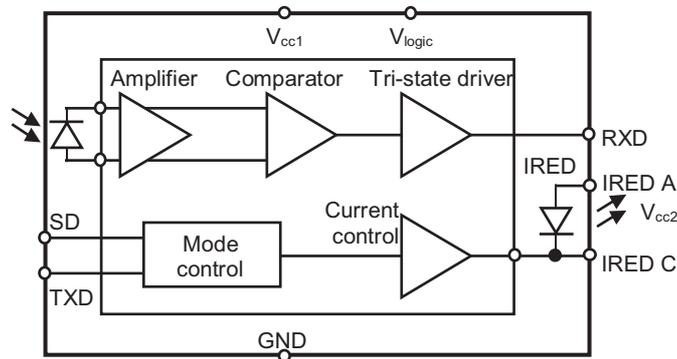
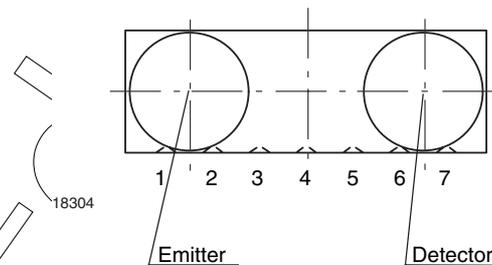


Figure 1. Functional Block Diagram

Pinout

TFBS6614, side view
Weight 80 mg



Pin Description

Pin Number	Function	Description	I/O	Active
1	IRED Anode	Connect IRED anode directly to V_{cc2} . For voltages higher than 3.6 V an external resistor might be necessary for reducing the internal power dissipation. An unregulated separate power supply can be used at this pin.		
2	IRED Cathode	IRED Cathode, internally connected to driver transistor		
3	TXD	This input is used to transmit serial data when SD is low. An on-chip protection circuit disables the LED driver if the Txd pin is asserted for longer than 100 μ s. When used in conjunction with the SD pin, this pin is also used to set the receiver speed mode.	I	high
4	RXD	Received Data Output, push-pull CMOS driver output capable of driving a standard CMOS or TTL load. No external pull-up or pull-down resistor is required. Floating with a weak pull-up of 500 k Ω (typ.) in shutdown mode.	O	low
5	SD	Shutdown, also used for dynamic mode switching. Setting this pin active places the module into shutdown mode. On the falling edge of this signal, the state of the Txd pin is sampled and used to set receiver low bandwidth (Txd = Low, SIR) or high bandwidth (Txd = High, MIR and FIR) mode.	I	high
6	V_{cc1}	Supply Voltage, analog part		
7	V_{logic}	Supply Voltage, digital part, I/O reference voltage for inputs and outputs.		
8	GND	Ground		



Absolute Maximum Ratings

Reference point Pin: GND unless otherwise noted

Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Parameter	Test Conditions	Symbol	Min	Typ.	Max	Unit
Supply voltage range, transceiver	$0\text{ V} < V_{CC2} < 6\text{ V}$	V_{CC1}	- 0.5		+ 6.0	V
IRED anode voltage	$0\text{ V} < V_{CC1} < 6\text{ V}$	V_{CC2}	- 0.5		+ 6.5	V
I/O reference voltage	$0\text{ V} < V_{CC2} < 6\text{ V}$ $0\text{ V} < V_{CC1} < 6\text{ V}$	V_{logic}	- 0.5		+ 6.0	V
Input current	For all pins, except IRED anode pin				10.0	mA
Output sinking current					25	mA
Power dissipation		P_D			500	mW
Junction temperature		T_J			125	°C
Ambient temperature range (Operating)		T_{amb}	- 25		+ 85	°C
Storage temperature range		T_{stg}	- 25		+ 85	°C
Soldering temperature	see recommended solder profiles (see figure 4, 5)				260	°C
Average output current		$I_{IRED(DC)}$			125	mA
Repetitive pulse output current	$< 90\ \mu\text{s}$, $t_{on} < 20\%$	$I_{IRED(RP)}$			600	mA
Voltage at all inputs and outputs	$V_{in} > V_{CC1}$ is allowed	V_{in}			5.5	V
Virtual source size	Method: (1-1/e) encircled energy	d	1.5	2.1		mm
Maximum Intensity for Laser Class 1 Operation of IEC60825-1 or EN60825-1, edition Jan. 2001*)					internal limitation to class 1	
IrDA® specified maximum limit					500	mW/sr
Due to the internal limitation measures the device is a "class 1" device under the specified conditions. It will not exceed the IrDA® intensity limit of 500mW/sr						

*) Sn/Pb and Pb-free soldering. The product passed VISHAY's standard convection reflow profile soldering test.

Definitions:

In the Vishay transceiver data sheets the following nomenclature is used for defining the IrDA operating modes:

SIR: 2.4 kbit/s to 115.2 kbit/s, equivalent to the basic serial infrared standard with the physical layer version IrPhy 1.0

MIR: 576 kbit/s to 1152 kbit/s

FIR: 4 Mbit/s

VFIR: 16 Mbit/s

MIR and FIR were implemented with IrPhy 1.1, followed by IrPhy 1.2, adding the SIR Low Power Standard. IrPhy 1.3 extended the Low Power Option to MIR and FIR and VFIR was added with IrPhy 1.4. A new version of the standard in any case obsoletes the former version.

Note: We apologize to use sometimes in our documentation the abbreviation LED and the word Light Emitting Diode instead of Infrared Emitting Diode (IRED) for IR -emitters. That is by definition wrong; we are here following just a bad trend.

Optoelectronic Characteristics

Transceiver

$T_{amb} = 25\text{ }^{\circ}\text{C}$, $V_{CC} = 2.7\text{ V}$ to 5.5 V unless otherwise noted.

Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Parameter	Test Conditions	Symbol	Min	Typ.	Max	Unit
Supply voltage		V_{CC}	2.7		5.5	V
Supply current (Idle) ¹⁾	SD = Low, $E_e = 0\text{ klx}$	I_{CC}		2	3	mA
Supply current (Idle) ¹⁾	SD = Low, $E_{e\text{ amb}} = 1\text{ klx}$ ²⁾	I_{CC}		2	3	mA
Supply current transmitting	SD = Low, Txd = High	I_{CC}			10	mA
Shutdown supply current	SD = High, $E_{e\text{ amb}} = 0\text{ klx}$	I_{SD}			2.0	μA
Shutdown supply current	SD = High, $E_{e\text{ amb}} = 1\text{ klx}$	I_{SD}			2.5	μA
Shutdown supply current	SD = High, $T = 85\text{ }^{\circ}\text{C}$, not ambient light sensitive	I_{SD}			5	μA
Operating temperature range		T_A	- 25		+ 85	$^{\circ}\text{C}$
Output voltage low	$I_{OL} = 1\text{ mA}$, $C_{Load} = 15\text{ pF}$	V_{OL}			0.4	V
Output voltage high	$I_{OL} = 500\text{ }\mu\text{A}$, $C_{Load} = 15\text{ pF}$	V_{OH}	$0.8 \times V_{CC}$			V
Output voltage high	$I_{OL} = 250\text{ }\mu\text{A}$, $C_{Load} = 15\text{ pF}$	V_{OH}	$0.9 \times V_{CC}$			V
Output Rxd current limitation high state	Short to ground				20	mA
Output Rxd current limitation low state	Short to V_{CC1}				20	mA
Rxd to V_{CC1} impedance	SD = High	R_{Rxd}	400	500	600	$\text{k}\Omega$
Input voltage low (Txd, SD)		V_{IL}	- 0.5		0.5	V
Input voltage high (Txd, SD)	CMOS level ³⁾ for shutdown current < $2\text{ }\mu\text{A}$	V_{IH}	$V_{CC} - 0.5$		$V_{CC} + 0.5$	V
Shutdown current	$V_{logic} = 3.3\text{ V}$ $V_{in(SD)} = 2.5\text{ V}$	I_{SD}		5		μA
Shutdown supply	$V_{logic} = 3.15\text{ V}$ $V_{in(SD)} = 2.5\text{ V}$	I_{SD}		0.5		μA
Input voltage high (Txd, SD)	TTL level, $V_{CC1} = 4.5\text{ V}$	V_{IH}	2.4			V
Input leakage current (Txd, SD)	- 25 $^{\circ}\text{C}$ to 85 $^{\circ}\text{C}$	I_L	- 10		+ 10	μA
Input capacitance (Txd, SD, Mode)		C_{IN}			5	pF

¹⁾ Receive mode only.

In transmit mode, add additional 85 mA (typ) for IRED current. Add Rxd output current depending on Rxd load.

²⁾ Standard Illuminant A.

³⁾ The typical threshold level between $0.5 \times V_{CC2}$ ($V_{CC} \leq 3\text{ V}$) and $0.4 \times V_{CC}$ ($V_{CC} = 5.5\text{ V}$). It is recommended to use the specified min/max values to avoid increased operating/shutdown current.

Receiver

$T_{amb} = 25\text{ }^{\circ}\text{C}$, $V_{CC} = 2.7\text{ V}$ to 5.5 V unless otherwise noted.

Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Parameter	Test Conditions	Symbol	Min	Typ.	Max	Unit
Minimum detection threshold irradiance ¹⁾ , SIR mode	9.6 kbit/s to 115.2 kbit/s $\lambda = 850\text{ nm}$ to 900 nm	E_e		40 (4)		mW/m^2 $(\mu\text{W/m}^2)$
Minimum detection threshold irradiance, FIR mode	4.0 Mbit/s $\lambda = 850\text{ nm}$ to 900 nm	E_e		100 (10)	150 (15)	mW/m^2 $(\mu\text{W/m}^2)$
Maximum detection threshold irradiance ²⁾	$\lambda = 850\text{ nm}$ to 900 nm	E_e	5 (500)			mW/m^2 (mW/m^2)
No detection receiver input irradiance	^{*)}	E_e	4 (0.4)			mW/m^2 $(\mu\text{W/m}^2)$
Rise time output signal	10 % to 90 %, 15 pF	$t_{r(\text{Rxd})}$	10		40	ns
Fall time of output signal	90 % to 10 %, 15 pF	$t_{f(\text{Rxd})}$	10		40	ns
Rxd pulse width of output signal, 50 %, SIR mode ^{**)}	input pulse length $1.4\text{ }\mu\text{s} < P_{Wopt} < 25\text{ }\mu\text{s}$	t_{PW}		2.1		μs
Rxd pulse width of output signal, 50 %, SIR mode	input pulse length $1.4\text{ }\mu\text{s} < P_{Wopt} < 25\text{ }\mu\text{s}$ $-25\text{ }^{\circ}\text{C} < T < 85\text{ }^{\circ}\text{C}$	t_{PW}	1.5	1.8	2.6	μs
Rxd pulse width of output signal, 50 %, MIR mode	input pulse length $P_{Wopt} = 217\text{ ns}$, 1.152 Mbit/s	t_{PW}	110	250	270	ns
Rxd pulse width of output signal, 50 %, FIR mode	input pulse length $P_{Wopt} = 125\text{ ns}$, 4.0 Mbit/s	t_{PW}	100		140	ns
Rxd pulse width of output signal, 50 %, FIR mode	input pulse length $P_{Wopt} = 250\text{ ns}$, 4.0 Mbit/s	t_{PW}	225		275	ns
Stochastic jitter, leading edge	$E_e = 100\text{ mW/m}^2$, 4.0 Mbit/s				20	ns
Stochastic jitter, leading edge	$E_e = 100\text{ mW/m}^2$, 1.152 Mbit/s				40	ns
Stochastic jitter, leading edge	$E_e = 100\text{ mW/m}^2$, 576 kbit/s				80	ns
Stochastic jitter, leading edge	$E_e = 100\text{ mW/m}^2$, $\leq 115.2\text{ kbit/s}$				350	ns
Receiver start up time	after completion of shutdown programming sequence Power on delay				500	μs
Latency		t_L		170	300	μs

Note: All timing data measured with 4 Mbit/s are measured using the IrDA[®] FIR transmission header. The data given here are valid 5 μs after starting the preamble.

*) This parameter reflects the backlight test of the IrDA physical layer specification to guarantee immunity against light from fluorescent lamps

***) Retriggering during applied optical pulse may occur

1) 2) **These terms are equivalent to the IrDA sensitivity definitions:**

1) **Minimum Irradiance E_e In Angular Range**, power per unit area. The receiver must meet the BER specification while the source is operating at the Minimum Intensity in Angular Range into the minimum Half-Angular Range at the maximum Link Length

2) **Maximum Irradiance E_e In Angular Range**, power per unit area. The optical power delivered to the detector by a source operating at the Maximum Intensity In Angular Range at **Minimum Link Length** must not cause receiver overdrive distortion and possible related link errors. If placed at the Active Output Interface reference plane of the transmitter, the receiver must meet its bit error ratio (BER) specification.

For more definitions see the document "Symbols and Terminology" on the Vishay Website
<http://www.vishay.com/docs/82512/82512.pdf>

Transmitter

$T_{amb} = 25\text{ }^{\circ}\text{C}$, $V_{CC} = 2.7\text{ V}$ to 5.5 V unless otherwise noted.

Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Parameter	Test Conditions	Symbol	Min	Typ.	Max	Unit
IRED operating current, switched current limiter	For 3.3 V operations no external resistor needed. For 5 V application that might be necessary depending on operating temperature range.	I_D	500	550	650	mA
Output leakage IRED current		I_{IRED}	-1		1	μA
Output radiant intensity recommended application circuit	$\alpha = 0^{\circ}, 15^{\circ}$ Txd = High, SD = Low, $V_{CC1} = V_{CC2} = 3.3\text{ V}$ Internally current-controlled, no external resistor	I_e	90	110	400	mW/sr
Output radiant intensity	$V_{CC1} = 5.0\text{ V}$, $\alpha = 0^{\circ}, 15^{\circ} = \text{Low}$ or SD = High (receiver is inactive as long as SD = High)	I_e			0.04	mW/sr
Output radiant intensity, angle of half intensity		α		± 24		$^{\circ}$
Peak - emission wavelength		λ_p	880	886	900	nm
Spectral bandwidth		$\Delta\lambda$		40		nm
Optical rise time, fall time		$t_{r,opt}, t_{f,opt}$	10		40	ns
Optical output pulse duration	input pulse width 217 ns, 1.152 Mbit/s	t_{opt}	207	217	227	ns
Optical output pulse duration	input pulse width 125 ns, 4.0 Mbit/s	t_{opt}	117	125	133	ns
Optical output pulse duration	input pulse width 250 ns, 4.0 Mbit/s	t_{opt}	242	250	258	ns
Optical output pulse duration	input pulse width $0.1\text{ }\mu\text{s} < t_{Txd} < 100\text{ }\mu\text{s}$ ^{*)}	t_{opt}		t_{Txd}		μs
Optical output pulse duration	input pulse width $t_{Txd} \geq 100\text{ }\mu\text{s}$ ^{*)}	t_{opt}	23		100	μs
Optical overshoot					25	%

^{*)} Typically the output pulse duration will follow the input pulse duration t and will be identical in length t . However, at pulse duration larger than $100\text{ }\mu\text{s}$ the optical output pulse duration is limited to $100\text{ }\mu\text{s}$. This pulse duration limitation can already start at $23\text{ }\mu\text{s}$.

Mode Switching

The TFBS6614 is in the SIR mode after power on as a default mode, therefore the FIR data transfer rate has to be set by programming sequence using the Txd and SD inputs as described below. The low frequency mode covers speeds up to 115.2 kbit/s. Signals with higher data rates should be detected in the high frequency mode. Lower frequency data can also be received in the high frequency mode but with reduced sensitivity. To switch the transceivers from low frequency mode to the high frequency mode and vice versa, the programming sequences described below are required.

Setting to the High Bandwidth Mode (0.576 Mbit/s to 4 Mbit/s)

1. Set SD/ Mode input to logic "High".
2. Set TxD input to logic "High". Wait $t_s \geq 200\text{ ns}$.
3. Set SD/ Mode to logic "Low" (the negative edge latches state of TxD, which determines speed setting).
4. After waiting $t_h \geq 200\text{ ns}$ TxD can be set to logic "Low". The hold time of TxD is limited by the maximum allowed pulse width.

TxD is now enabled as normal TxD input for the high bandwidth mode.

Setting to the Lower Bandwidth Mode (2.4 kbit/s to 115.2 kbit/s)

1. Set SD/ Mode input to logic "High".
 2. Set TxD input to logic "Low". Wait $t_s \geq 200$ ns.
 3. Set SD/ Mode to logic "Low" (the negative edge latches state of TxD, which determines speed setting).
 4. TxD must be held for $t_h \geq 200$ ns.
- TxD is now enabled as normal TxD input for the lower bandwidth mode.

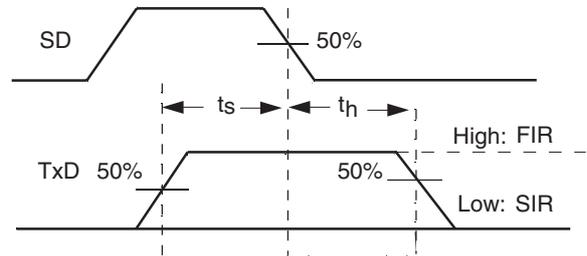


Figure 2. Mode Switching Timing Diagram

Truth table

Inputs			Outputs	
SD	Txd	Optical input Irradiance mW/m ²	Rxd	Transmitter
high	x	x	weakly pulled (500 kΩ) to V _{cc1}	0
low	high	x	low (active)	I _e
low	high > 80 μs	x	high	0
low	low	< 4	high	0
low	low	> Min. Detection Threshold Irradiance < Max. Detection Threshold Irradiance	low (active)	0
low	low	> Max. Detection Threshold Irradiance	x	0

Recommended Circuit Diagram

Operated at a clean low impedance power supply the TFBS6614 needs no additional external components when the internal current control is used. For reducing the IRED drive current for low power applications with reduced range an additional resistor can be used to connect the IRED to the separate power supply. Depending on the entire system design and board layout, additional components may be required. (see figure 3).

Worst-case conditions are test set-ups with long cables to power supplies. In such a case capacitors are necessary to compensate the effect of the cable inductance. In case of small applications as e.g. mobile phones where the power supply is close to the transceiver big capacitors are normally not necessary.

The TFBS6614 is designed to operate in system with logical I/O level independent of the supply voltage. It can interface to IR controllers with low voltage logic from 1.5 V upwards to TTL (5 V). The reference voltage is to be connected to the V_{logic} input.

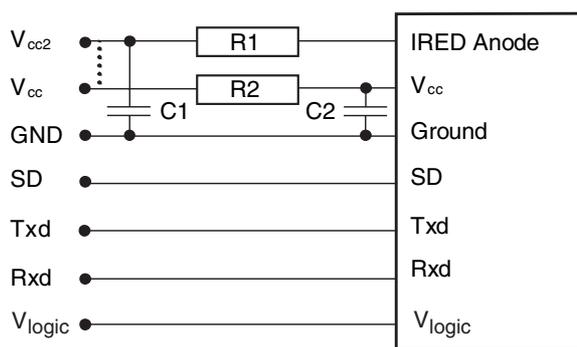


Figure 3. Recommended Application Circuit

The capacitor C1 is buffering the supply voltage and eliminates the inductance of the power supply line. This one should be a small ceramic version or other

fast capacitor to guarantee the fast rise time of the IRED current. The resistor R1 is optional for reducing the IRED drive current.

Vishay transceivers integrate a sensitive receiver and a built-in power driver. The combination of both needs a careful circuit board layout. The use of thin, long, resistive and inductive wiring should be avoided. The inputs (Txd, SD) and the output Rxd should be directly (DC) coupled to the I/O circuit.

The capacitor C2 combined with the resistor R2 is the low pass filter for smoothing the supply voltage when noisy supply voltage is used or pick-up via the wiring is expected.

R2, C1 and C2 are optional and dependent on the quality of the supply voltage V_{ccx} and injected noise. An unstable power supply with dropping voltage during transmission may reduce the sensitivity (and transmission range) of the transceiver.

The placement of these parts is critical. It is strongly recommended to position C2 as close as possible to the transceiver power supply pins.

In any case, when connecting the described circuit to the power supply, low impedance wiring should be used.

When extended wiring is used the inductance of the power supply can cause dynamically a voltage drop at V_{cc2} . Often some power supplies are not to follow the fast current rise time. In that case another 10 μ F capacitor at V_{cc2} will be helpful.

The recommended components in table 1 are for test set-ups

Keep in mind that basic RF - design rules for circuit design should be taken into account. Especially longer signal lines should not be used without termination. See e.g. "The Art of Electronics" Paul Horowitz, Winfield Hill, 1989, Cambridge University Press, ISBN: 0521370957.

Table 1.
Recommended Application Circuit Components

Component	Recommended Value	Vishay Part Number
C1, C2	0.1 μ F, Ceramic	VJ 1206 Y 104 J XXMT
R1	Supply voltage > 3.6 V: add a resistor in series e.g. 2 Ω . The internal controller is able to limit the current to about 550 mA.	
R2	10 Ω , 0.125 W	

Recommended Solder Profile

Solder Profile for Sn/Pb soldering

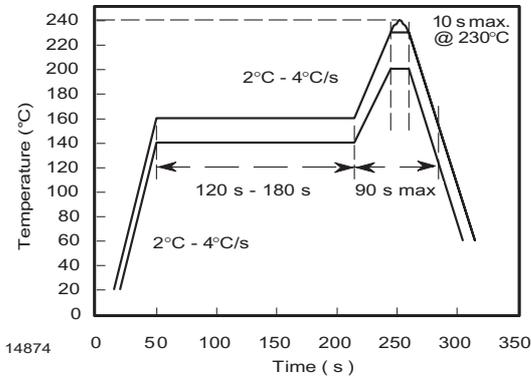


Figure 4. Recommended Solder Profile for Sn/Pb soldering

Lead-Free, Recommended Solder Profile

The TFBS6614 is a lead-free transceiver and qualified for lead-free processing. For lead-free solder paste like Sn_(3.0 - 4.0)Ag_(0.5 - 0.9)Cu, a Ramp-Soak-Spike (RSS) reflow profile is recommended. Shown

below in figure 5 is Vishay's recommended profile for use with the TFBS6614 transceivers. For more details please refer to Application note: SMD Assembly Instruction.

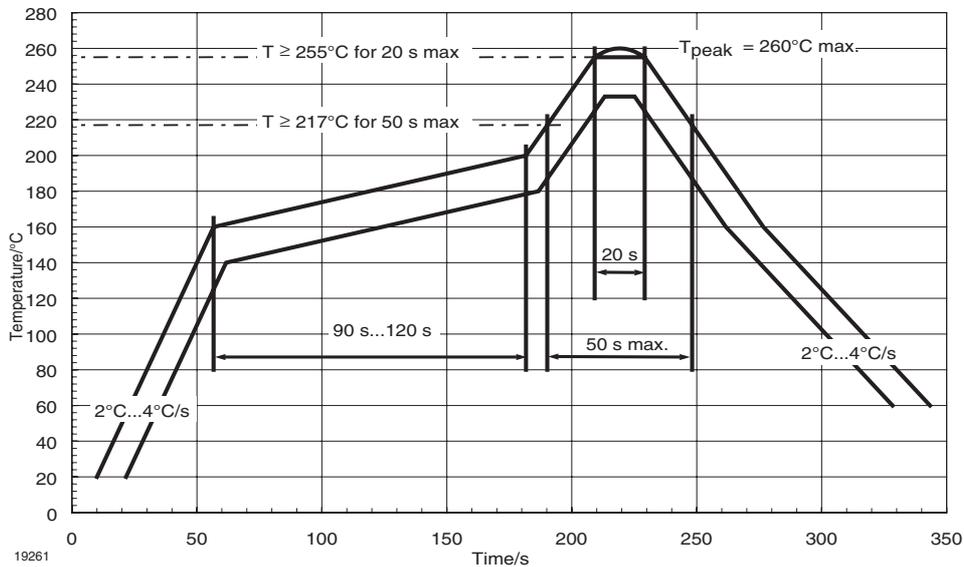
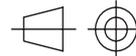
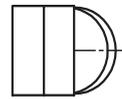
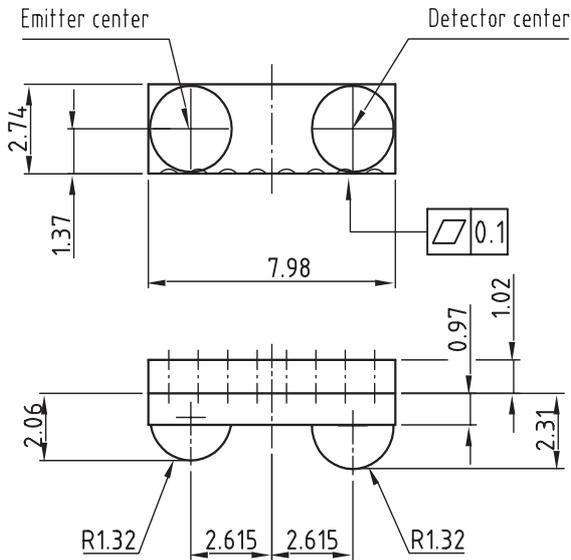


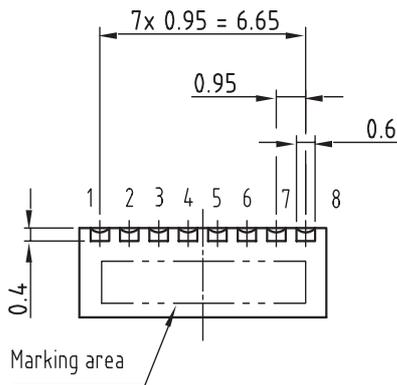
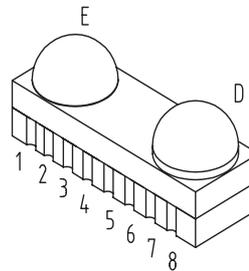
Figure 5. Solder Profile, RSS Recommendation

TFBS6614 Mechanical Dimensions in mm

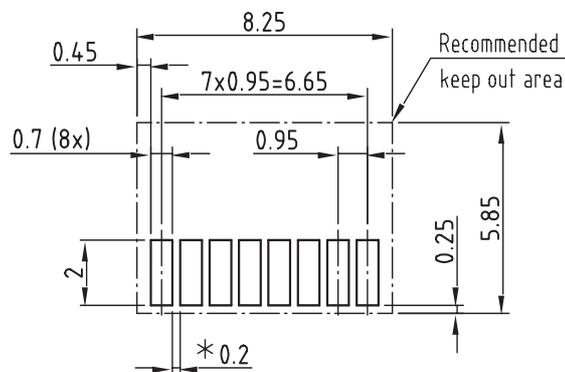


technical drawings
according to DIN
specifications

All dimensions in mm
Tolerances ± 0.2



Recommended PCB Footprint

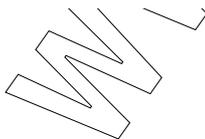


* min 0.2 Photoimageable
solder mask recommended
between pads to prevent bridging

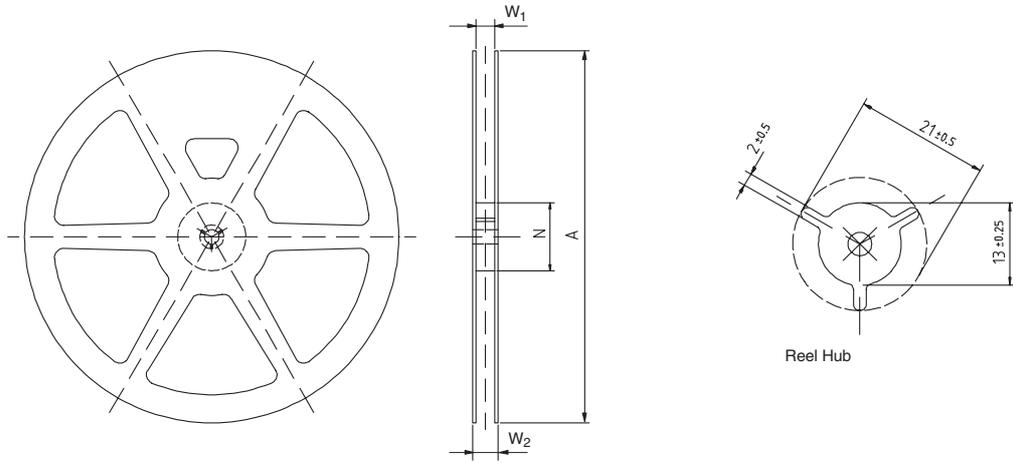
Drawing-No.: 6.550-5258.01-4

Issue: 1; 24.06.03

18074



Reel Dimensions



14017

Tape Width	A max.	N	W_1 min.	W_2 max.	W_3 min.	W_3 max.
mm	mm	mm	mm	mm	mm	mm
24	330	60	24.4	30.4	23.9	27.4

www.vishay.com

Ozone Depleting Substances Policy Statement

It is the policy of Vishay Semiconductor GmbH to

1. Meet all present and future national and international statutory requirements.
2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

Vishay Semiconductor GmbH has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively
2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA
3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

Vishay Semiconductor GmbH can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

We reserve the right to make changes to improve technical design and may do so without further notice.

Parameters can vary in different applications. All operating parameters must be validated for each customer application by the customer. Should the buyer use Vishay Semiconductors products for any unintended or unauthorized application, the buyer shall indemnify Vishay Semiconductors against all claims, costs, damages, and expenses, arising out of, directly or indirectly, any claim of personal damage, injury or death associated with such unintended or unauthorized use.

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