Broadcom WLAN Chipset for 802.11a/b/g

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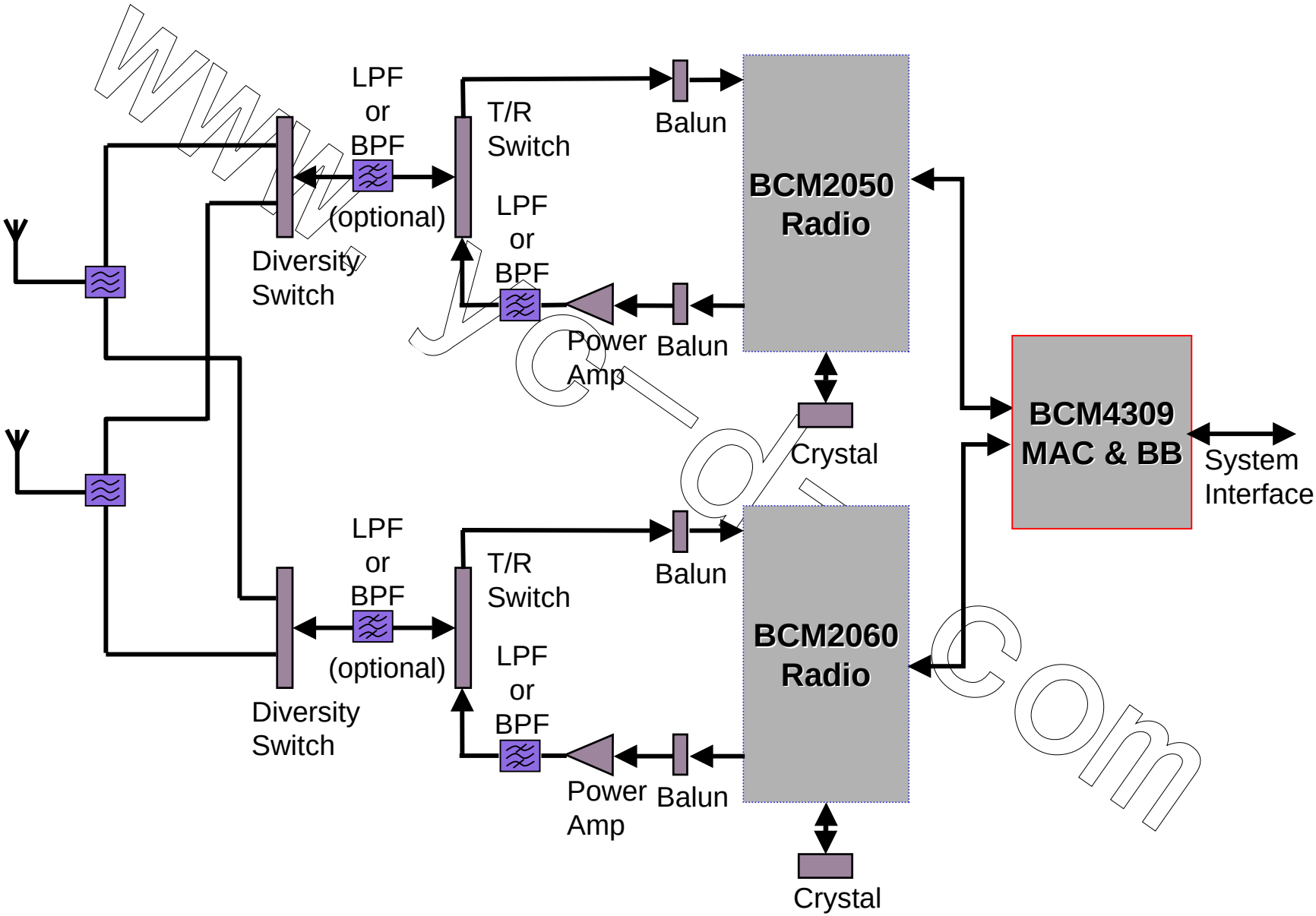
Broadcom Corporation, CA, USA

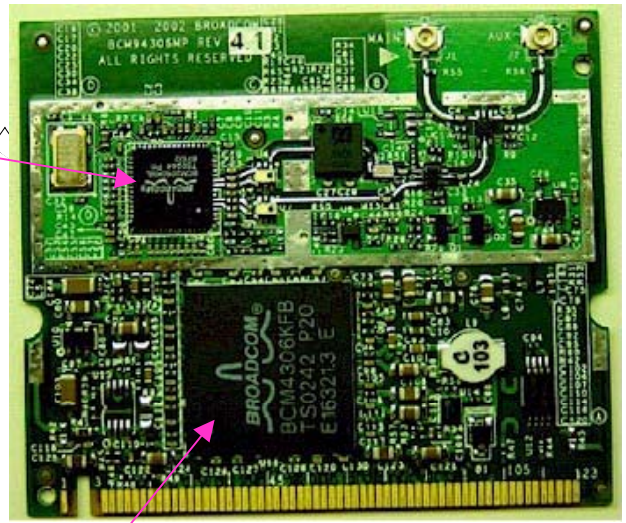
Outline

- **Transceiver Architecture**
  - Baseband IC (BCM4306)
  - .11g RFIC (BCM2050)
  - .11a RFIC (BCM2060)
- System Measurement Results
- Conclusion

Dual Band Overall Block Diagram



Single-band MiniPCI Card



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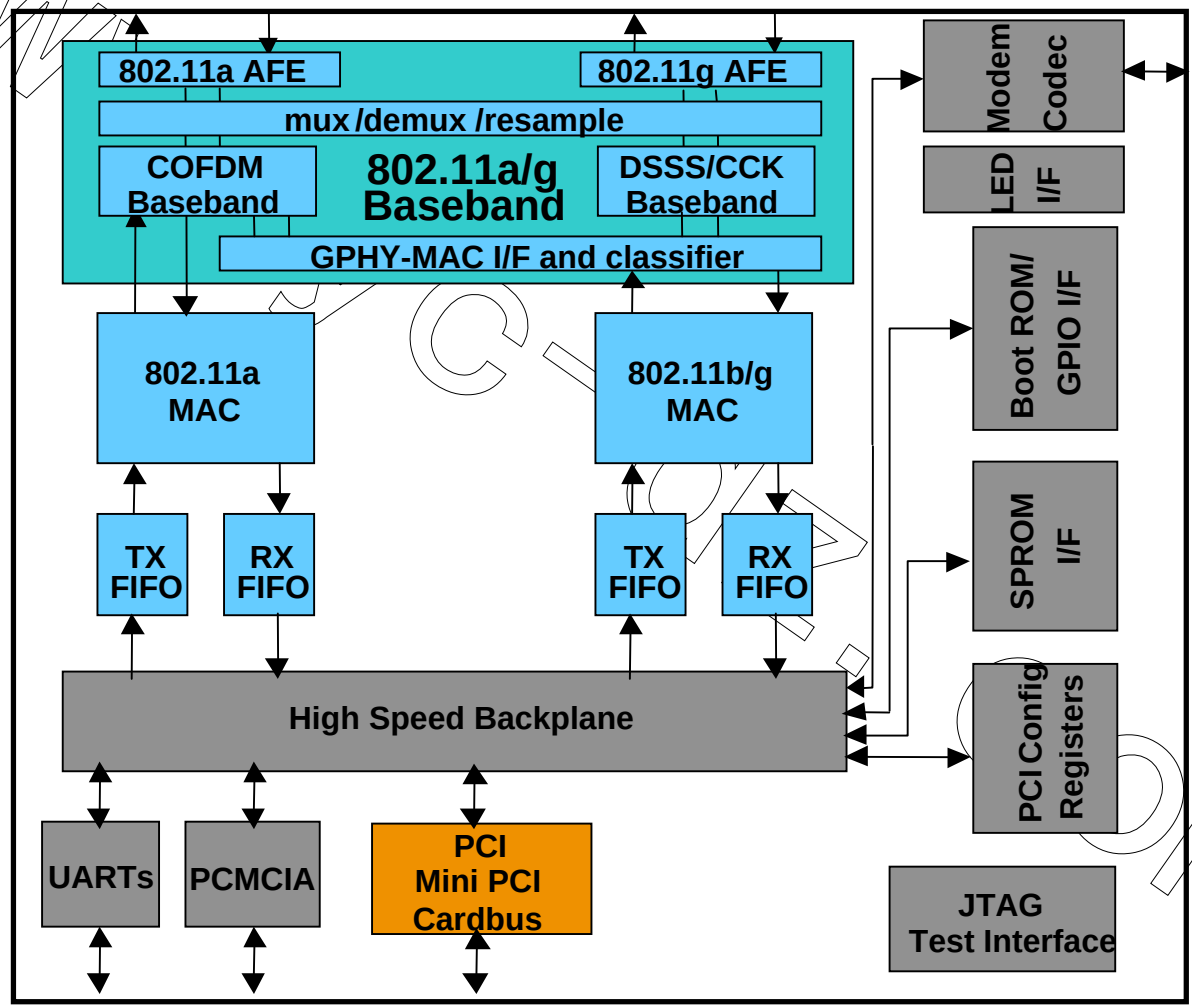
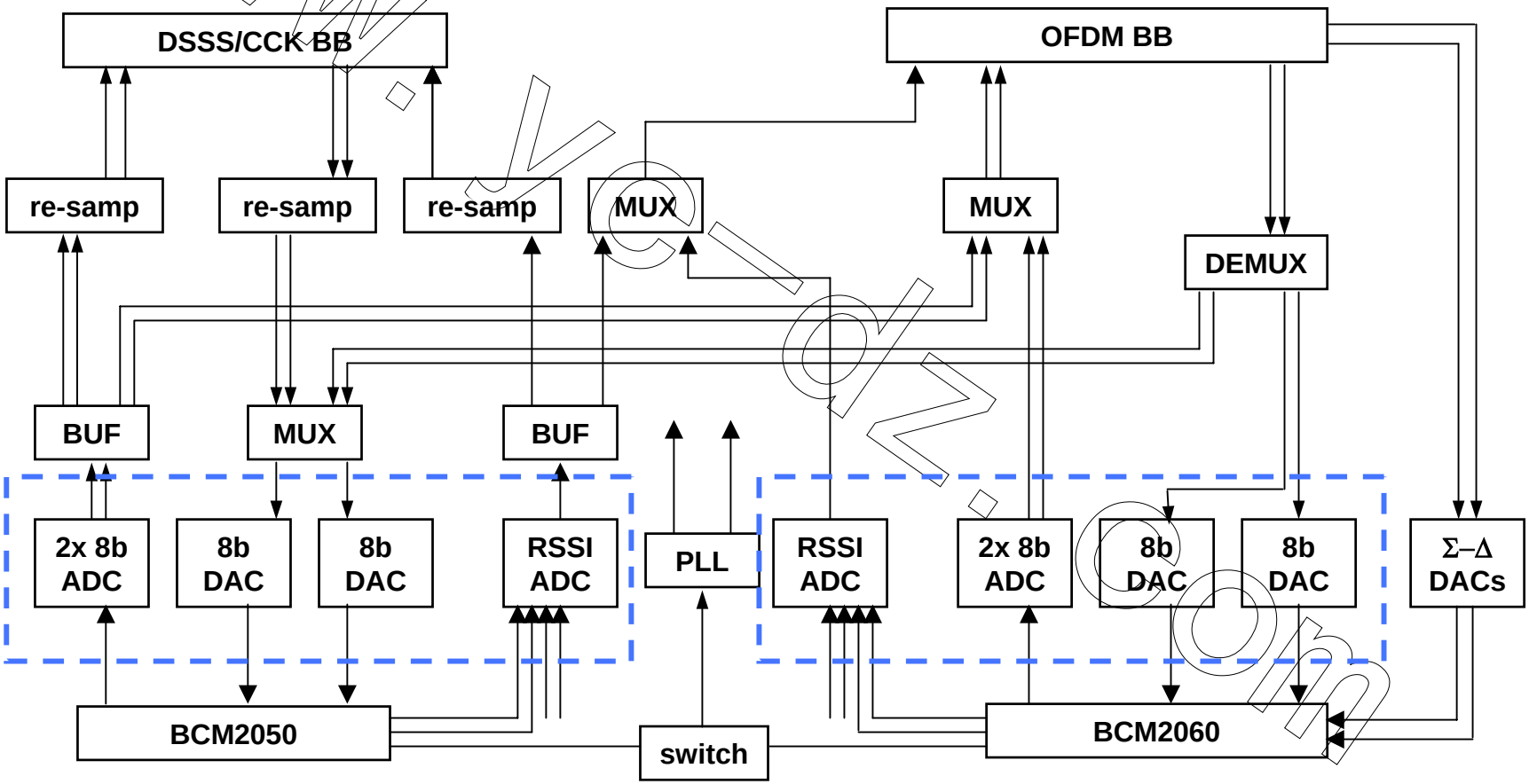
Baseband Block Diagram



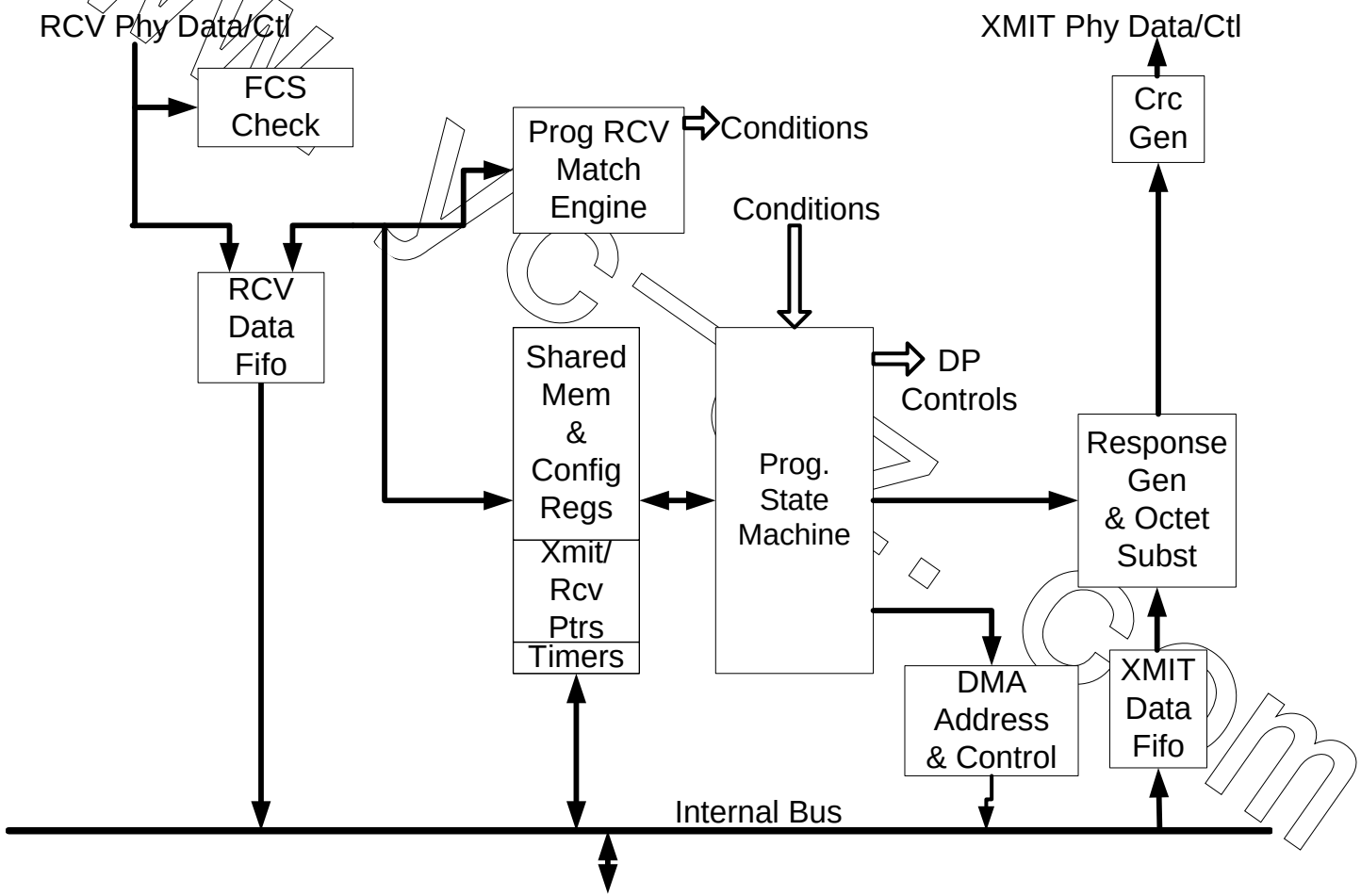
DSSS/CCK PHY

- Microcoded preamble processor computes equalizer coefficients on each received frame.
  - > 170 MMACs/sec.
- 11 Mbps r.m.s. delay spread tolerance > 200 nsec.

BCM4306/9 AFE Diagram



MAC Architecture



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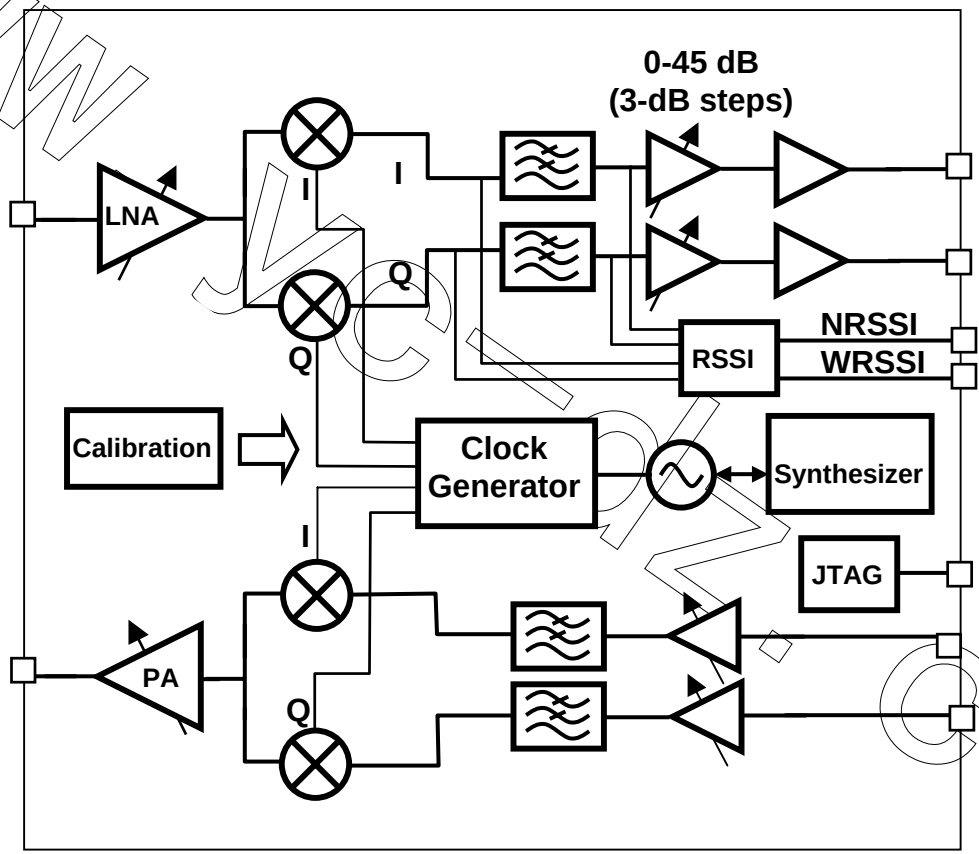
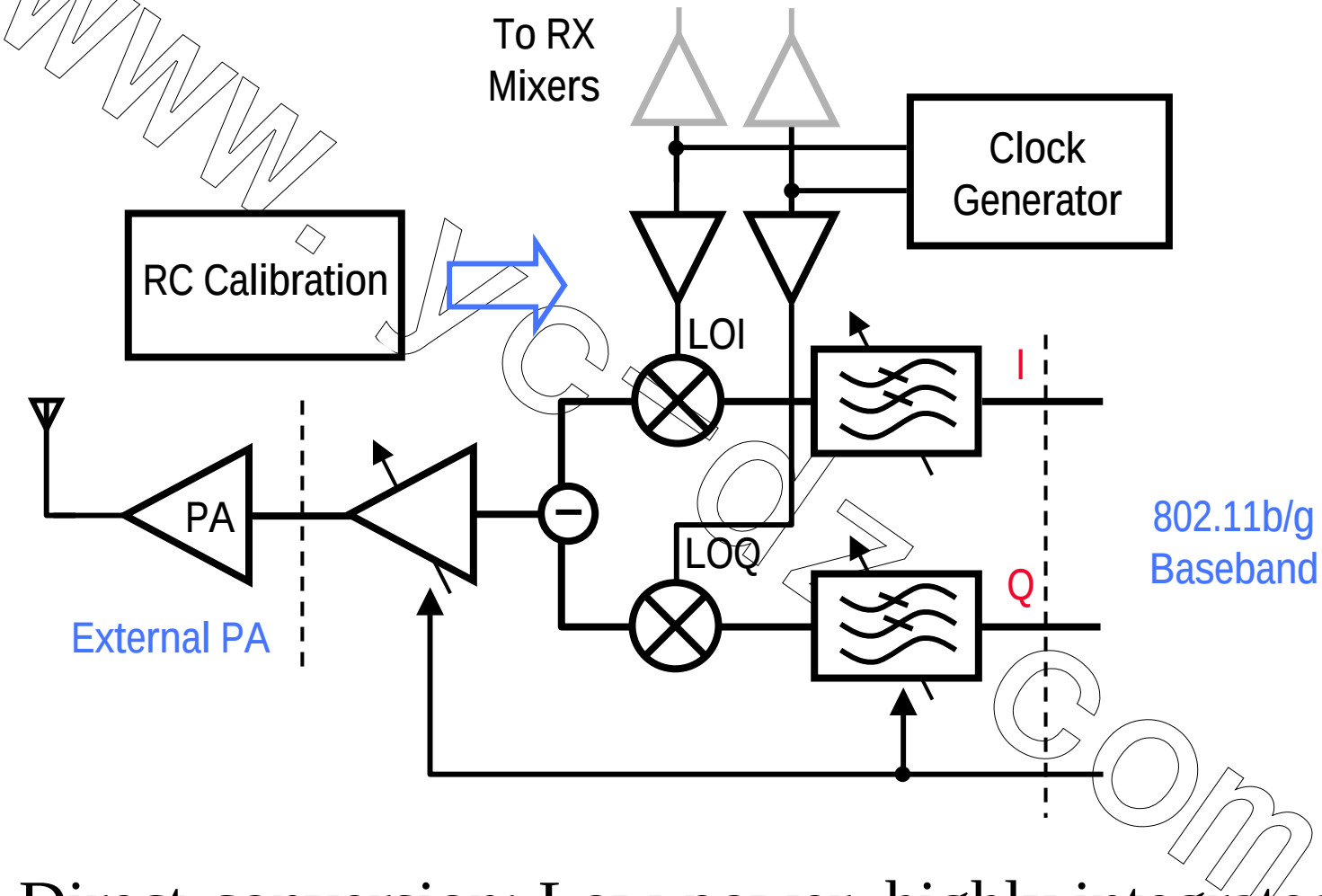
BCM2050 Block Diagram

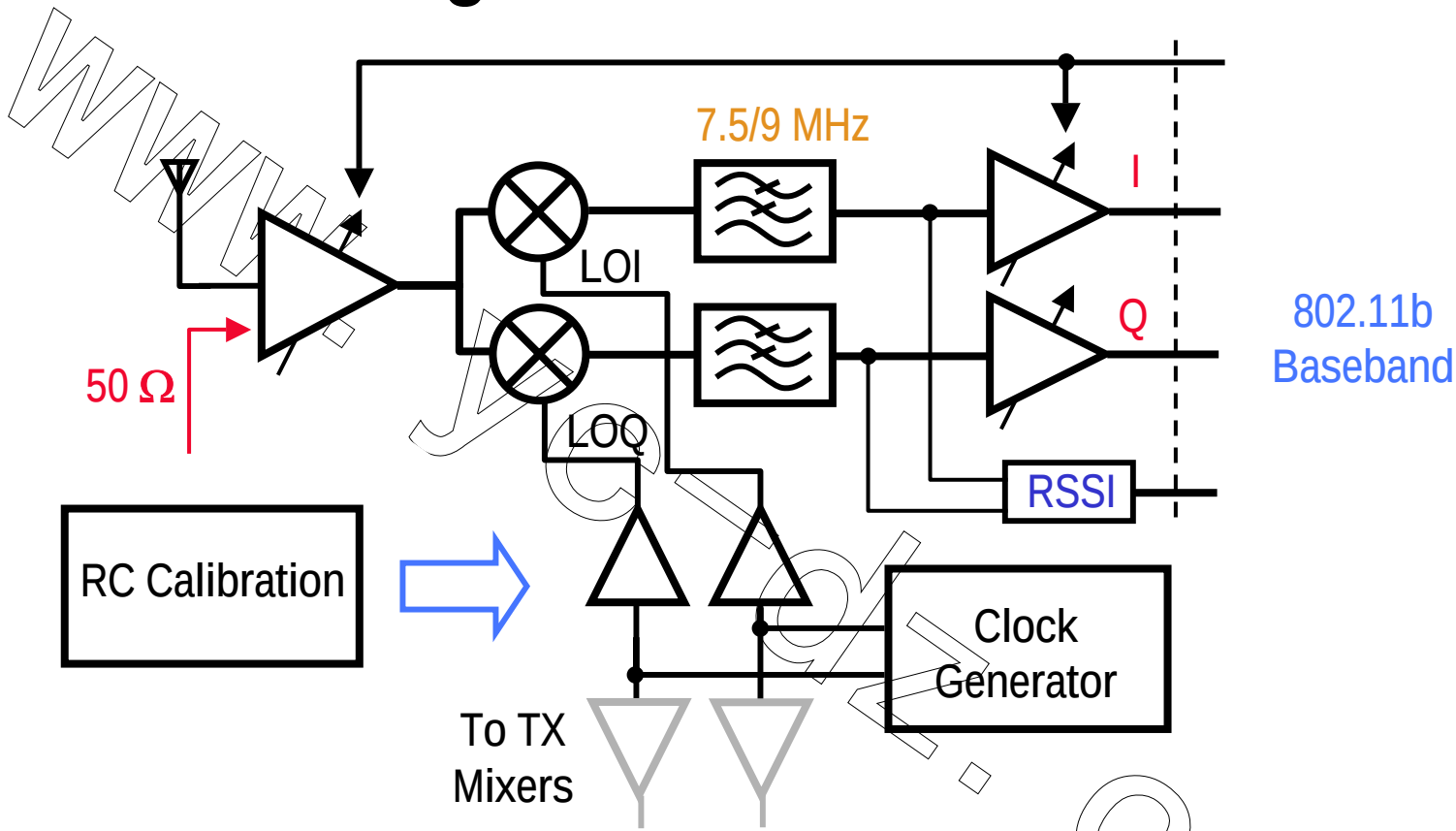


802.11b/g Transmitter Architecture



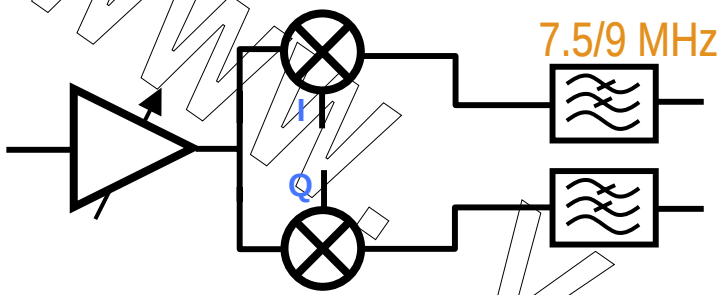
- Direct-conversion: Low-power, highly integrated

802.11b/g Receiver Architecture

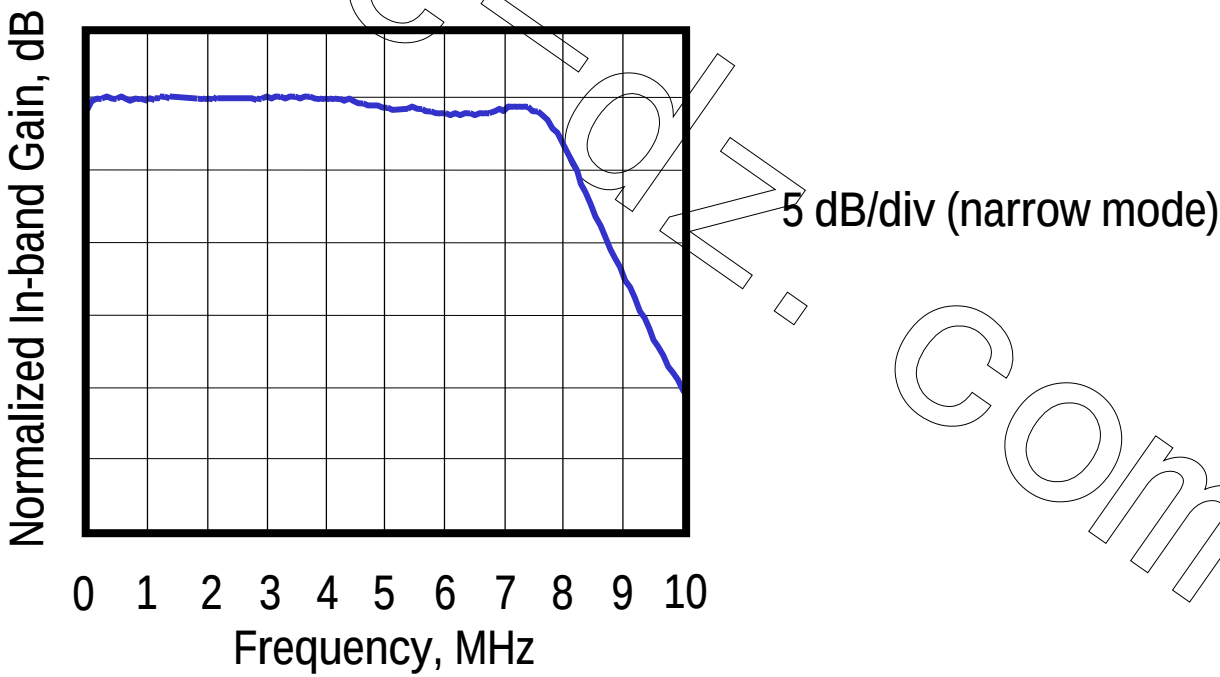


- Low-IF: Power-hungry IF filters
- Super-heterodyne: Off-chip IF filters
- Direct-conversion is the best

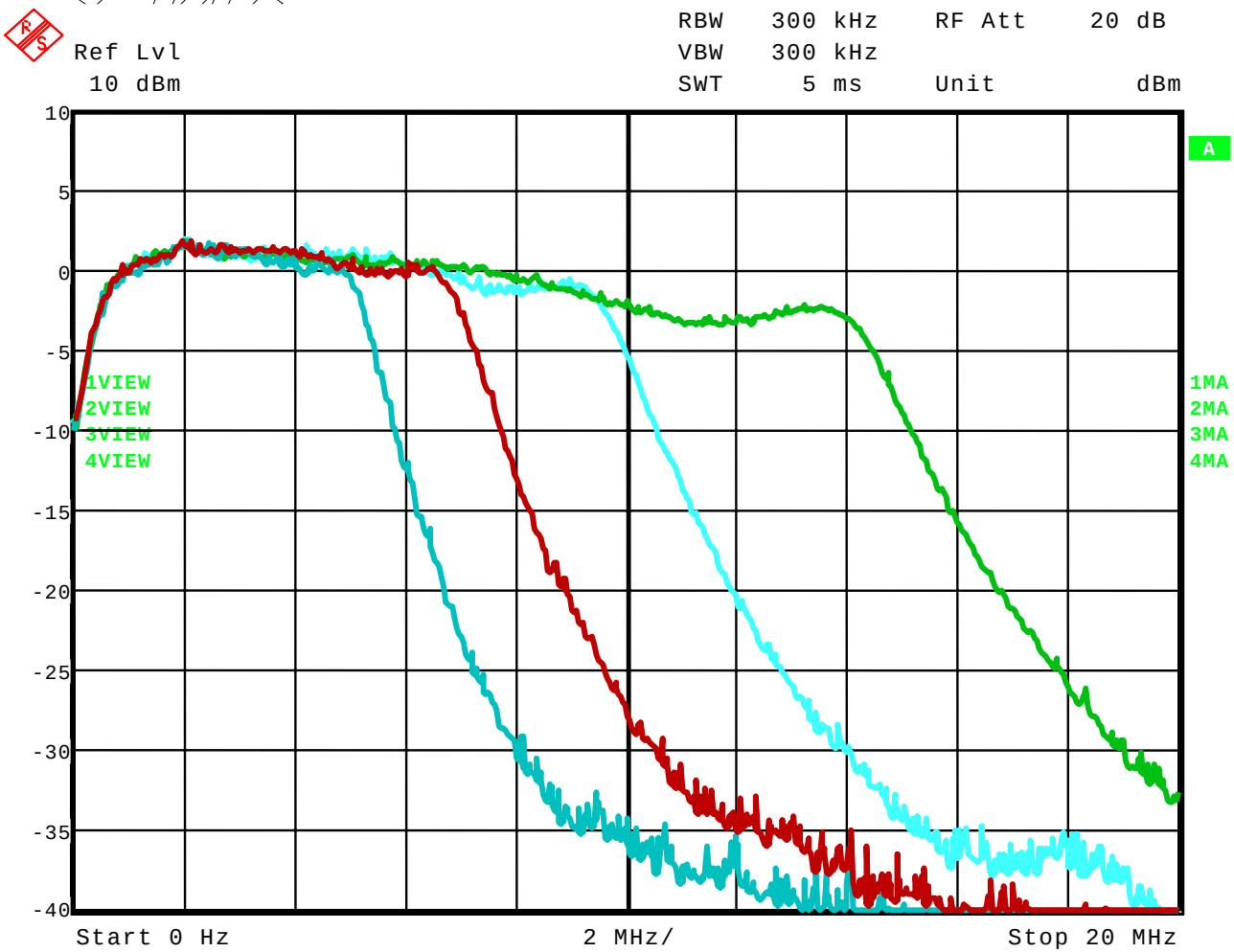
Receiver Front-End



- Common-source LNA
- Gilbert-type I/Q mixers
- Active RC filters
- S_{11}<-16 dB, IIP3=-8 dBm

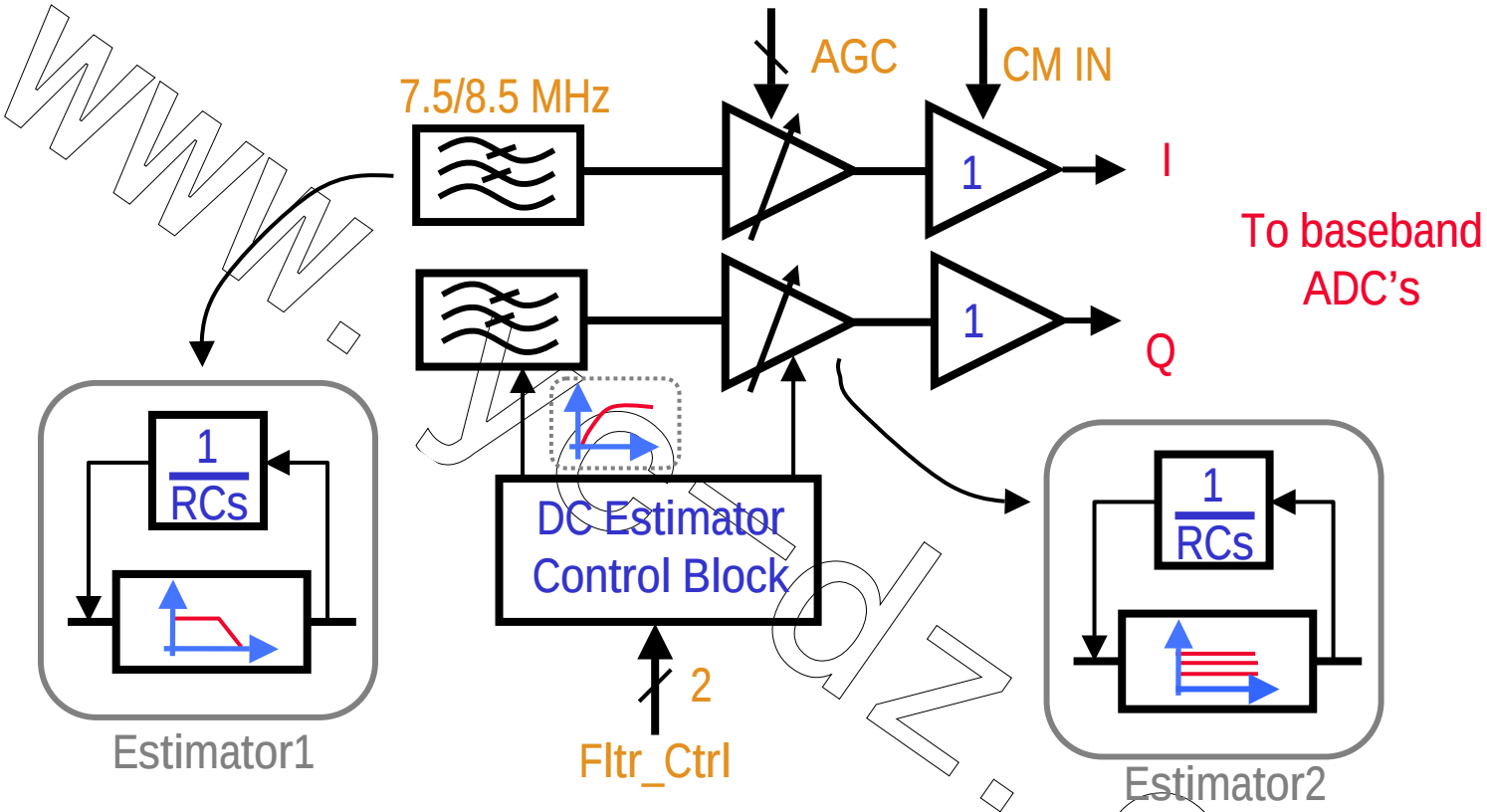


Programmable RX Filter



- RC 11111
- RC 11011
- Default 11b
- RC 00000

Receiver Baseband Section

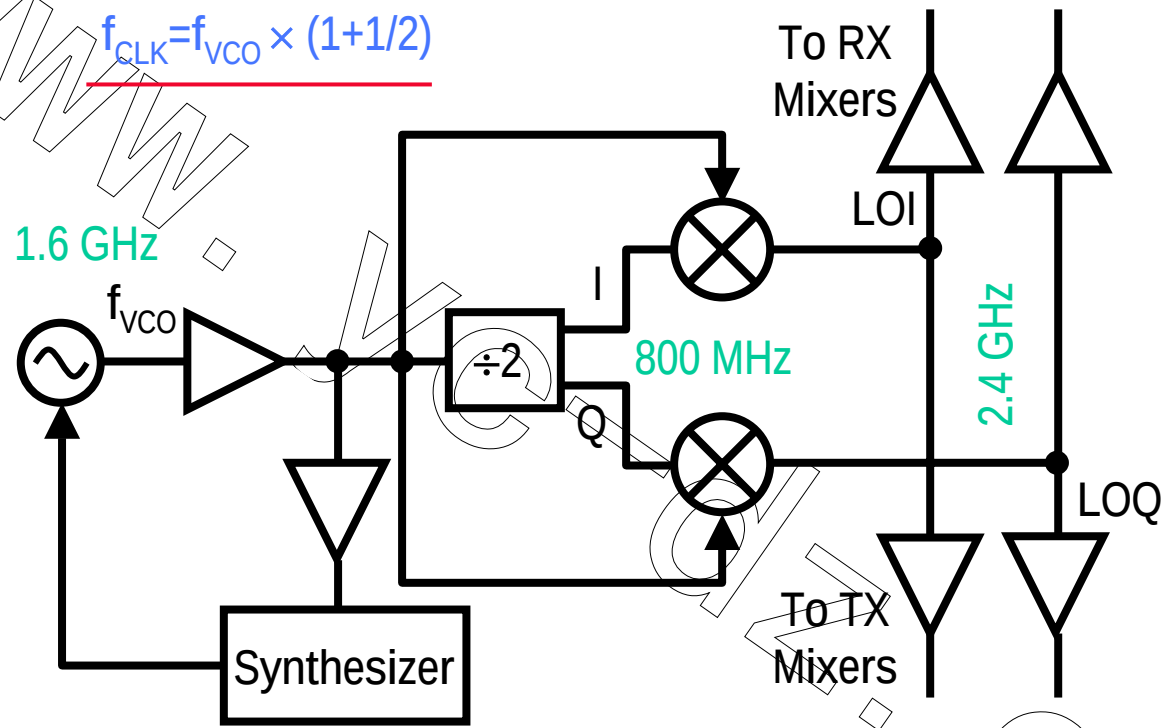


- **5th order Chebychev LPF with programmable bandwidth has sharp cut-off to attenuate interference**
- **Two independent offset cancellation loops for LPF and PGA**

Built-in Radio Calibration

- Built-in calibration ensures repeatability and consistency
  - Controls the effects of process variation to achieve the highest yield on a bulk CMOS process
  - Minimizes the effects of temperature variations during operation
- Calibrates all major blocks of the radio to within 2% of target
    - Filter phase and gain characteristics
    - Gain blocks and matching between major components
    - Center Frequency
  - Does not affect the normal operation and occurs in the normal Tx to Rx switching time – within 10 μsec.

Clock Generator Architecture



- Resolves PA pulling
- Spurs attenuated by on-chip LC filters

BCM2050 Specifications

Parameter	Value
NF	4 dB typ.
Receiver IIP3 (max. gain)	-16 dBm typ.
Receiver IIP3 (min. gain)	4 dBm typ.
Transmitter output power	5 dBm typ.
Transmitter OIP3	18 dBm
Transmitter output power range	5 dBm to -15 dBm typ.
Transmitter EVM	-27 dB min. at 54 Mbps
Receive-mode current consumption	110 mA typ. (1.8 V)
Transmit-mode current consumption	80 mA typ. (1.8 V)
Vdd	1.8 V

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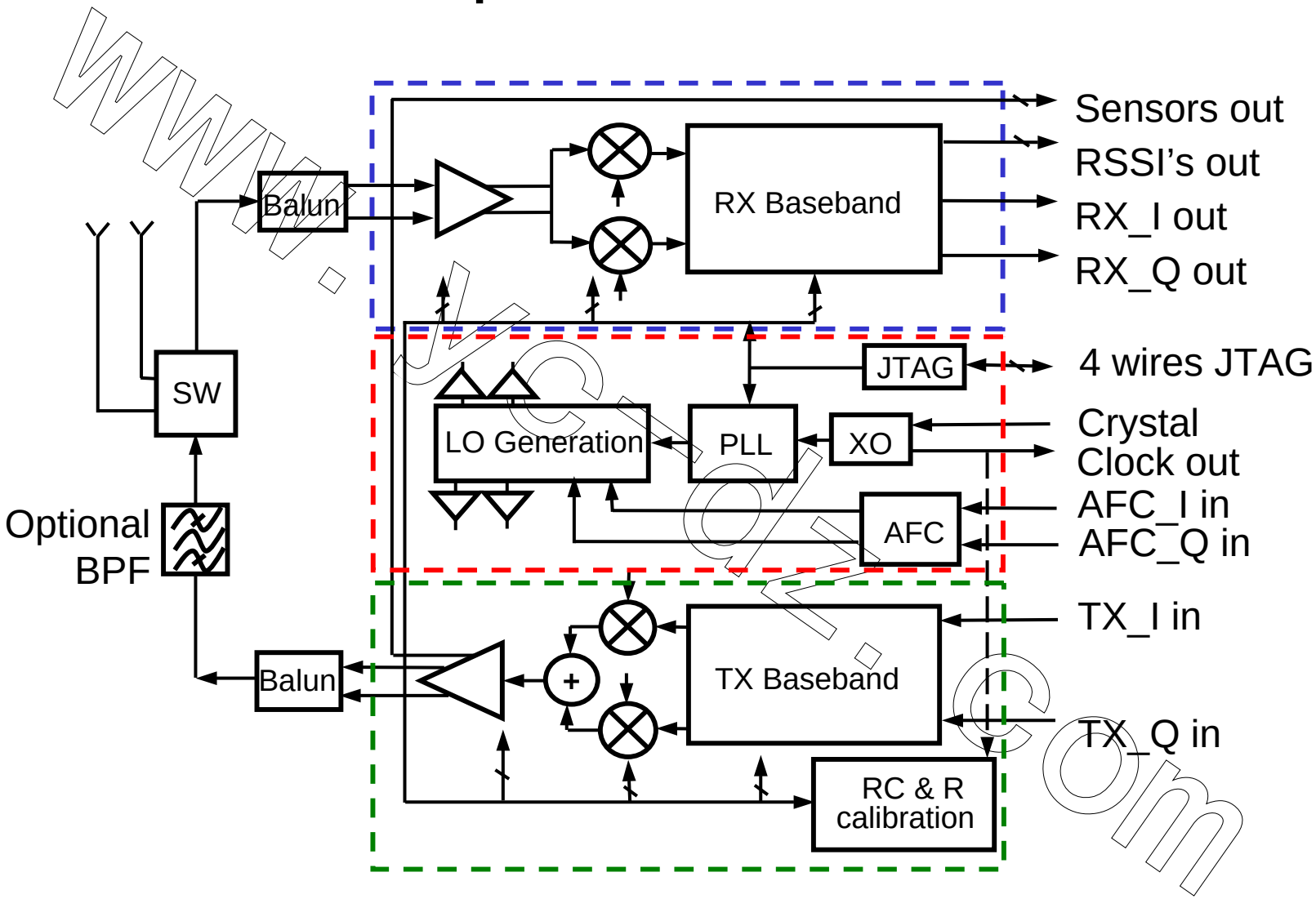
802.11a Radio Architecture

- Goal: Lowest Cost, Highest Performance, Lowest Power Consumption Radio
  - Direct Conversion Receiver and Transmitter Architecture
  - CMOS Implementation
  - Integrated PA
  - Take Advantage of Auto-Calibration Schemes

Implementation Challenges

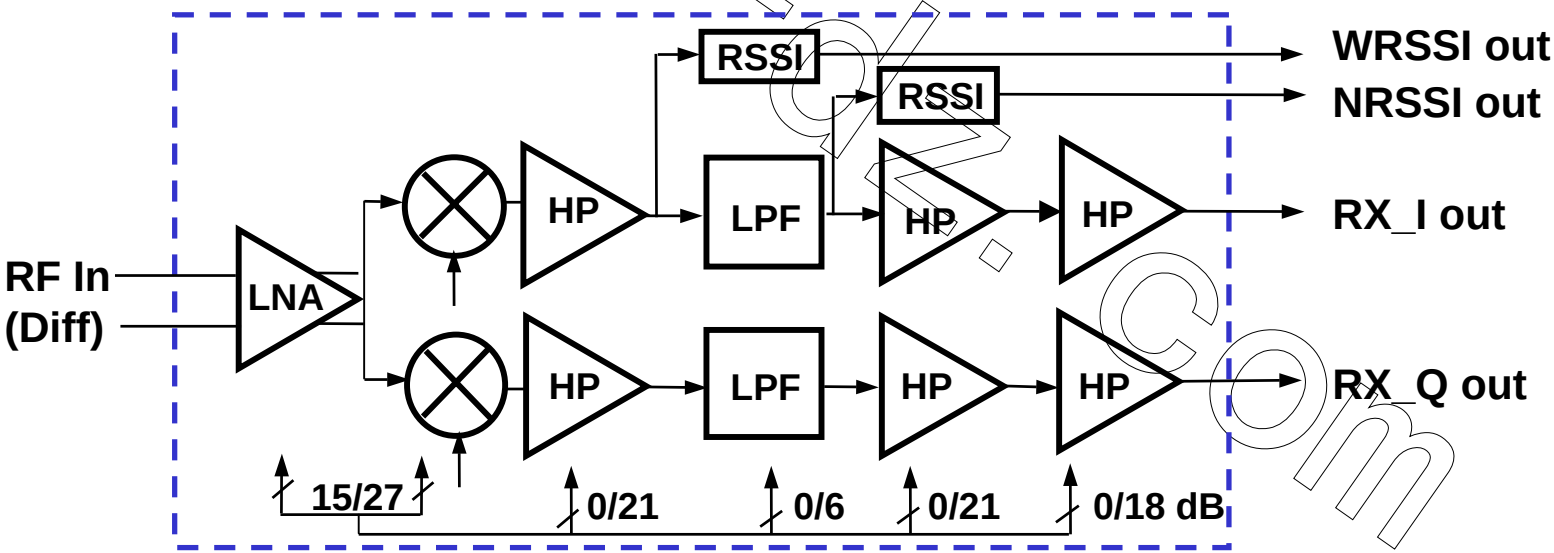
- Direct Conversion:
  - DC offsets
  - Flicker noise on receive path
  - Rx path and/or Tx path oscillations
  - Quadrature accuracy
  - LO pulling
  - LO feedthrough
- Integrated PA
  - High linearity requirements for PA
- Auto-Calibration
  - Automatic Carrier Frequency Control (AFC) Loop

BCM2060 Simplified Radio Architecture



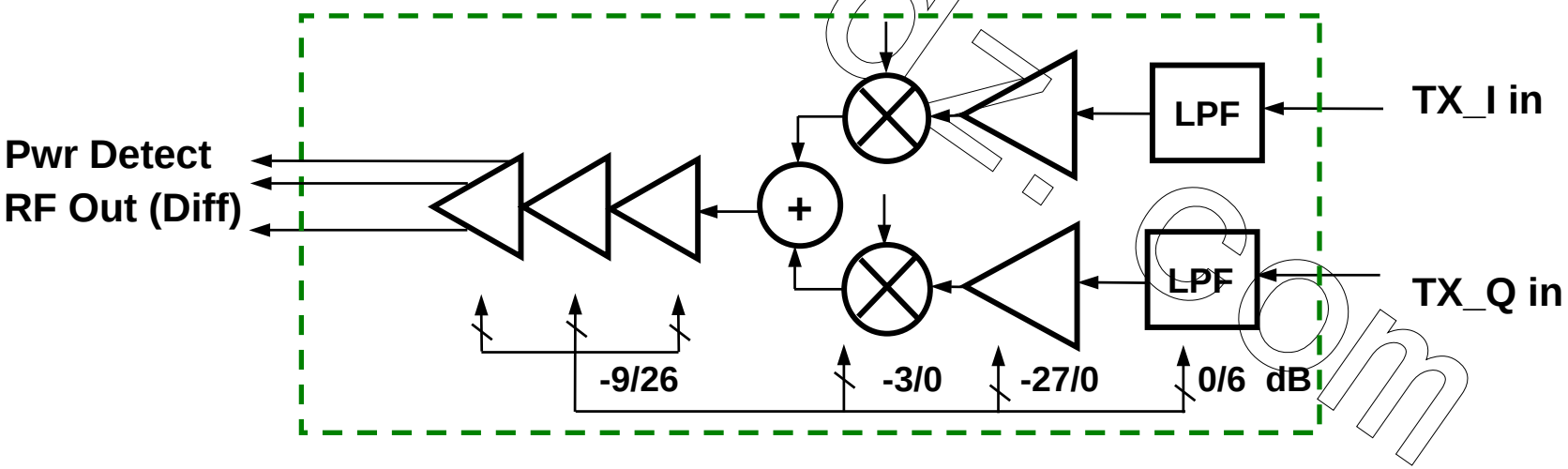
Receiver Description

- Full integration
- On-Chip LNA input matching
- High-gain, low-noise, high-linearity, gain controllable LNA/mixer
- 3 stages of high-pass VGA's
- A 5th-order Chebychev LPF
- Dual RSSI's
- System NF of 4dB and max gain of 93dB is achieved



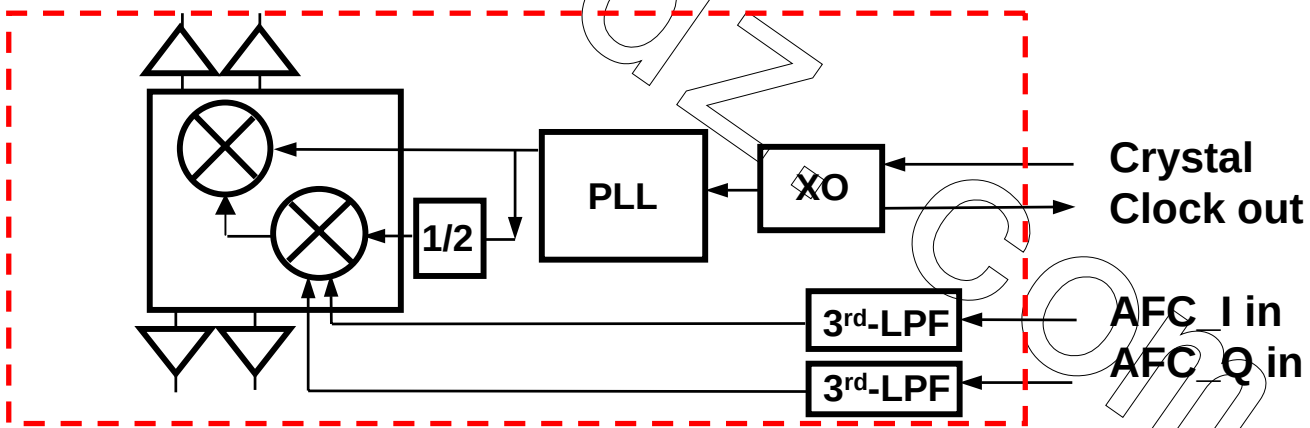
Transmitter Description

- Full integration
- 3rd-order Butterworth LPF's
- Baseband and RF VGA's
- High-linearity, high-power integrated class AB power amplifier
- On-chip power amplifier output matching
- TX P_{-1dB} of 19dBm and P_{sat} of 23dBm are achieved



PLL Description

- Full Integration
- Integer-N PLL with programmable loop bandwidth
- "Fractional-VCO"† with $f_{vco} = 2/3\ f_{rf}$
  - Reduces pulling from high-power on-chip PA
  - Reduces transmitter LO feed-through
  - Reduces receiver DC offsets due to self-mixing
- Automatic frequency control integrated into PLL
- PLL achieves PN of < -100dBc/Hz@30KHz offset with f_{rf} = 5.24 GHz

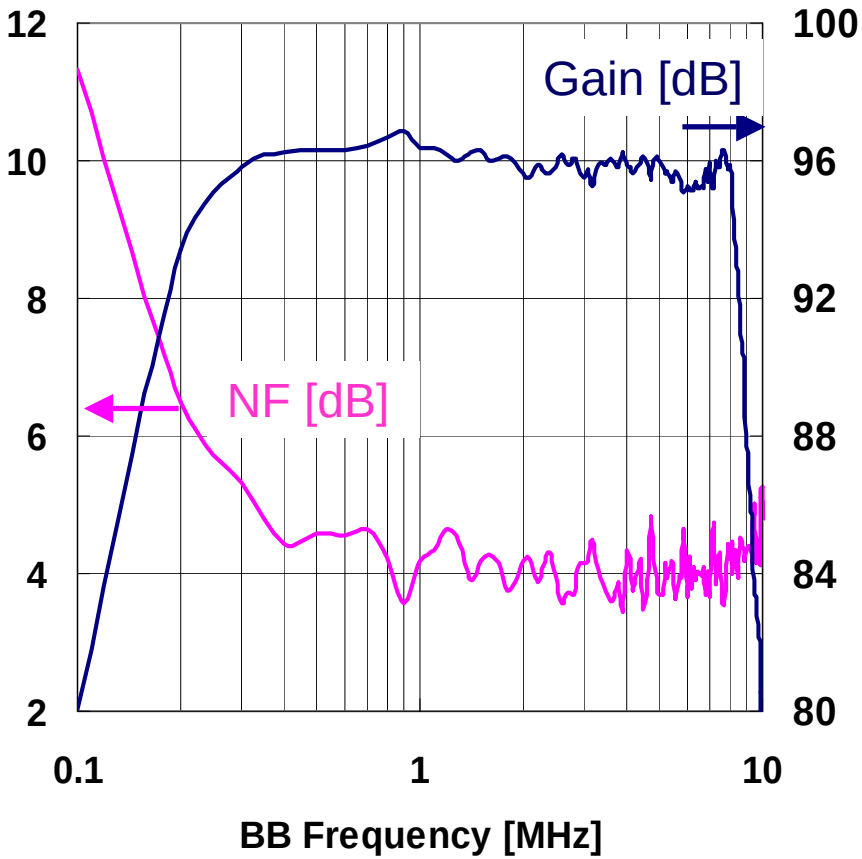


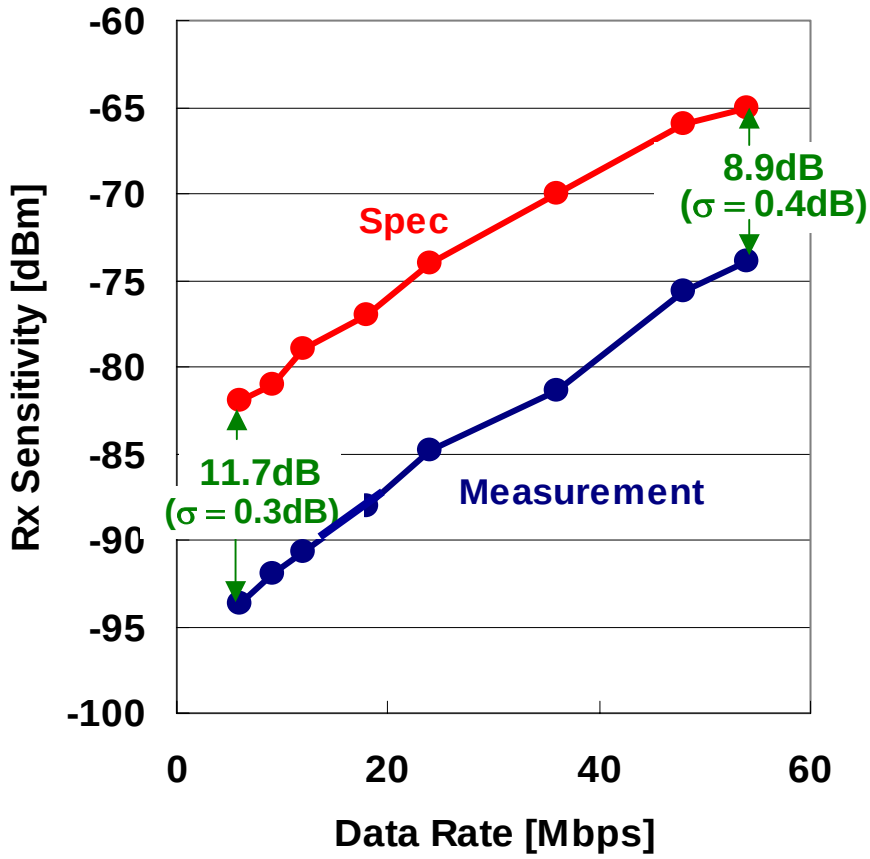
†H. Darabi, et. al., ISSCC 2001

Chip Level Auto-Calibration

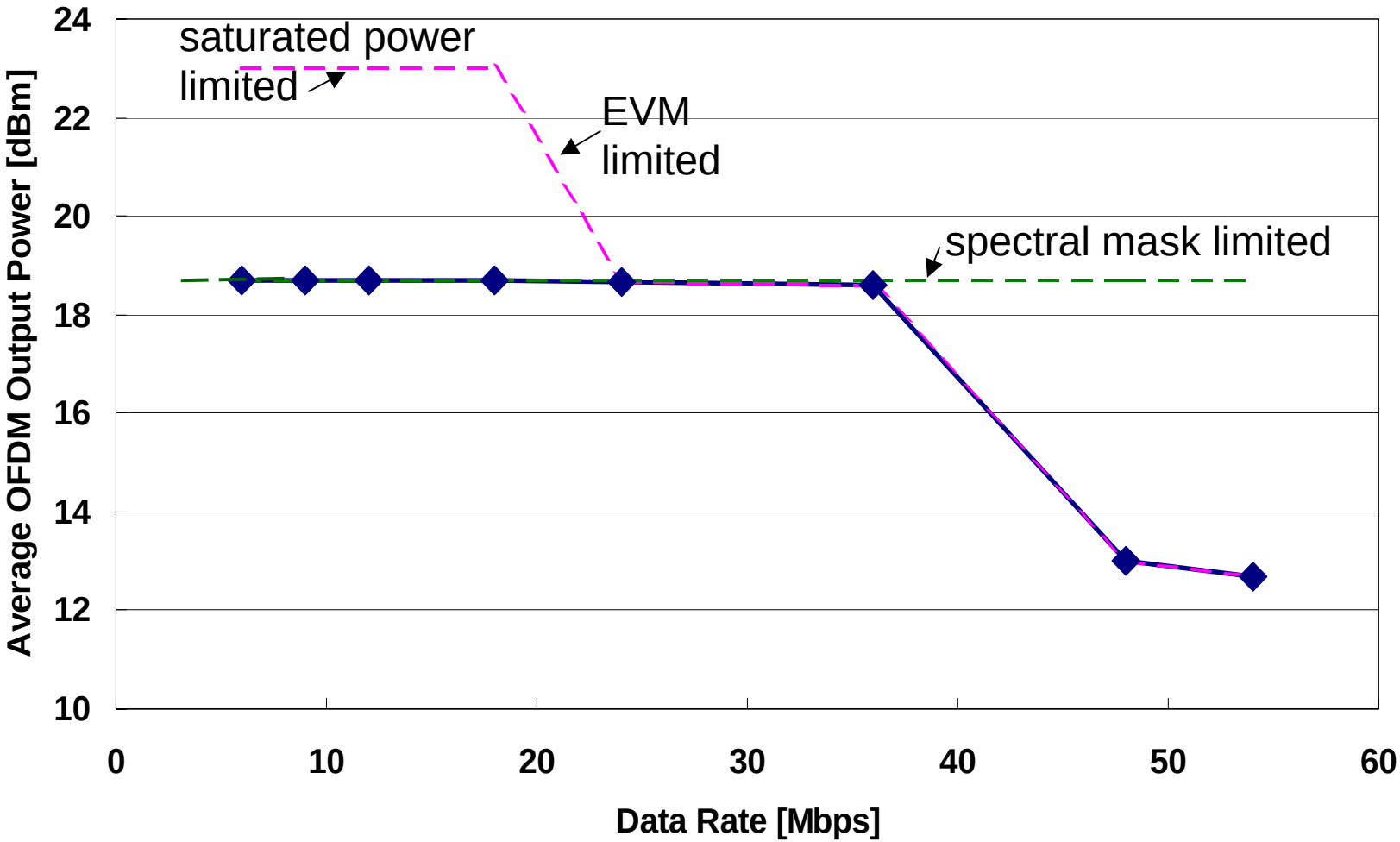
- VCO tuning
- AFC
- AFC self-calibration
- R-Calibration on bandgap blocks
- RC time constant calibration
- Integrated power detector
- Integrated temperature sensor
- Transmit LO feedthrough cancellation

Rx System NF and Sensitivity

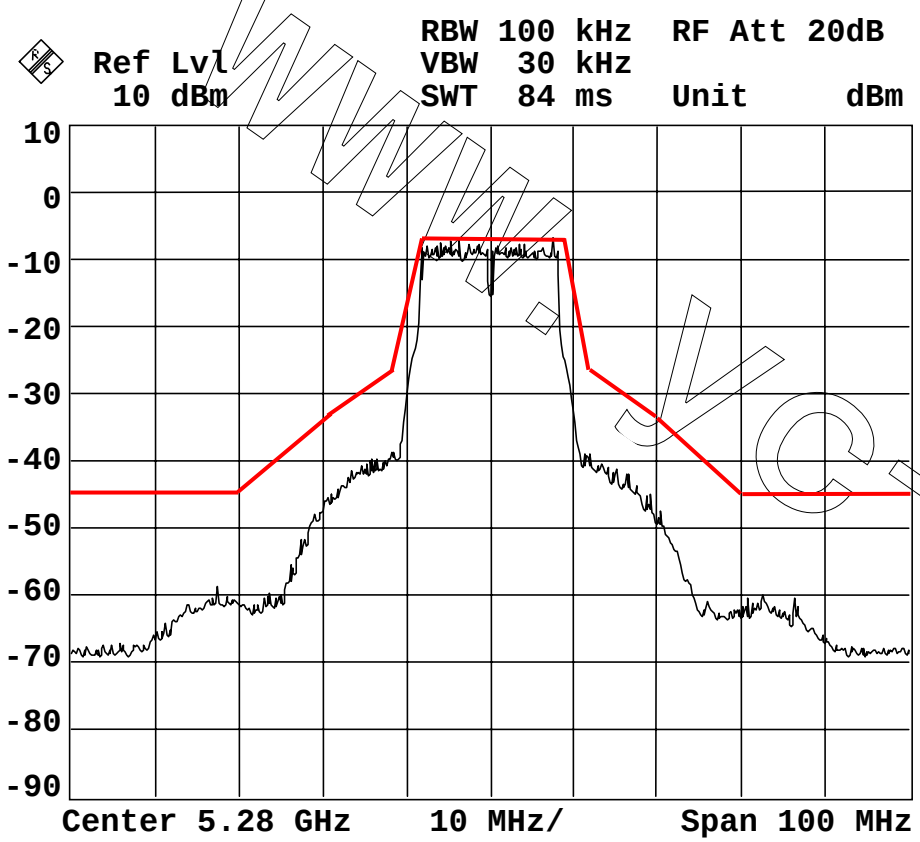




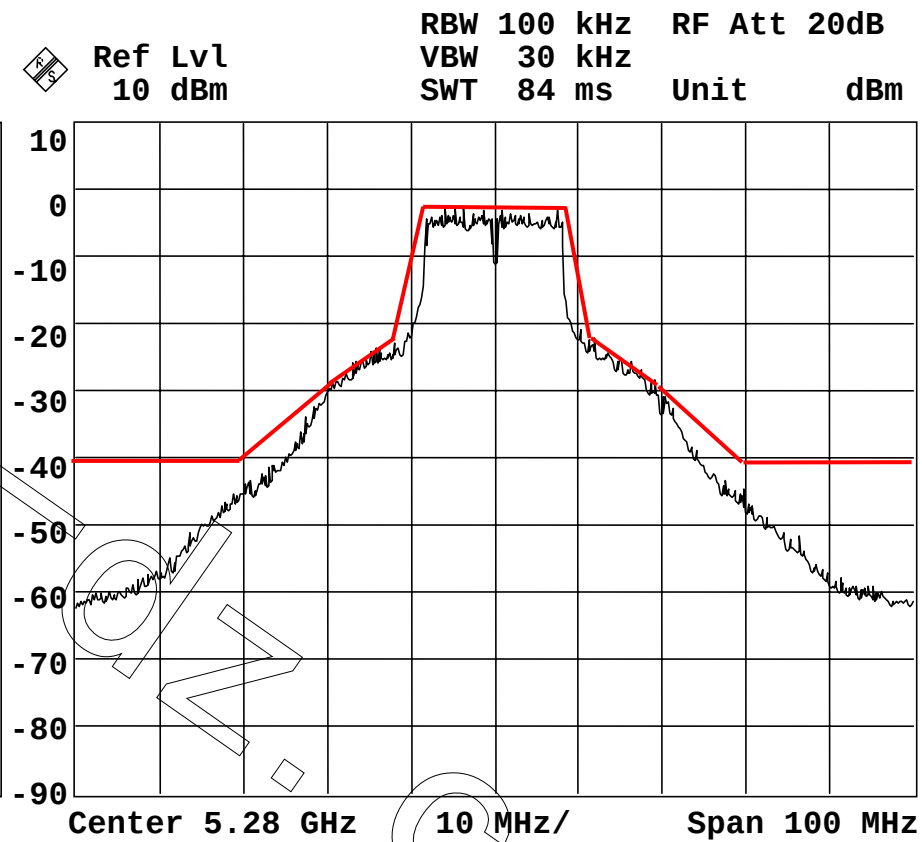
Measured Transmit Output Power



Measured TX Power Spectrum



12.8dBm, 54Mbps, QAM64
(EVM Limited)

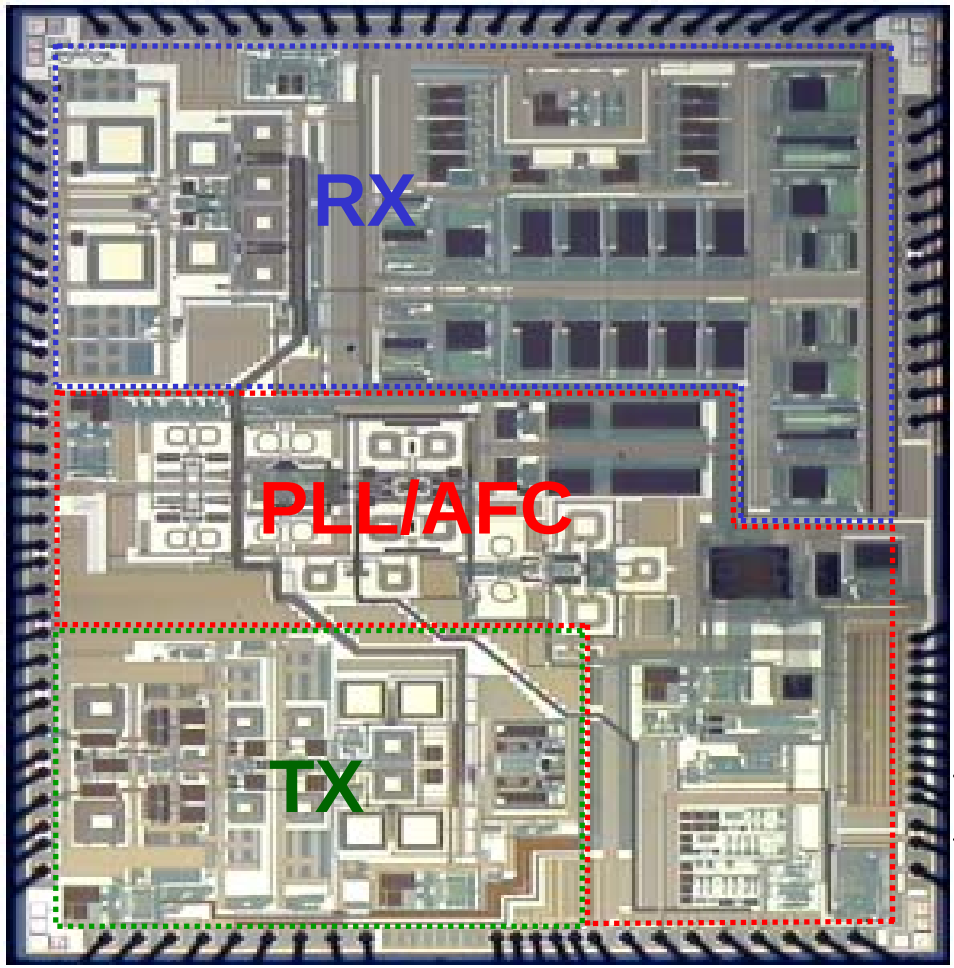


18.7dBm, 36Mbps, QAM16
(Spectral Mask Limited)

Summary of Transceiver Performance

	Measured (this paper)	*Unit*
Frequency Band	**5.15 – 5.35**	**GHz**
RX NF	**4**	**dB**
RX Sensitivity (6Mbps)	**-93.7 ± 0.9**	**dBm**
RX Sensitivity (54Mbps)	**-73.9 ± 1.2**	**dBm**
RX IIP3	**-4.8**	**dBm**
RX IIP2	**> 30**	**dBm**
RX Gain Range	**15 to 93**	**dB**
TX Power Range	**-30 to +18.7**	**dBm**
TX Psat	**+23**	**dBm**
TX P-1dB	**+19**	**dBm**
Vdd	**1.8**	**V**
Vdd_PA	**3.3**	**V**
Phase Noise @ 30KHz	**-100**	**dBc/Hz**
RX Power Consumption	**150**	**mW**
TX Power Consumption	**380 (15dBm OFDM output)**	**mW**
ESD	**> ±2.5 on all pins**	**KV**
Technology	**0.18um 1P5M CMOS**	
Die Size	**11.7 (including padring)**	**mm^2**

Die Microphotograph of BCM2060



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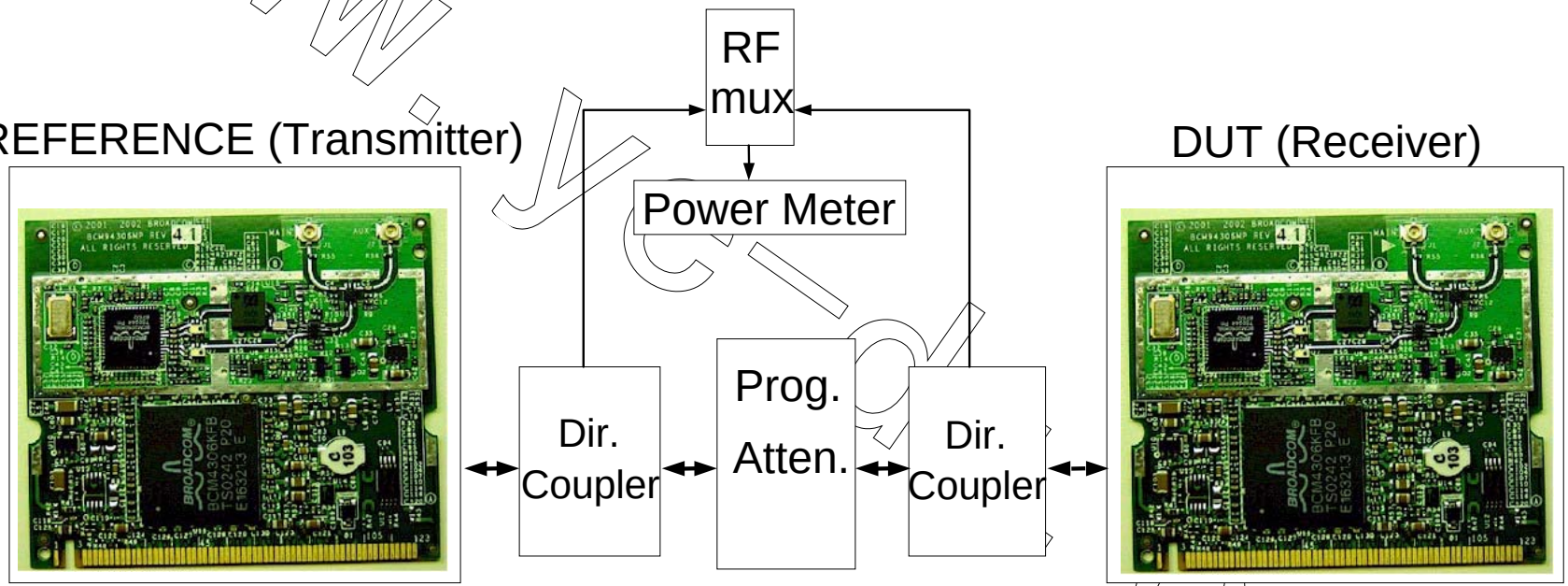
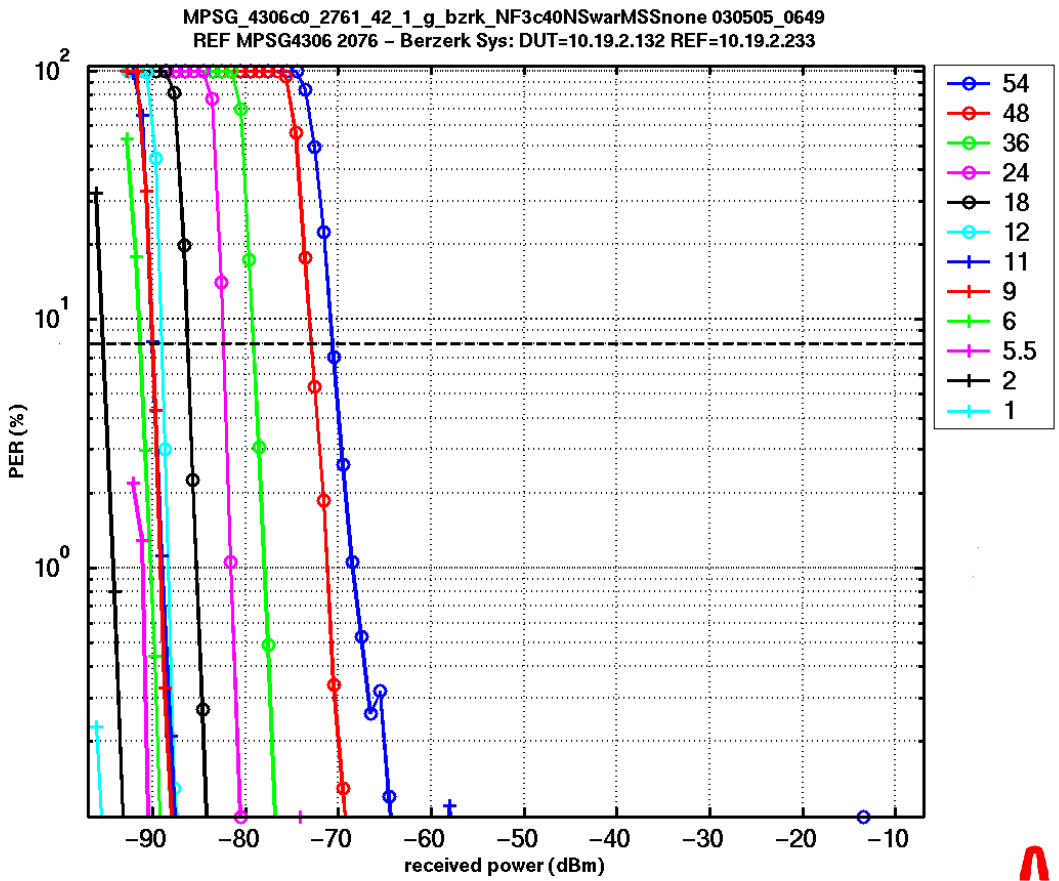
Flat-Channel Sensitivity Test Diagram



802.11g System Sensitivity Test Result

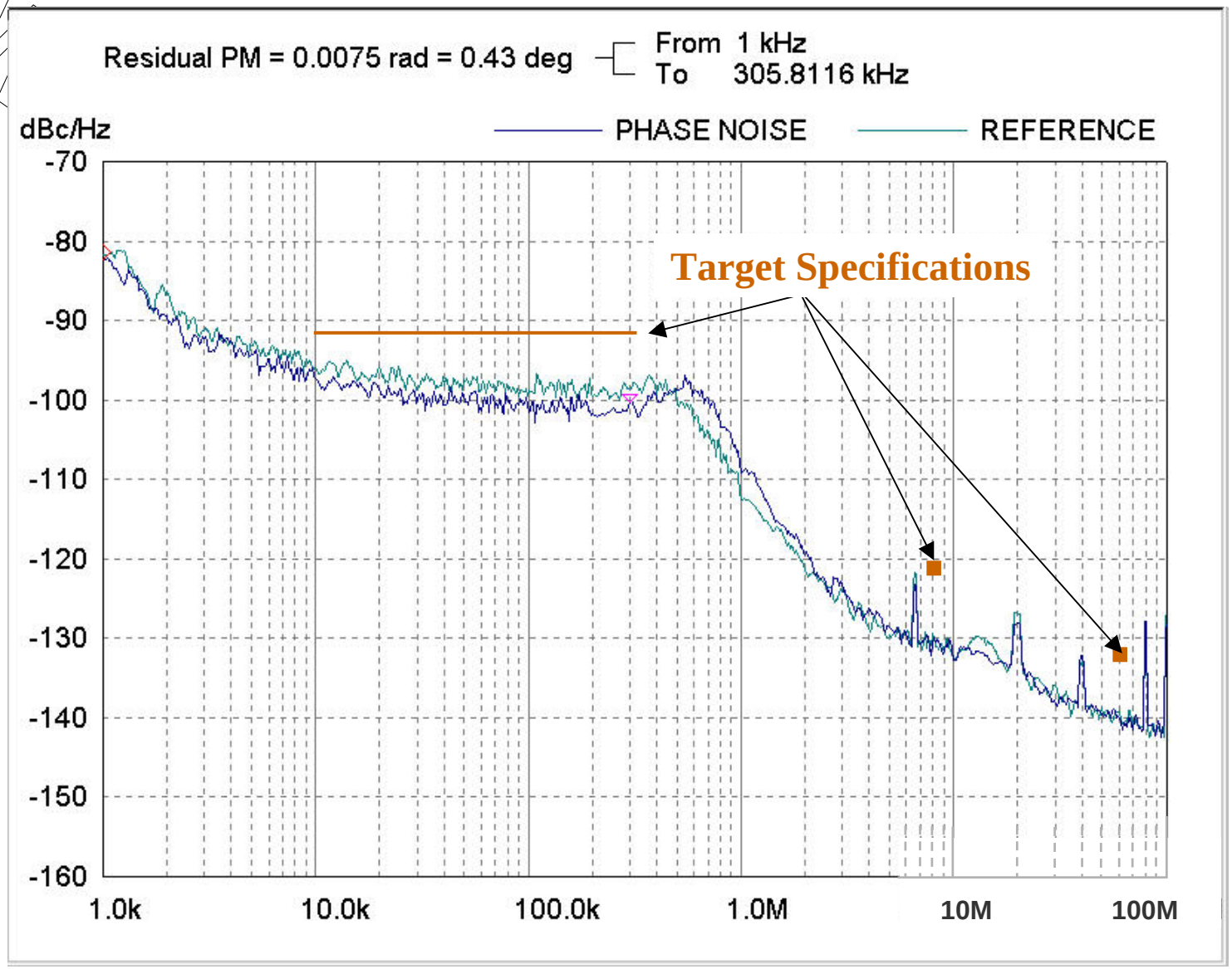


1 Mbps sensitivity
-97 dBm

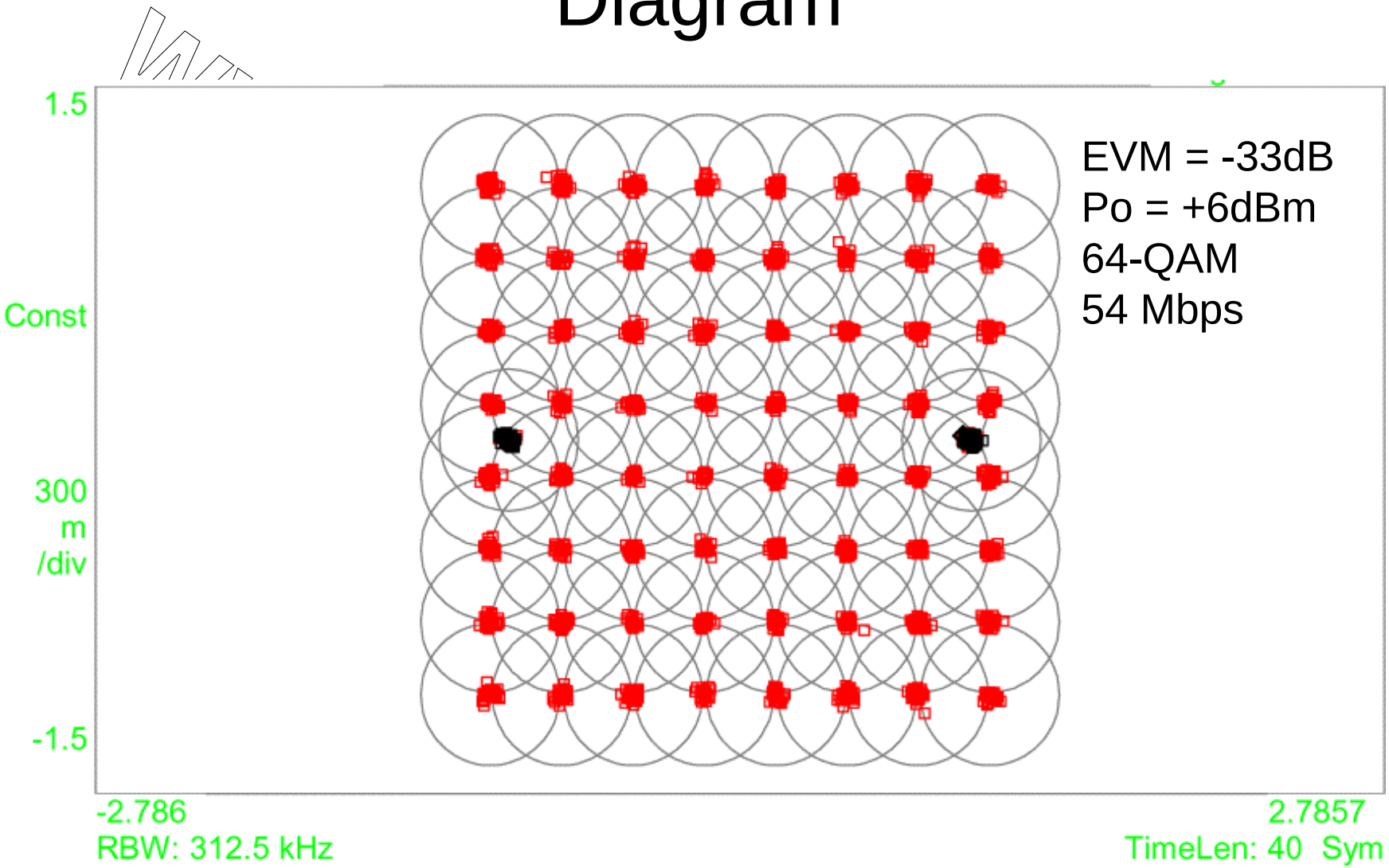
54 Mbps sensitivity
< -70 dBm

Results include all PCB and connector losses.

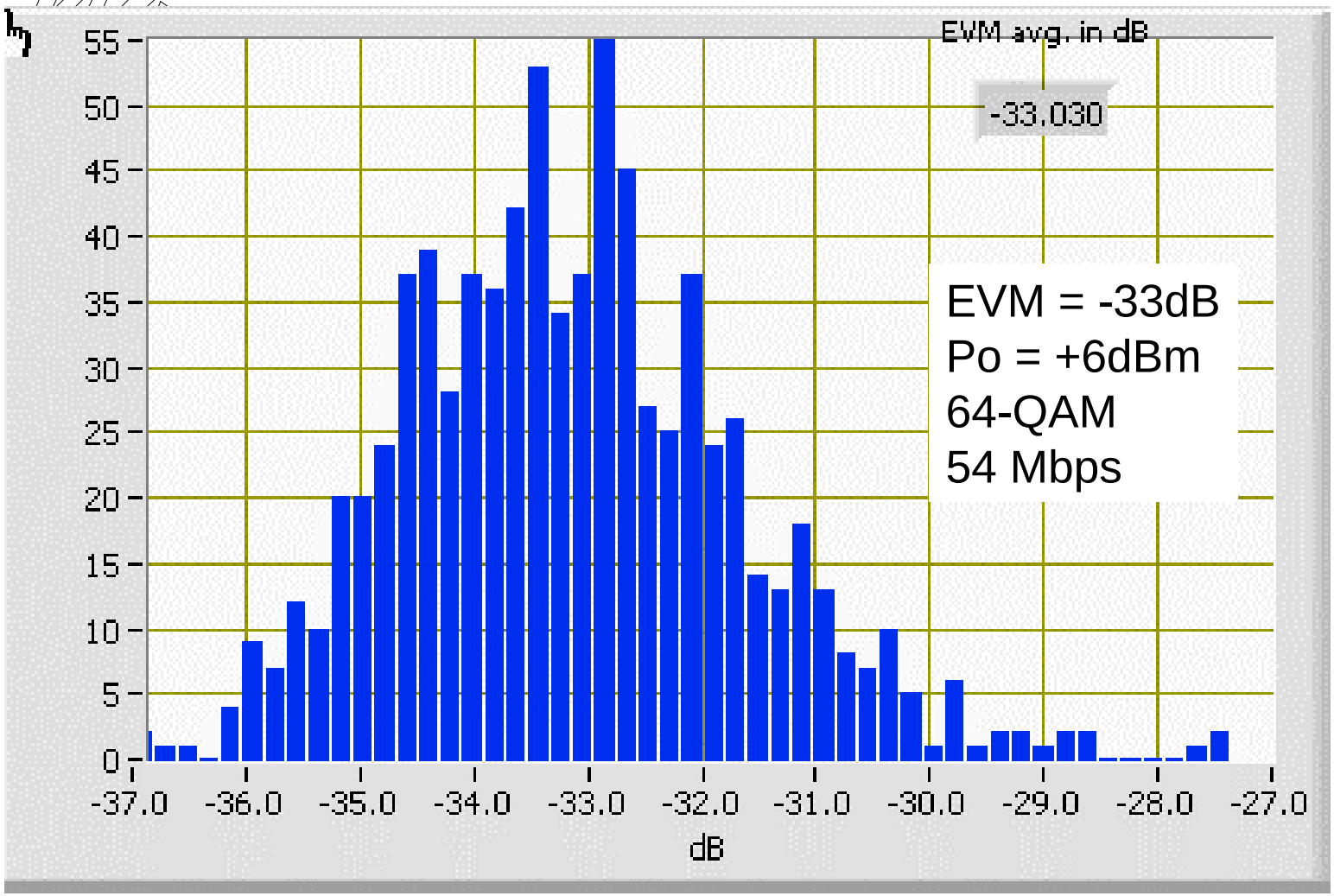
Measured BCM2060 Phase Noise



Measured 802.11a TX Constellation Diagram



Measured 802.11a TX EVM Histogram



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Conclusions

- Highest Performance, Highest Integration, Smallest Size, Lowest Power Consumption IEEE 802.11g Transceiver Reported to Date
  - 4 dB Rx chain noise figure
  - Excellent performance in the presence of real-world impairments
  - Fully integrated, direct conversion
  - Various integrated self contained or system level calibration capabilities for high yield and tight tolerances
  - 790 mW transmit or receive (1.8 V), RF and baseband/MAC
  - 10 mW sleep mode, RF and baseband/MAC
  - 802.11g receiver sensitivity with all board losses
    - -70 dBm 54 Mbps
    - -97 dBm 1 Mbps

Conclusions

- Highest Performance, Highest Integration, Smallest Size, Lowest Power Consumption IEEE 802.11a Transceiver Reported to Date
  - 4 dB Rx chain noise figure
  - 23 dBm Tx P_{sat} with integrated PA
  - Excellent performance in the presence of real-world impairments
  - Fully integrated, direct conversion
  - Integrated or system level calibration capabilities for high yield and consistent performance

Acknowledgements

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