Broadcom WLAN Chipset for 802.11a/b/g

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Broadcom Corporation, CA, USA
Outline

• Transceiver Architecture
  – Baseband IC (BCM4306)
  – .11g RFIC (BCM2050)
  – .11a RFIC (BCM2060)

• System Measurement Results

• Conclusion
Dual Band Overall Block Diagram

- BCM2050 Radio
- BCM2060 Radio
- BCM4309 MAC & BB

Key Components:
- Power Amp
- T/R Switch
- Diversity Switch
- LPF or BPF
- Balun
- Crystal
- System Interface

(All components are connected as per the diagram, showing the flow of signals and interconnections.)
Single-band MiniPCI Card

BCM2050

BCM4306
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Baseband Block Diagram

Diagram showing the block diagram of a baseband module with various components such as:

- 802.11a AFE
- 802.11g AFE
- COFDM Baseband
- 802.11a/g Baseband
- DSSS/CCK Baseband
- GPHY-MAC I/F and classifier
- 802.11a MAC
- 802.11b/g MAC
- TX FIFO
- RX FIFO
- High Speed Backplane
- UARTs
- PCMCIA
- PCI Mini PCI Cardbus
- PCI Config Registers
- UARTs
- LED I/F
- Boot ROM/GPIO I/F
- SPROM I/F
- JTAG Test Interface
DSSS/CCK PHY

• Microcoded preamble processor computes equalizer coefficients on each received frame.
  – > 170 MMACs/sec.
• 11 Mbps r.m.s. delay spread tolerance > 200 nsec.
MAC Architecture

Diagram showing the flow of data and control signals in a MAC (Media Access Control) architecture. Key components include:
- RCV Phy Data/Ctl
- FCS Check
- RCV Data Fifo
- Prog RCV Match Engine
- Conditions
- Shared Mem & Config Regs
- Xmit/Rcv Ptrs
- Timers
- Prog. State Machine
- Conditions
- DP Controls
- Response Gen & Octet Subst
- DMA Address & Control
- XMIT Data Fifo
- XMIT Phy Data/Ctl
- Crc Gen
- Internal Bus

The diagram illustrates the complex interactions and processing steps involved in managing data and control signals in a MAC architecture.
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BCM2050 Block Diagram

- LNA
- Calibration
- Clock Generator
- Synthesizer
- PA
- 0-45 dB (3-dB steps)
- RSSI
- NRSSI
- WRSSI
- JTAG

www.yc-dz.com
• Direct-conversion: Low-power, highly integrated
802.11b/g Receiver Architecture

- Low-IF: Power-hungry IF filters
- Super-heterodyne: Off-chip IF filters
- Direct-conversion is the best
Receiver Front-End

- Common-source LNA
- Gilbert-type I/Q mixers
- Active RC filters
- $S_{11}<-16$ dB, IIP3=-8 dBm

![Diagram of Receiver Front-End](image)

**Normalized In-band Gain, dB**

5 dB/div (narrow mode)
Programmable RX Filter

Ref Lvl
10 dBm

RC 11111
RC 11011
Default 11b
RC 00000
• 5th order Chebychev LPF with programmable bandwidth has sharp cut-off to attenuate interference

• Two independent offset cancellation loops for LPF and PGA
Built-in Radio Calibration

- Built-in calibration ensures repeatability and consistency
  - Controls the effects of process variation to achieve the highest yield on a bulk CMOS process
  - Minimizes the effects of temperature variations during operation
- Calibrates all major blocks of the radio to within 2% of target
  - Filter phase and gain characteristics
  - Gain blocks and matching between major components
  - Center Frequency
  - Does not affect the normal operation and occurs in the normal Tx to Rx switching time – within 10 µsec.
Clock Generator Architecture

- Resolves PA pulling
- Spurs attenuated by on-chip LC filters
BCM2050 Specifications

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>NF</td>
<td>4 dB typ.</td>
</tr>
<tr>
<td>Receiver IIP3 (max. gain)</td>
<td>-16 dBm typ.</td>
</tr>
<tr>
<td>Receiver IIP3 (min. gain)</td>
<td>4 dBm typ.</td>
</tr>
<tr>
<td>Transmitter output power</td>
<td>5 dBm typ.</td>
</tr>
<tr>
<td>Transmitter OIP3</td>
<td>18 dBm</td>
</tr>
<tr>
<td>Transmitter output power range</td>
<td>5 dBm to -15 dBm typ.</td>
</tr>
<tr>
<td>Transmitter EVM</td>
<td>-27 dB min. at 54 Mbps</td>
</tr>
<tr>
<td>Receive-mode current consumption</td>
<td>110 mA typ. (1.8 V)</td>
</tr>
<tr>
<td>Transmit-mode current consumption</td>
<td>80 mA typ. (1.8 V)</td>
</tr>
<tr>
<td>Vdd</td>
<td>1.8 V</td>
</tr>
</tbody>
</table>
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802.11a Radio Architecture

- Goal: Lowest Cost, Highest Performance, Lowest Power Consumption Radio
  - Direct Conversion Receiver and Transmitter Architecture
  - CMOS Implementation
  - Integrated PA
  - Take Advantage of Auto-Calibration Schemes
Implementation Challenges

• Direct Conversion:
  – DC offsets
  – Flicker noise on receive path
  – Rx path and/or Tx path oscillations
  – Quadrature accuracy
  – LO pulling
  – LO feedthrough

• Integrated PA
  – High linearity requirements for PA

• Auto-Calibration
  – Automatic Carrier Frequency Control (AFC) Loop
BCM2060 Simplified Radio Architecture

Balun

Optional BPF

RX Baseband

LO Generation

PLL

XO

AFC

JTAG

RC & R calibration

Balun

Sensors out
RSSI’s out
RX_I out
RX_Q out

4 wires JTAG
Crystal Clock out
AFC_I in
AFC_Q in

TX_I in

TX_Q in
Receiver Description

- Full integration
- On-Chip LNA input matching
- High-gain, low-noise, high-linearity, gain controllable LNA/mixer
- 3 stages of high-pass VGA’s
- A 5th-order Chebychev LPF
- Dual RSSI’s
- System NF of 4dB and max gain of 93dB is achieved
Transmitter Description

- Full integration
- 3rd-order Butterworth LPF’s
- Baseband and RF VGA’s
- High-linearity, high-power integrated class AB power amplifier
- On-chip power amplifier output matching
- TX P_{1dB} of 19dBm and P_{sat} of 23dBm are achieved
PLL Description

- Full Integration
- Integer-N PLL with programmable loop bandwidth
- “Fractional-VCO”† with $f_{vco} = 2/3 \ f_r$
  - Reduces pulling from high-power on-chip PA
  - Reduces transmitter LO feed-through
  - Reduces receiver DC offsets due to self-mixing
- Automatic frequency control integrated into PLL
- PLL achieves PN of <-100dBc/Hz@30KHz offset with $f_r = 5.24 \text{ GHz}$

†H. Darabi, et. al., ISSCC 2001
Chip Level Auto-Calibration

- VCO tuning
- AFC
- AFC self-calibration
- R-Calibration on bandgap blocks
- RC time constant calibration
- Integrated power detector
- Integrated temperature sensor
- Transmit LO feedthrough cancellation
Rx System NF and Sensitivity

![Graph showing Gain and NF vs BB Frequency and Data Rate](image.png)

**Gain [dB]**

- 100
- 96
- 92
- 88
- 84
- 80
- 76
- 72
- 68

**NF [dB]**

- 0.1
- 1
- 10

**BB Frequency [MHz]**

- 80
- 84
- 88
- 92
- 96

**Rx Sensitivity [dBm]**

- 8.9 dB (σ = 0.4 dB)
- 11.7 dB (σ = 0.3 dB)

**Data Rate [Mbps]**

- 0
- 20
- 40
- 60
Measured Transmit Output Power

Data Rate [Mbps]

Average OFDM Output Power [dBm]

- saturated power limited
- EVM limited
- spectral mask limited
Measured TX Power Spectrum

12.8dBm, 54Mbps, QAM64 (EVM Limited)

18.7dBm, 36Mbps, QAM16 (Spectral Mask Limited)
# Summary of Transceiver Performance

<table>
<thead>
<tr>
<th></th>
<th>Measured (this paper)</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Frequency Band</strong></td>
<td>5.15 – 5.35 GHz</td>
<td>GHz</td>
</tr>
<tr>
<td><strong>RX NF</strong></td>
<td>4</td>
<td>dB</td>
</tr>
<tr>
<td><strong>RX Sensitivity (6Mbps)</strong></td>
<td>-93.7 ± 0.9 dBm</td>
<td></td>
</tr>
<tr>
<td><strong>RX Sensitivity (54Mbps)</strong></td>
<td>-73.9 ± 1.2 dBm</td>
<td></td>
</tr>
<tr>
<td><strong>RX IIP3</strong></td>
<td>-4.8</td>
<td>dBm</td>
</tr>
<tr>
<td><strong>RX IIP2</strong></td>
<td>&gt; 30</td>
<td>dBm</td>
</tr>
<tr>
<td><strong>RX Gain Range</strong></td>
<td>15 to 93 dB</td>
<td></td>
</tr>
<tr>
<td><strong>TX Power Range</strong></td>
<td>-30 to +18.7 dBm</td>
<td></td>
</tr>
<tr>
<td><strong>TX Psat</strong></td>
<td>+23</td>
<td>dBm</td>
</tr>
<tr>
<td><strong>TX P-1dB</strong></td>
<td>+19</td>
<td>dBm</td>
</tr>
<tr>
<td><strong>Vdd</strong></td>
<td>1.8 V</td>
<td>V</td>
</tr>
<tr>
<td><strong>Vdd_PA</strong></td>
<td>3.3 V</td>
<td>V</td>
</tr>
<tr>
<td><strong>Phase Noise @ 30KHz</strong></td>
<td>-100 dBc/Hz</td>
<td></td>
</tr>
<tr>
<td><strong>RX Power Consumption</strong></td>
<td>150 mW</td>
<td>mW</td>
</tr>
<tr>
<td><strong>TX Power Consumption</strong></td>
<td>380 (15dBm OFDM output) mW</td>
<td></td>
</tr>
<tr>
<td><strong>ESD</strong></td>
<td>&gt; ±2.5 on all pins</td>
<td>KV</td>
</tr>
<tr>
<td><strong>Technology</strong></td>
<td>0.18um 1P5M CMOS</td>
<td></td>
</tr>
<tr>
<td><strong>Die Size</strong></td>
<td>11.7 (including padring) mm²</td>
<td></td>
</tr>
</tbody>
</table>
Die Microphotograph of BCM2060

RX

PLL/AFC

TX
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Flat-Channel Sensitivity Test Diagram

REFERENCE (Transmitter) -> RF mux -> Power Meter -> DUT (Receiver)

- Dir. Coupler
- Prog. Attenuator
- Dir. Coupler
802.11g System Sensitivity Test Result

1 Mbps sensitivity
-97 dBm

54 Mbps sensitivity
< -70 dBm

Results include all PCB and connector losses.
Measured BCM2060 Phase Noise

Residual PM = 0.0075 rad = 0.43 deg

From 1 kHz
To 305.8116 kHz

Target Specifications
Measured 802.11a TX Constellation Diagram

EVM = -33dB
Po = +6dBm
64-QAM
54 Mbps

RBW: 312.5 kHz
TimeLen: 40 Sym
Measured 802.11a TX EVM Histogram

EVM = -33dB
Po = +6dBm
64-QAM
54 Mbps
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Conclusions

- Highest Performance, Highest Integration, Smallest Size, Lowest Power Consumption IEEE 802.11g Transceiver Reported to Date
  - 4 dB Rx chain noise figure
  - Excellent performance in the presence of real-world impairments
  - Fully integrated, direct conversion
  - Various integrated self contained or system level calibration capabilities for high yield and tight tolerances
  - 790 mW transmit or receive (1.8 V), RF and baseband/MAC
  - 10 mW sleep mode, RF and baseband/MAC
  - 802.11g receiver sensitivity with all board losses
    - -70 dBm 54 Mbps
    - -97 dBm 1 Mbps
Conclusions

• Highest Performance, Highest Integration, Smallest Size, Lowest Power Consumption IEEE 802.11a Transceiver Reported to Date
  – 4 dB Rx chain noise figure
  – 23 dBm Tx $P_{\text{sat}}$ with integrated PA
  – Excellent performance in the presence of real-world impairments
  – Fully integrated, direct conversion
  – Integrated or system level calibration capabilities for high yield and consistent performance
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