VV6411/VV6410/VV6500 & STV0676

USB CIF/VGA Digital Camera Chipset

The USB camera chipsets from STMicroelectronics are at the heart of a variety of products which have proven to be highly successful in a demanding marketplace. Supported by comprehensive reference designs, technical backup and fully-featured software drivers, STMicroelectronics offers camera manufacturers the opportunity to benefit from rapid time to market with a product of proven quality.

The VV6411/VV6410 and VV6500 are ColorMOS™ digital CMOS sensors that deliver outstanding picture quality. These sensors have been created specifically to meet the standards required for personal video communications. Both sensors feature automatic black and dark level calibration to ensure optimum image quality.

The STV0676 co-processor is an evolution of the STV0672 product. STV0676 will operate at a lower core voltage and reduced internal clock rates resulting in significantly lower power consumption than STV0672.

Additional improvements realised with STV0676 include 30fps VGA and CIF capability, improved video compression and a new I2C slave mode to fully enable embedded video applications.

The STV0676 requires a 1V8 source to power the internal core logic. This supply will be delivered by an external voltage regulator or direct from a future generation sensor.

The STV0676 co-processor receives image data from the sensor, that is processed, compressed and passed to the USB port. It incorporates a digital video processor engine, which performs automatic exposure, automatic gain control and automatic white balance, together with colour matrixing, gamma correction, aperture correction, automatic defect correction and noise cancellation logic. This data is then passed to the proprietary video compression block that delivers high frame rates with minimum impact on image quality. The USB interface supports USB isochronous data transfer mode, ensuring access to guaranteed bandwidth at all time, irrespective of how many peripherals are then added.

The chipset is backed by a fully-featured driver which provides a wide range of user-definable settings for optimum camera setup. The user interface supports a degree of customisation.

KEY FEATURES

- Real-time video - up to 30fps CIF,30fps VGA
- Multiple output video modes supported
- USB 1.1 compliant
- Motion-JPEG compression
- Isochronous USB data transfer
- Automatic black and dark level calibration
- Full VfW and TWAIN driver support
- Integrated voltage regulation
- On the fly pixel defect detection and correction
- Minimal BOM for complete USB camera
- Programmable vendor ID
- Embedded applications support
  - I2C slave (low speed)
  - JPEG/YCbCr video out port

APPLICATIONS

- USB Camera
- Biometric identification
- Toys and games

SPECIFICATIONS

Pixel resolution	352 x 288 (CIF) 640 x 480 (VGA)
Exposure control	Automatic (to +82dB)
Gain control	Automatic (to +24dB)
Signal/Noise ratio	c.56dB
Supply voltage	4V1-6V0 DC (internally regulated)
USB Compatibility	USB Specification V1.1 Meets full power management requirements with no external components required
Chipset Supply current	< 100mA (CIF @ 30fps) < 100mA (VGA @ 30fps)
Operating temperature (ambient)	0^{o}C - 40^{o}C (for extended temp. info please contact STMicroelectronics)
Package type	VV6410C036: 36CLCC VV6411C036: 36CLCC,44OTQFP VV6500C001: 48CLCC STV0676: 64TQFP

Table of Contents

1. Document Revision History

Revision	Date	Comments
1.0	17/01/01	First Product preview release
1.1	22/01/01	Information added on • Microport • Serial EEPROM • digiport • Slave I2C implementation • I2C Register map
1.2	01/02/01	Microport description updated
A	07/03/01	Details of exisiting STV0672 register map removed to avoid confusion Added reference to VV6411 sensor

Table 1 : Document Revision History

2. Introduction

2.1 STV0676 Chipset General Description

The STV0676 is a digital video processor requiring no external RAM and minimum of passive support components to provide a complete USB camera. STV0676 accepts raw digital video data from a CIF format CMOS sensor (VV6411/VV6410) or from a VGA format CMOS sensor (VV6500) and is capable of transferring the resulting JPEG compressed YCbCr video data to a host PC over USB at rates up to 30 frames per second CIF or VGA.

The STV0676 architecture consists of a number of separate functional blocks:

- Video Processor (VP) to include interface logic to sensor
- Video Compressor (VC)
- USB control block
- General purpose control

The VP controls the VV6411/VV6410/VV6500 sensor and processes the raw RGB pixel data into YCbCr images

This YCbCr data is compressed by the VC.

The USB control block transfers the compressed data to the host PC. System operation, responding to host requests and commands as well as performing sensor exposure control and colour balance is handled by the video processor (VP).

2.2 Video Processor (VP)

2.2.1 Video Processor/Sensor Interface

The STV0676 video processor (VP) module provides formatted YCbCr 4:2:2-sampled digital video to the video compressor (VC) module at frame rates up to 30 frames per second. The VP also interfaces directly to the VV6411/VV6410/VV6500 image sensors. The interface to the sensor incorporates:

- A 5-wire data bus SDATA[4:0] for receiving both video data and embedded timing references.
- A 2-wire serial interface SSDA,SSCL to control the sensor (allow reconfiguration of the sensor registers).
- The sensor clock SCLK.
- The sensor regulates the USB system power to 3V3 for both the sensor and the STV0676. The sensor requires one external simple transistor in conjunction with the internal regulator to provide current drive to be able to successfully power the 3V3 for the complete camera system
- The sensor also provides a power-on-reset signal that is used to reset the STV0676. This power-on-reset signal also resets the sensor.
- The module supports USB suspend mode.

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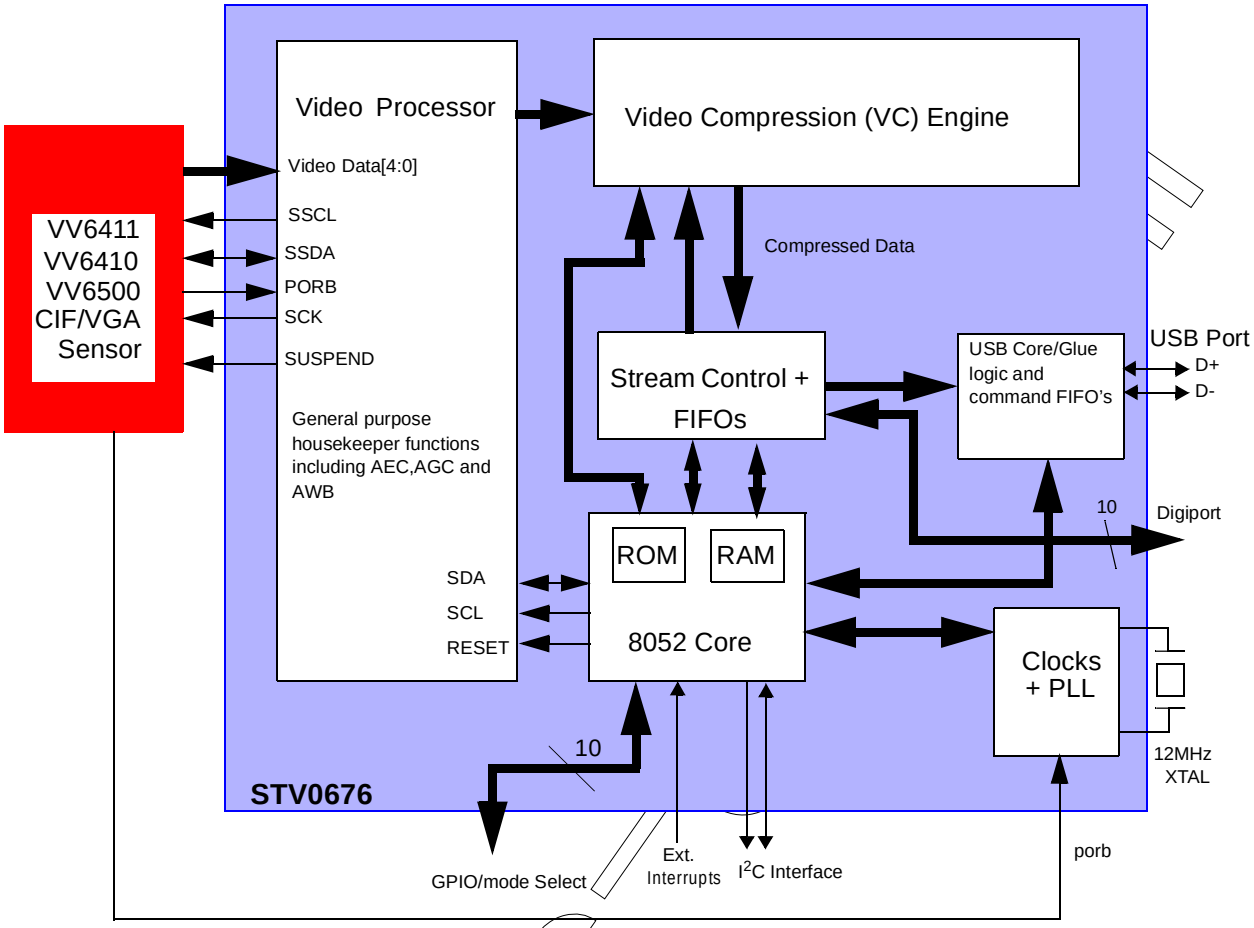

Figure 1 : Block Diagram of STV0676 Video Processor Module

2.2.2 Video Processor Functions

STV0676 provides a master clock SCLK to the camera module. Each 10-bit pixel value generated by the sensor is transmitted across the 5wire, (the MSBit of the databus is unused in the current application but it will support future sensors where a 12bit ADC architecture may be used), databus SDATA[4:0] as a pair of sequential 5-bit nibbles, most significant nibble first. Codes representing the start and end frames and the start and end of lines are embedded within the video pixel data stream to allow the video processor receiver to synchronise with the video data which the sensor is generating.

The video processing engine performs the following functions on incoming data

- full colour restoration at each pixel site from Bayer-patterned input data
- matrixing/gain on each colour channel for colour purity
- peaking for image clarity
- gamma correction
- colour space conversion (including hue and saturation control) from raw RGB to YCbCr[4:2:2].

The 2-wire sensor serial interface (SSDA and SSCL) provides control of sensor configuration.

2.2.3 Auto Exposure and Gain Control

Control of the sensor exposure is automatically controlled by STV0676. Sensor exposure is evaluated (and, where necessary modified) once per frame, where a frame consists of 2 video fields. The video fields are identical in length, that is they do not

contain any of the half line detail of the analogue video standards like CCIR or NTSC. Two fields per frame are required by the internal sensor video timing model. Integration time, sensor analogue gain and STV0676 digital gain are all used to control the overall exposure. The STV0676 exposure algorithm uses an asymptotic approach in calculating the change required in the present exposure value to approach the requested exposure target.

2.2.4 Defect Correction

STV0676 automatically detects and corrects for pixel defects, without the need for any additional components or additional sensor calibration procedures. This greatly simplifies camera assembly and test, when compared with previous EEPROM-based defect correction schemes. The pixel defect correction scheme in STV0676 ensures that VV6411/VV6410+STV0676 and VV6500+STV0676 are 'defect free' chipsets.

2.3 Video Compression (VC) Engine

The video compression engine performs 3 main functions:

- Up scaling of input YCbCr 4:2:2 video stream from the VP (typically to scale from QVGA to CIF image formats)
- Compression and Encoding of YCbCr stream into Motion-JPEG (M-JPEG) format
- USB Bandwidth monitoring

The data stream from the VP can be upto VGA size. The scaler in VC can downsize this image. Once scaled the video stream is then converted into M-JPEG format. M-JPEG simply treats video as a series of JPEG still images. The conversion is realised via a sequential DCT (Discrete Cosine Transform) with Huffman encoding. After transfer over USB the M-JPEG stream will be decoded in the Video-for-Windows (VfW) device driver running on the host.

The VC module is capable of compression ratios of up to 100:1 although clearly this is scene dependent. Image framerate produced by the STV0676 chipset is fixed and furthermore the available USB bandwidth is also fixed (within the software driver). The VC module varies the compression ratio to match the fluctuating input video data rates, that vary according to scene dynamics, to the available USB bandwidth and required framerate.

The final stage of the VC block manages the data transfer rate from the local VC FIFO store to the USB core. STV0676 can perform this management automatically, by employing long-term (frame-level) and short-term (block-level) compression management. The former is achieved by varying a scalar quality-factor from frame to frame, to drive expected data rates upwards or downwards. The latter is achieved by truncating the zig-zag sequence of AC coefficients more or less severely according to how many preset thresholds of FIFO usage have been crossed. As FIFO usage approaches maximum, this truncation process reduces instantaneous data rates until stability is regained, at the cost of local loss of detail in the image. The latter process is transparent to the decoder. Statistics of threshold-crossing activity are subsequently used in the long-term quality setting decision.

2.4 Control Processor

The embedded 8052 microprocessor core plays a very important role within the STV0676 controlling data flow through the major sub blocks within STV0676 as well as the I2C communications to reconfigure VP in line with requests from the device driver.

2.5 VV6411/VV6410/VV6500 General Description

The VV6411 and VV6410 sensor are CIF format, 352 x 288 pixels, CMOS image sensors capable of outputting digital pixel data at frame rates, of up to 30 frames per second. The VV6500 sensor is a VGA format, 640 x 480 pixels, CMOS image sensor capable of outputting digital pixel data at frame rates, of up to 30 frames per second in VGA mode. Both sensor arrays are covered by colour filters.

VV6411/VV6410/VV6500 have on-chip 10-bit analogue to digital converters and are designed to interface directly to the STV0676 co-processor chip as described above.

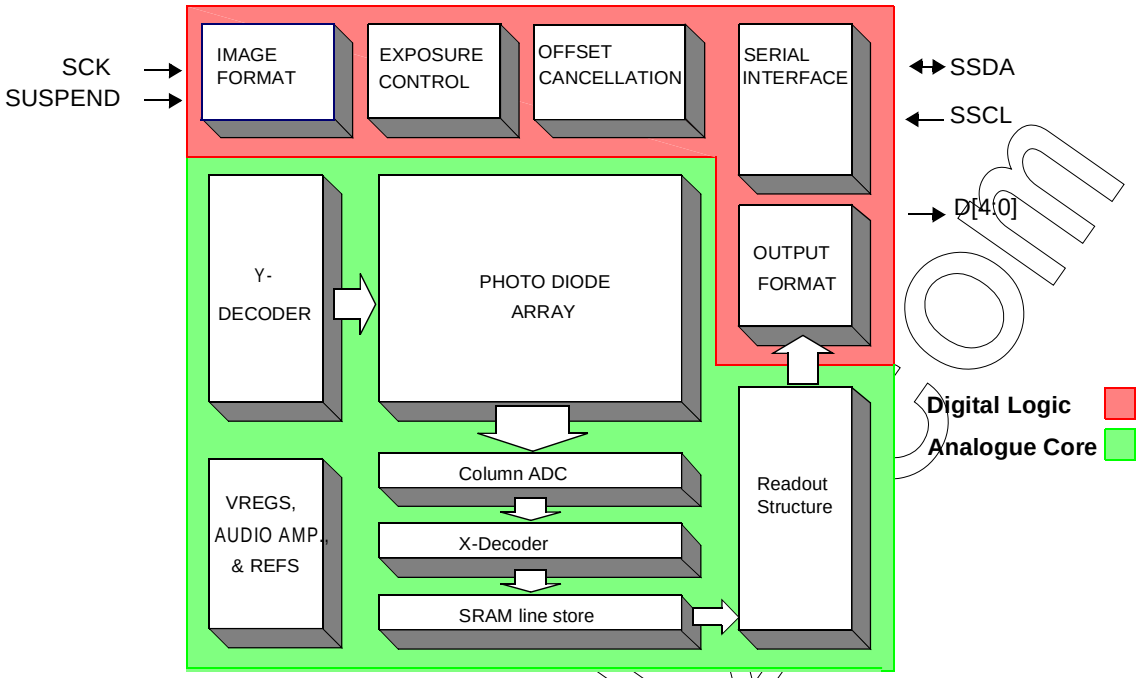

Figure 2 : Block Diagram of VV6411/VV6410/VV6500 Image Sensor (5-wire output)

2.5.1 Image Format

The output image format is either CIF (352 x 288 pixel array) or VGA (640 x 480 pixel array). To provide the colour co-processor with the extra information it needs for interpolation at the edges of the VV6411/VV6410/VV6500 pixel array, an additional border 2 pixels deep on all 4 sides of the array is enabled under serial interface control. The resulting image size of 356 x 292 pixels (or 644 x 484 pixels for VGA) is the default power up state for this sensor. The pixel array is covered by a set of Bayer pattern colour dyes, see Figure 3 for details.

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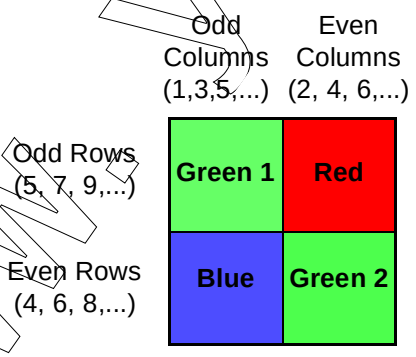

Figure 3 : Bayer Colourisation Pattern

2.6 Power Management

All the power management for the chipset is controlled by the sensor. A series of on board voltage regulators regulate the incoming VBUS supply to derive all the necessary power supplies required by the camera chipset.

The chipset conforms to all power requirements specified by USB Version 1.1.

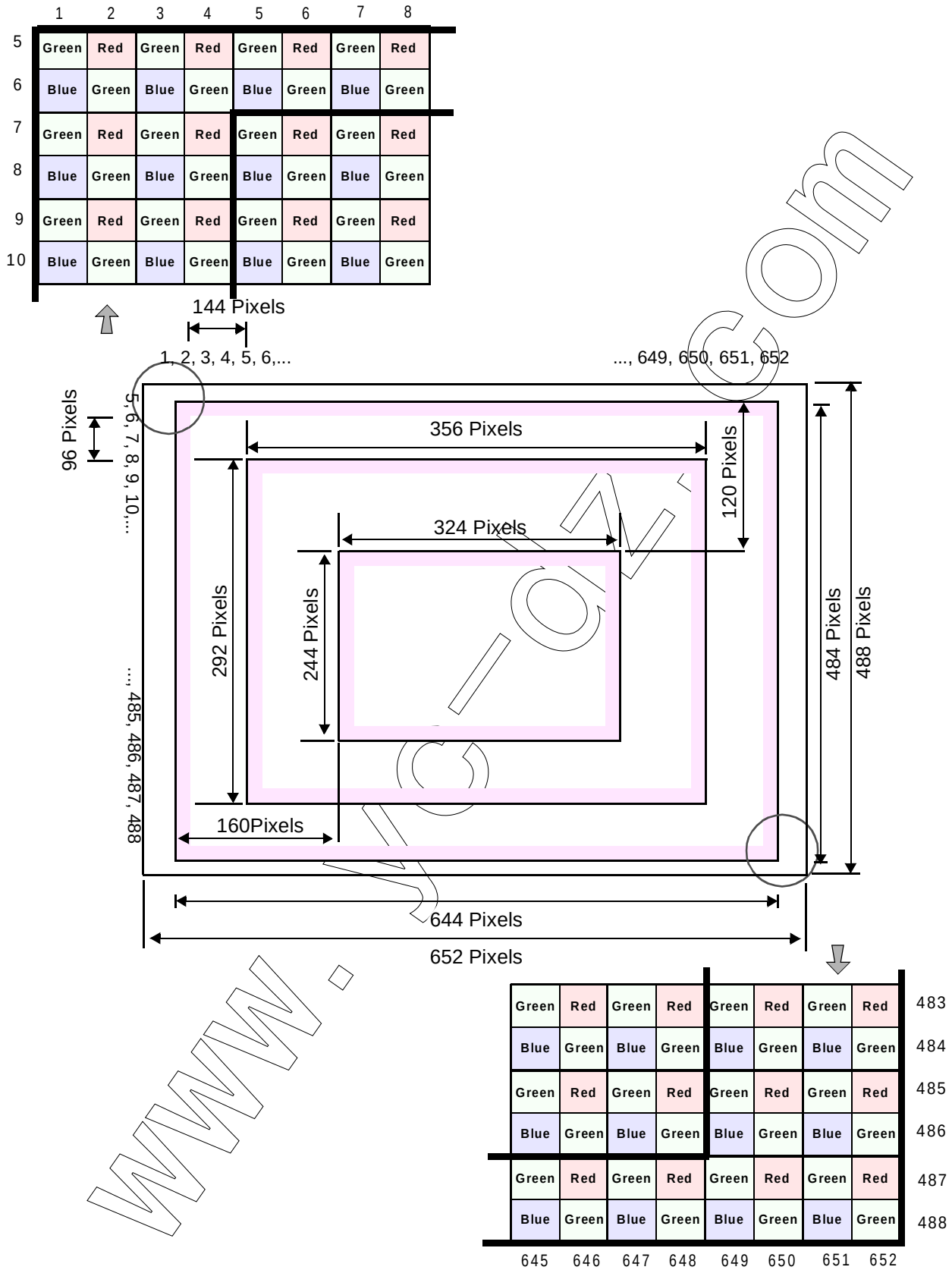

Figure 4 : Image Formats

2.7 Suspend Mode

Under the control of the SUSPEND pin VV6411/VV6410/VV6500 can be forced into an ultra low power mode. The sensor will consume less than 80µA of current while suspended and the STV0676 device will consume approximately 50µA. The total chipset consumption therefore is approximately 150µA.

The sensor will enter suspend mode when the SUSPEND pin has been driven high. It is important to note that the clock to the sensor should be kept running during the SUSPEND mode.

Mode	Description	Approx. Module Current
Suspend	Camera module in lowest power state. Suspend has been asserted by host and all blocks within STV0676 have been powered down.	TBA

Table 2 : STV0676 chipset power consumption

2.8 Still Image Upload and Remote Wake-Up

The present STV0676 reference design includes 2 micro switches, identified as SW1 and SW2. Two special functions are supported by these switches - image upload via a TWAIN driver and remote wake up of the host.

Presently both of these features will be invoked by depressing SW1. If the camera/host is in standby mode then pressing SW1 will force the system to wake up. Thereafter SW1 will control the uploading of still images to the host. It is important to note that STV0676 must always be used in tethered mode, attached to a PC, and there is no local memory for image storage.

3. External Interfaces

3.1 USB Interface

The USB Interface is designed to be compliant with the Version 1.1 of the USB Specification. The STV0676 chipset solution is a low Power Device and is therefore suitable for connection to any USB port on a PC or on a self-powered hub or when connected to a bus-powered hub. Please contact STmircoelectronics for confirmation.

The device fits into the Device Framework specified in Chapter 9 of the USB Specification as follows:

- The device supports a single high power configuration (*Configuration 1*).
- *Endpoint 0* is the default control endpoint and is always supported
- *Endpoint 0* supports all of the USB commands required by the device framework.
- Vendor Specific commands on *Endpoint 0* are used for all device control.
- *Configuration 1* supports a single interface *(Interface 0*)
- *Interface 0* supports 8 alternate settings (*Alternates 0-7*)
- The alternate settings support between 0 and 2 additional endpoints.
- *Endpoint 1* is used for Isochronous transfer of image data
- *Endpoint 3* is used for transferring status information, e.g. state of a hardware button.
- The endpoints are configured as follows in the alternate settings:

Alternate Setting	Endpoint1 (Isochronous)	Endpoint3 (Interrupt)
0	Not present	Not present
1	Not present	8 bytes/packet; 1 packet/8 Frames
2	128 bytes/packet; 1 Packet/frame	8 bytes/packet; 1 packet/8 Frames
3	384 bytes/packet; 1 Packet/frame	8 bytes/packet; 1 packet/8 Frames
4	640 bytes/packet; 1 Packet/frame	8 bytes/packet; 1 packet/8 Frames
5	768 bytes/packet; 1 Packet/frame	8 bytes/packet; 1 packet/8 Frames
6	896 bytes/packet; 1 Packet/frame	8 bytes/packet; 1 packet/8 Frames
7	1023 bytes/packet; 1 Packet/frame	8 bytes/packet; 1 packet/8 Frames

Table 3 : Endpoint Alternate Settings

The best and most consistent performance in terms of image quality will always be obtained in the highest bandwidth setting (Alternate 7). Under some circumstances it may not be possible for the host to allocate this amount of USB bandwidth to the device.

The isochronous settings reserve varying quantities of bandwidth - from 10% to 85% of USB bandwidth. The lower settings will give poor image quality due to heavy compression applied to maintain high framerate streaming of image data, but at the same time will leave more bandwidth free for other USB devices. This may be more desirable if more than one camera is to be used, or if there are other isochronous peripherals connected. The device driver allows the user to specify the maximum bandwidth they wish to allocate to data transfer from the device. If the maximum specified by the user is not available, perhaps because another isochronous device has already reserved that bandwidth, then lower alternates will be tried until one succeeds.

Benchmark testing of the STV0676 indicates that 30fps CIF video (compressed) can be accomodated in 50% of USB bandwidth.

3.2 Mode selection

All USB devices will report a VID, PID and power consumption as part of a Standard Device Descriptor. The VID and PID for STV0676 can be configured by the state of the digiport bus bits or alternatively by an EEPROM. The mode selection is made using the 2 MODESEL pins as described in Table 4 below.

MODESEL[1]	MODESEL[0]	Mode of operation
0	0	USB Mode. External EEPROM fitted therefore PID,VID and power consumption read from this source. See Section 3.4
1	0	Slave I^2C mode.
0	1	USB mode. Default. No external EEPROM fitted the PID,VID and power consumption data determined by digiport[7:0]. See Section 3.3
1	1	Reserved

Table 4 : Mode Selection

3.3 Selecting VID and PID via the Digiport

The current reference design for the STV0676-chipset has digiport[7:0] connected to VSS, thus the VID and PID are 16'h0553 and 16'h0140 respectively.

The digiport also controls the device current consumption that is reported to the host at device enumeration.

digiport bit slice	Function
[3:0]	Configures the ls nibble of the PID
[5:4]	Master VID/PID select
[7:6]	Power setting

Table 5 : Basic Digiport Configuration

digiport[3:0]	PID ls nibble
4'b0000	4'b0000
4'b0001	4'b0001
4'b0010	4'b0010
4'b0011	4'b0011
4'b0100	4'b0100
4'b0101	4'b0101
4'b0110	4'b0110
4'b0111	4'b0111
4'b1000	4'b1000

Table 6 : Digiport ls nibble Configuration

digiport[3:0]	PID ls nibble
4'b1001	4'b1001
4'b1010	4'b1010
4'b1011	4'b1011
4'b1100	4'b1100
4'b1101	4'b1101
4'b1110	4'b1110
4'b1111	4'b1111

Table 6 : Digiport ls nibble Configuration

digiport[5:4]	VID/PID Reported
2'b00	16'h0553/16'h014x[1]
2'b01	16'h0553/16'h015x[1]
2'b10	16'h0553/16'h016x[1]
2'b11	16'h0553/16'h017x[1]

Table 7 : Master VID/PID Selection

1. **The 'x' ls nibble of the PID is defined by the value from Table 6 above**

digiport[7:6]	Current consumption reported
2'b00	98mA
2'b01	250mA
2'b10	350mA
2'b11	500mA

Table 8 : Device Power Consumption Indicator

3.4 Serial EEPROM

STV0676 is designed to be used with a 128 or 256 byte serial I2C EEPROM. The EEPROM can be programmed with data to allow a user to fully customise the USB identity of STV0676. The configuration of this data is as follows:

3.4.1 EEPROM Format and Contents

Location	Contents
0	Fixed number, must be 0x'ED
1	Fixed number, must be 0x'15

Table 9 : EEPROM Format and Contents

Location	Contents
2	Reserved, must be 0x'00
3	Max device power (=mA/2, e.g. 400mA enter 0x'C8)
4	VidLo, low byte of the vendor ID
5	VidHi, highbyte of the vendor ID
6	PidLo, low byte of the product ID
7	PidHi, highbyte of the product ID
8	Manufacturer string offset ,example below
9	Product string offset, see below
10	Interface 0 String offset
11	Reserved, must be 0x'00
12	Reserved, must be 0x'00
13	Checksum

Table 9 : EEPROM Format and Contents

The remaining space is available for the string blocks indexed at locations 8, 9 and 10.

3.4.2 Strings

The strings referred to above are the USB String descriptors referenced from the device, configuration and interface descriptors. The value should be set to '0' if the string is not implemented, or the offset in bytes of the start of the string block in the EEPROM.

The first byte of each string block is the number of the characters in the string. Subsequent bytes are the actual string, which need not include a terminating null. An Example might be:

Location	Contents
8	Manufacturer string offset = 16
16	String length = 5
17	String text = 'H' (in ascii)
18	String text = 'e' (in ascii)
19	String text = 'l' (in ascii)
20	String text = 'l' (in ascii)
21	String text = 'o' (in ascii)

Table 10 : EEPROM device string example

3.4.3 CheckSum

The checksum is calculated by adding the byte value of EEPROM locations 0 to 12 inclusive, the low order byte of the result is stored in location 13.

3.5 I2C Slave mode

STV0676 can be configured to act as an I2C slave. This new feature has been introduced in STV0676 to address embedded video applications where the device registers cannot be controlled over USB. Details of the I2C messages supported and

description of the full I2C resister bank is available from STMicroelectronics.

3.6 Digiport input and output

The digiport is a 10bit bus that can operate input and output operations as well as hold the PID, VID and power comsumption data for USB. Full details on the digiport operation and control are available from STMicroelectronics.

3.7 General Purpose Input and Output

STV0676 makes up to 8 pins available as general purpose inputs or outputs. It is envisaged that these pins could be used to drive led's, buzzers or perhaps take input from switches.

4. Detailed specifications

4.1 STV0676 Absolute Max Ratings

Description	Range	Unit
Operating Temperature	0 to 70	°C
Storage Temperature	-50 to 150	°C
Voltage on USB D+/D-	0 - VDD	V

4.2 STV0676 AC/DC Characteristics

Parameter	Description	Min	Typ	Max	Units	Comments
VDD_CORE	Primary STV0676 Power Supply	1.55	1.8	1.95	V	4
VDD_IO	3.3V Power Supply for on-chip USB tranceiver and IO	3.0	3.3	3.6	V	
VDD_PLL	Analog supply to the PLL	1.60	1.8	2.0	V	4
$I_{suspend}$	Suspend/powerdown mode current				µA	
I_{active}	Active, high power mode current				mA	
I_{active}	STV0676 active, low power mode current				mA	VDD at 3V6 with VV6411/VV6410 sensor
					mA	VDD at 3V6 with VV6500 sensor
$I_{leakage}$	Leakage current				µA	
V_{ILU}	USB differential pad D+/D- input low			0.8	V	
V_{IHU}	USB differential pad D+/D- input high (driven)	2.0			V	
V_{IHUZ}	USB differential pad D+/D- input high (floating)	2.7		3.6	V	
V_{DI}	USB differential pad D+/D- input sensitivity	0.2			V	1
V_{CM}	USB differential pad D+/D- common mode voltage	0.8		2.5	V	2
V_{OLU}	USB differential pad D+/D- output low voltage	0.0		0.3	V	
V_{OHU}	USB differential pad D+/D- output high voltage	2.8		3.6	V	
V_{CRS}	USB differential pad D+/D- output signal cross over voltage	1.3	1.65	2.0	V	
R_{PU}	USB differential pad D+/D- pullup resistor	1.425		1.575	KΩ	
R_{PD}	USB differential pad D+/D- pulldown resistor	14.25		15.75	KΩ	
V_{Il}	CMOS input low voltage (XTAL_IN)			0.687	V	
V_{IH}	CMOS input high voltage (XTAL_IN)	1.19			V	
V_{HYS}	Hysteresis (XTAL_IN)		0.51		V	
V_{Il}	CMOS input low voltage			0.35VDD	V	3
V_{IH}	CMOS input high voltage	0.65VDD			V	3
V_{T+}	CMOS schmitt input low to high threshold voltage		2.15		V	3
V_{T-}	CMOS schmitt input high to low threshold voltage		1.05		V	3
V_T	Threshold point		1.65		V	3
V_{OH}	Output high voltage	2.4			V	
V_{OL}	Output low voltage			0.4	V	

4.3 Chipset VV6411/VV6410/VV6500+STV0676

Mode of Operation		VV6410/ VV6411+STV0676	VV6500+STV0676
Standby mode	Camera module in lowest power state. Suspend has been asserted by host. The clock to sensor has been removed and all blocks within STV0676 have been powered down.	TBA	TBA
Start-up mode	STV0676 is in low power mode. Fast clocks enabled allowing STV0676 to process commands from host PC. Sensor and video processor module are held in reset	TBA	TBA
Active mode	All STV0676 modules and sensor are enabled with video data being transferred to host PC.	TBA	TBA

Table 11 : VV6411/VV6410/VV6500+STV0676 chipset current consumption

4.1 VV6411/VV6410 AC/DC Specification

Parameter	Comment	Units
Image Format	356 x 292 pixels (CIF)	-
Pixel Size	7.5 x 6.9	µm
Technology	0.5µm 3 level metal CMOS	-
Array Format	CIF	-
Exposure control range	81 (minimum exposure period 3µs and maximum exposure period is 33ms)[1]	db
Supply Voltage	3.0-6.0 DC +/-10%	V
Operating Temp. range	0 - 40	^{o}C
V_{OL_max}[2]	0.512	V
V_{OH_min}[3]	2.054	V
V_{I_maxL}[4]	0.683	V
V_{IH_min}[5]	2.237	V
Serial interface frequency range	0-100kHz	

1. **We assume CIF (30fps) mode, input clock of 16MHz and internal clock divisor of 1.**
2. **This will be worst case reading. Device outputs had significant capacitive loading and supply voltage reduced to 2V7**
3. **This will be worst case reading. Device outputs had significant capacitive loading and supply voltage reduced to 2V7**
4. **This will be worst case reading. Device outputs had significant capacitive loading and supply voltage reduced to 2V7**
5. **This will be worst case reading. Device outputs had significant capacitive loading and supply voltage reduced to 2V7**

Table 12 : VV6411/VV6410 DC specification

4.2 VV6500 AC/DC Specification

Parameter	Comment	Units

Image Format	644 x 484pixels (VGA)	-
Pixel Size	7.5 x 7.5	µm
Technology	0.5µm 3 level metal CMOS	-
Array Format	VGA	-
Exposure control range	81 (minimum exposure period 3µs and maximum exposure period is 33ms)[1]	db
Supply Voltage	3.0-6.0 DC +/-10%	V
Operating Temp. range	0 - 40	°C
V_{OL_max}[2]	TBA	V
V_{OH_min}[3]	TBA	V
V_{I_maxL}[4]	TBA	V
V_{IH_min}[5]	TBA	V
Serial interface frequency range	0-100	kHz

1. **We assume CIF (30fps) mode, input clock of 16MHz and internal clock divisor of 1.**
2. **This is worst case reading. Device outputs had significant capacitive loading and supply voltage reduced to 2V7**
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4. **This is worst case reading. Device outputs had significant capacitive loading and supply voltage reduced to 2V7**
5. **This is worst case reading. Device outputs had significant capacitive loading and supply voltage reduced to 2V7**

Table 13 : Preliminary Data for VV6500

4.3 VV6410 Optical Characterisation Data

Optical Parameter[1]	Min	Typical	Max	Units
Dark Current	-	46	-	mV/sec
Average Sensitivity	-	2.1	-	V/lux.sec
Fixed Pattern Noise (FPN)	-	1.74	-	mV
Vertical Fixed Pattern Noise (VFPN)	-	1.2	-	mV
Random Noise	-	1.17	-	mV
Sensor SNR	-	c.56	-	dB
Shading (Gross)	-	0.9	-	mV

Table 14 : VV6411/VV6410 Optical Characterisation Data

1. **All of these parameters are measured at 25°C**

4.4 VV6411/VV6410 Optical Characterisation Data

Optical Parameter[1]	Min	Typical	Max	Units
Dark Current	-	TBA	-	mV/sec
Average Sensitivity	-	TBA	-	V/lux.sec
Fixed Pattern Noise (FPN)	-	TBA	-	mV
Vertical Fixed Pattern Noise (VFPN)	-	TBA	-	mV
Random Noise	-	TBA	-	mV
Sensor SNR	-	TBA	-	dB
Shading (Gross)	-	TBA	-	mV

Table 15 : VV6411/VV6410 Optical Characterisation Data

1. **All of these parameters are measured at 25 °C**

4.5 VV6500 Optical Characterisation Data

Optical Parameter[1]	Min	Typical	Max	Units
Dark Current	-	TBA	-	mV/sec
Average Sensitivity	-	TBA	-	V/lux.sec
Fixed Pattern Noise (FPN)	-	TBA	-	mV
Vertical Fixed Pattern Noise (VFPN)	-	TBA	-	mV
Random Noise	-	TBA	-	mV
Sensor SNR	-	TBA	-	dB
Shading (Gross)	-	TBA	-	mV

Table 16 : VV6500 Optical Characterisation Data

1. **All of these parameters are measured at 25 °Cfs**

4.5.1 Noise Parameters and Dark Current

Various noise parameters are measured on the 411/410 and 500 series sensors as follows:

- Fixed Pattern Noise (FPN)
- Vertical Fixed Pattern Noise (VFPN)
- Random Noise
- Fine Shading
- Gross Shading

The parameters will be described in more detail below along with the data produced by the characterisation programme.

4.5.2 Blooming

Blooming is a phenomenon that does not affect CMOS sensors in the same way as CCD imagers are afflicted. With a CCD blooming can cause an entire column/columns to flood and saturate.

CMOS imagers are however affected by a different type of saturation. If an intense light source, (e.g. Maglite torch), is shone at very close proximity to the image sensor the pixel sampling mechanism will break down and rather than displaying a saturated white light a black image will occur.

The 411/410 pixel architecture uses Correlated Double Sampling (CDS) to help reduce noise in the system. The pixel is read normally first, yielding the true integrated signal information, then the pixel is reset and very quickly read for a second time This normally yields black information - as the pixel has had no exposure time - that can be subtracted from the signal from the first read. This subtraction will remove much of the noise from the pixel leaving only the useful signal information.

In an example where a pixel has saturated in both the first and the second reads due to an intense light source. When the noise cancellation subtraction operation is then performed the result is close to zero signal from the pixel therefore resulting in the displayed black image.

We do not perform any test measurements for this phenomenon.

4.5.3 Dark Current

This is defined as the rate at which the average pixel voltage increases over time with the device not illuminated. The dark current will be measured at a gain setting of 4 and a clock divisor of 16 at a fixed temperature and will be expressed in mV.

4.5.4 Fixed Pattern Noise

The FPN of an image sensor is the average pixel non-temporal noise divided by the average pixel voltage. The illumination source will be white light that has been IR filtered, producing a diffuse uniform illumination at the surface of the sensor package. The FPN will be calculated at coarse exposure settings of 0,10,150,250 and 302 with gain set to 1. 10 frames are grabbed and averaged to produce a temporally independent frame before each calculation. FPN will be expressed in mV.

4.5.5 Vertical Fixed Pattern Noise

VFPN describes the spatial noise in an image sensor related to patterns with a vertical orientation. The VFPN is defined as the standard deviation over all columns of the average pixel voltage for each column determined at zero exposure and zero illumination. VFPN will be expressed in mV.

4.5.6 Random Noise

Random noise is the temporal noise component within the image. Random noise will be expressed in mV.

4.5.7 Shading

This describes how average pixel values per “block” change across the image sensor array. For fine shading calculations the image sensor array is split into 30 pixel by 30 pixel blocks. An average value is then calculated for each block and the averages are then compared across the whole device. The blocks are increased in size to 60 pixels by 60 pixels for the gross shading calculation. Shading will be expressed in mV.

4.6 VV6411/VV6410 Power Consumption

Operating Condition	Current Consumption
Low power mode current consumption	c.6mA
Sleep mode current consumption[1]	c.18mA
Suspend mode current consumption (with CLKIP disabled)	<100uA
Normal operating mode current consumption[2]	<30mA

1. **Estimated figures - this parameter was not measured during final characterisation**
2. **Measured while device is clocked at 16MHz and streaming CIF video at 30fps**

4.7 VV6500 Power Consumption

Operating Condition	Current Consumption
Low power mode current consumption	c.8mA
Sleep mode current consumption[1]	c.18mA
Suspend mode current consumption (with CLKIP disabled)	<100uA
Normal operating mode current consumption[2]	<42mA

1. **Estimated figures - this parameter was not measured during final characterisation**
2. **Measured while device is clocked at 24MHz and streaming VGA video at 30fps**

Table 17 : VV6411/VV6410 Current consumption in different modes

4.8 Digital Input Pad Pull-Up and Pull-Down Strengths (VV6411/VV6410 and VV6500)

Pad Type	Pads	Min current	Max Current
Library pulldown	suspend	35µA	52µA
Library pullup	sclk, sda, oeb	25µA	42µA
Custom pullup	resetb	66µA	250µA

Table 18 : Pad Pull-up/Pull-down Strengths

5. Pinout and pin descriptions

5.1 VV6411/VV6410 Pin Details (36CLCC)

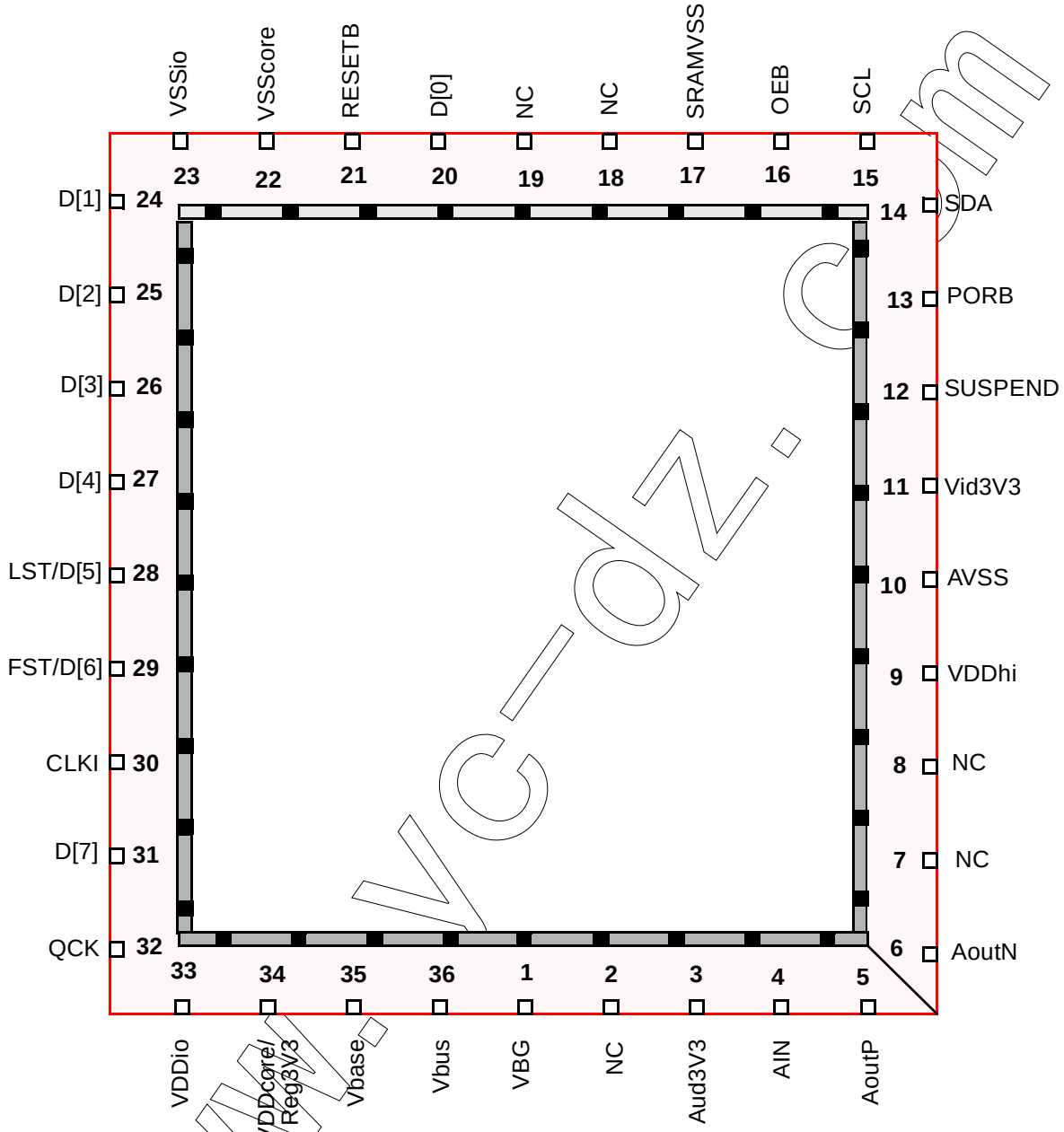


Figure 5 : 36 pin CLCC package pin assignment

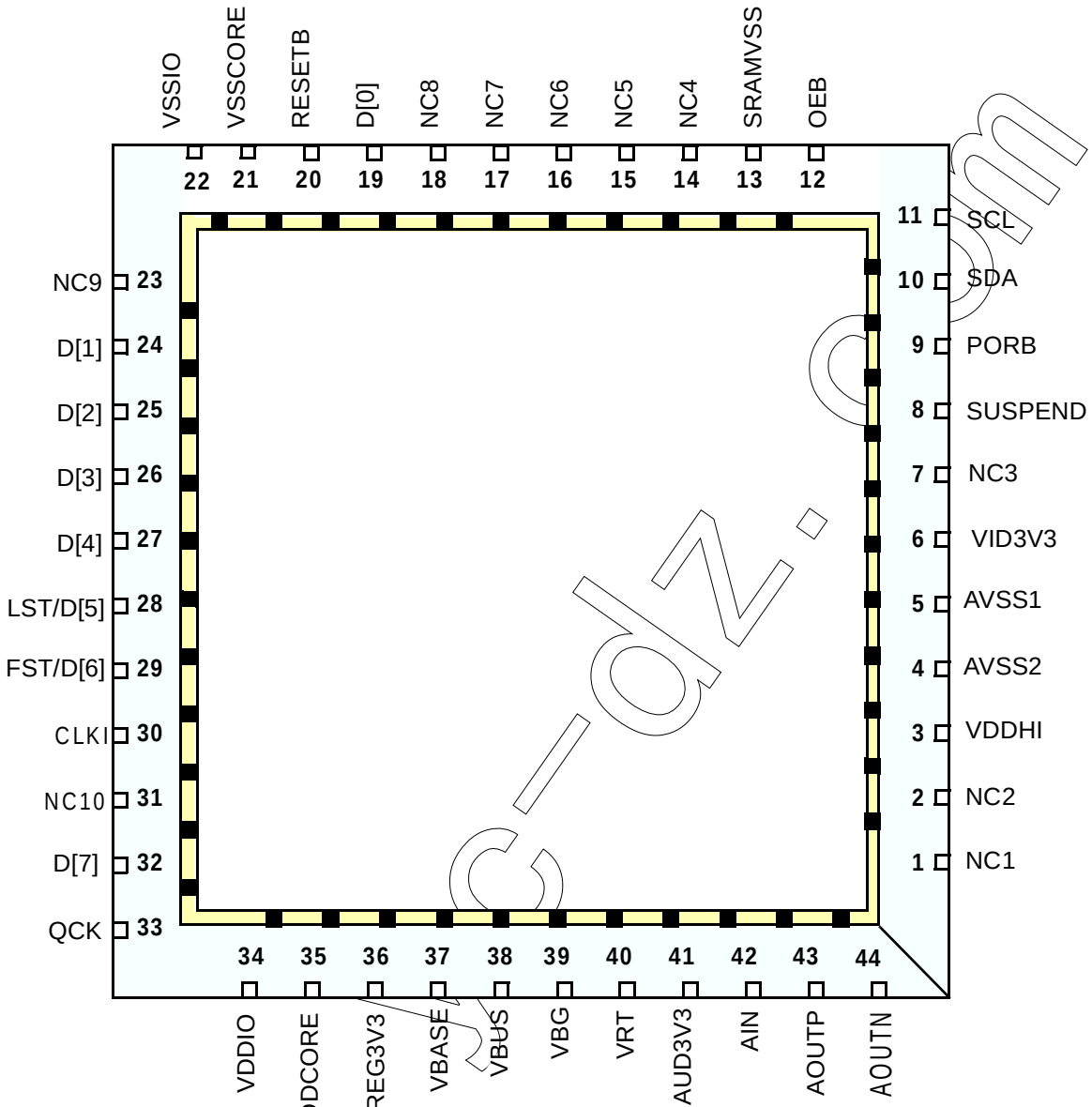
Name	Pin Number	Type	Description
POWER SUPPLIES			
AVSS	10	GND	Core analog ground and reference supplies.

Name	Pin Number	Type	Description
SRAMVSS	17	GND	In-column SRAM analog ground.
VDDcore/ Reg3V3	34	PWR	Digital logic power.
VDDio	33	PWR	Digital pad ring power.
VSScore	22	GND	Digital logic ground.
VSSio	23	GND	Digital pad ring ground.
Vid3V3	11	PWR	On-chip Video Supply Voltage Regulator Output
Aud3V3	3	PWR	On-chip Audio Amplifier Voltage Regulator Output
ANALOG SIGNALS			
VBG	1	OA	Internally generated bandgap reference voltage 1.22V
VDDHI	9	IA	Voltage doubler output, 4.6V -> 4.8V
VBase	35	OA	Drive for base of external bipolar
Vbus	36	IA	Incoming power supply
AIN	4	IA	Analog input to Audio Amplifier
AOutP	5	OA	Analog output of Audio Amplifier (positive)
AOutN	6	OA	Analog output of Audio Amplifier (negative)
PORB	13	OD	Power-on Reset (Bar) Output.
DIGITAL VIDEO INTERFACE			
D[4] D[3] D[2] D[1] D[0]	27 26 25 24 20	ODT	Tri-stateable 5-wire output data bus. - D[4] is the most significant bit. - D[4:0] have programmable drive strengths 2, 4 and 6 mA
QCK	32	ODT	Tri-stateable data qualification clock.
LST/D[5]	28	ODT	Tri-stateable Line start output May be configured as tri-stateable output data bit 5 D[5].
FST/D[6]	29	ODT	Tri-stateable Frame start signal. May be configured as tri-stateable output data bit 6 D[6].
D[7]	31	ODT	Tri-stateable Data wire (ms data bit). May be configured as tri-stateable output data bit 6 D[6].
OEB	16	ID↓	Digital output (tri-state) enable.
DIGITAL CONTROL SIGNALS			

Name	Pin Number	Type	Description
RESETB	21	ID↑	System Reset. Active Low. May be configured as System Sync. Active Low.
SUSPEND	12	ID↑	USB Suspend Mode Control signal. Active High If this feature is not required then the support circuit must pull the pin to ground. The combination of an active high signal and pull up pad was chosen to limit current drawn by the device while in suspend mode.
SERIAL INTERFACE			
SCL	15	BI↑	Serial bus clock (input only).
SDA	14	BI↑	Serial bus data (bidirectional, open drain).
SYSTEM CLOCKS			
CLKI	30	ID↓	Schmitt Buffered Clock input

Key			
A	Analog Input	D	Digital Input
OA	Analog Output	ID↑	Digital input with internal pull-up
BI	Bidirectional	ID↓	Digital input with internal pull-down
BI↑	Bidirectional with internal pull-up	OD	Digital Output
BI↓	Bidirectional with internal pull-down	ODT	Tri-stateable Digital Output

5.2 VV6411/VV6410 Pin Details (44OTQFP)



Name	Pin Number	Type	Description
POWER SUPPLIES			
AVSS2	4	GND	Core analog ground and reference supplies.
AVSS1	5	GND	Core analog ground and reference supplies.
SRAMVSS	13	GND	In-column SRAM analog ground.
VDDcore	35	PWR	Digital logic power.
Reg3V3	36	PWR	Digital logic power.
VDDio	34	PWR	Digital pad ring power.

Name	Pin Number	Type	Description
VSScore	21	GND	Digital logic ground.
VSSio	22	GND	Digital pad ring ground.
Vid3V3	6	PWR	On-chip Video Supply Voltage Regulator Output
Aud3V3	41	PWR	Audio regulator output
ANALOG SIGNALS			
VBG	39	OA	Internally generated bandgap reference voltage 1.22V
VDDHI	3	IA	Voltage doubler output, 4.6V -> 4.8V
VBase	37	OA	Drive for base of external bipolar
Vbus	38	IA	Incoming power supply 3.3 -> 6V
AIN	42	IA	Analog input to Audio Amplifier
AOutP	43	OA	Analog output of Audio Amplifier (positive)
AOutN	44	OA	Analog output of Audio Amplifier (negative)
PORB	9	OD	Power-on Reset (Bar) Output
DIGITAL VIDEO INTERFACE			
D[4] D[3] D[2] D[1] D[0]	27 26 25 24 19	ODT	Tri-stateable 5-wire output data bus. - D[4] is the most significant bit. - D[4:0] have programmable drive strengths 2, 4 and 6 mA
QCK	33	ODT	Tri-stateable data qualification clock.
LST/D[5]	28	ODT	Tri-stateable Line start output May be configured as tri-stateable output data bit 5 D[5].
FST/D[6]	29	ODT	Tri-stateable Frame start signal. May be configured as tri-stateable output data bit 6 D[6].
D[7]	32	ODT	Tri-stateable Data wire (ms data bit). May be configured as tri-stateable output data bit 6 D[6].
OEB	12	ID↓	Digital output (tri-state) enable.
DIGITAL CONTROL SIGNALS			
RESETB	20	ID↑	System Reset. Active Low. May be configured as System Sync. Active Low.
SUSPEND	8	ID↑	USB Suspend Mode Control signal. Active High If this feature is not required then the support circuit must pull the pin to ground. The combination of an active high signal and pull up pad was chosen to limit current drawn by the device while in suspend mode.

Name	Pin Number	Type	Description
SERIAL INTERFACE			
SCL	11	BI↑	Serial bus clock (input only).
SDA	10	BI↑	Serial bus data (bidirectional, open drain).
SYSTEM CLOCKS			
CLKI	30	ID↓	Schmitt Buffered Clock input

Key			
A	Analog Input	D	Digital Input
OA	Analog Output	ID↑	Digital input with internal pull-up
BI	Bidirectional	ID↓	Digital input with internal pull-down
BI↑	Bidirectional with internal pull-up	OD	Digital Output
BI↓	Bidirectional with internal pull-down	ODT	Tristateable Digital Output

5.3 VV6500 Pin Details

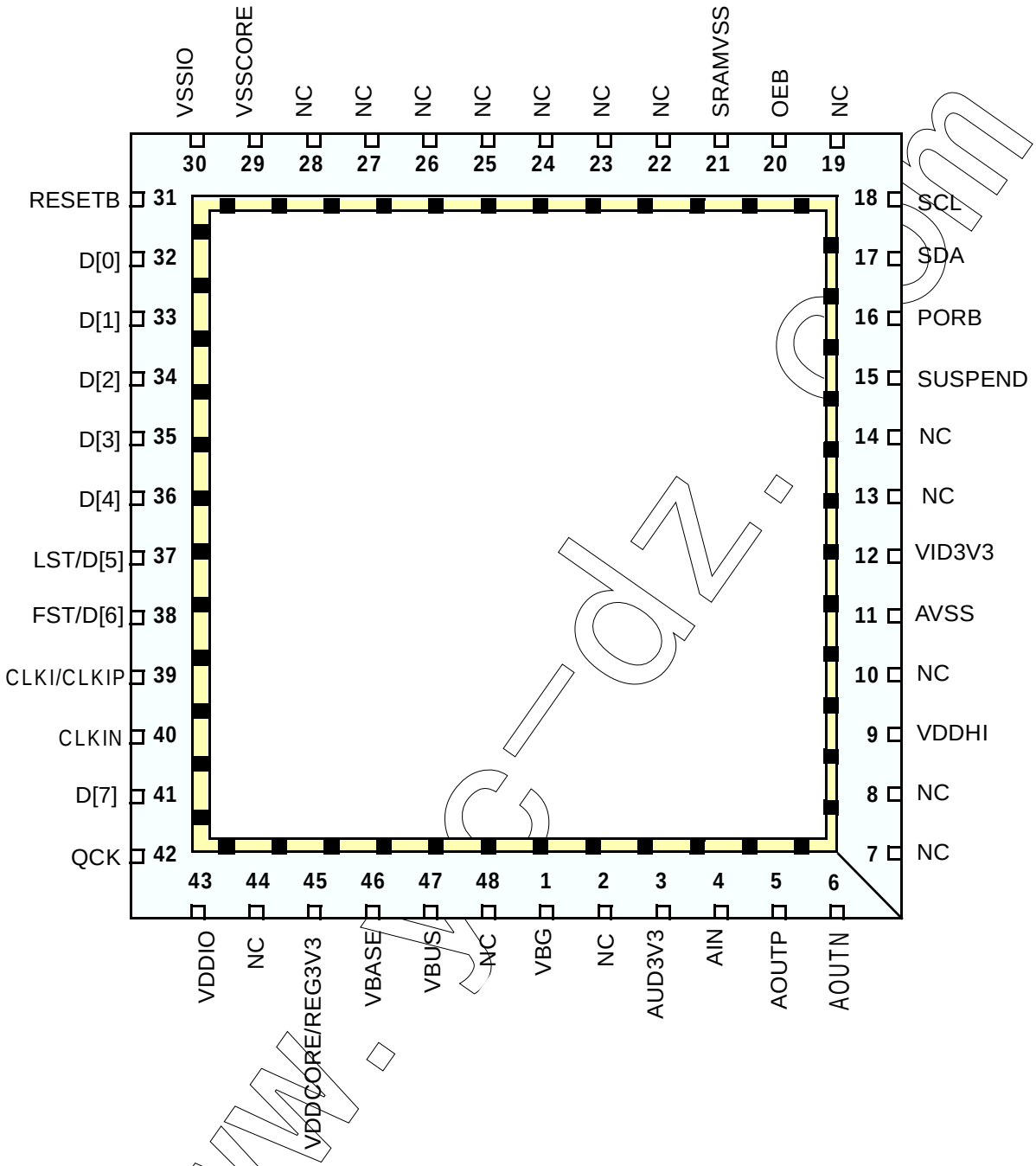


Figure 6 : 48 pin LCC package pin assignment

Name	Pin Number	Type	Description
POWER SUPPLIES			
AVSS	11	GND	Core analog ground and reference supplies.

Name	Pin Number	Type	Description
SRAMVSS	21	GND	In-column SRAM analog ground.
VDDIO	43	PWR	Digital pad ring power.
VSSCORE	29	GND	Digital logic ground.
VSSIO	30	GND	Digital pad ring ground.
SRAMVSS	21	GND	In-column SRAM analogue ground.
VDDCORE/ REG3V3	45	PWR	Digital logic power/Regulated 3V3 digital supply
ANALOG SIGNALS			
VBG	1	OA	Internally generated bandgap reference voltage 1.22V
AIN	4	IA	Analog input to Audio Amplifier
AOUTP	5	OA	Analog output of Audio Amplifier (positive)
AOUTN	6	OA	Analog output of Audio Amplifier (negative)
VDDHI	9	OA	Output from voltage doubler, 4.6V -> 4.8V
VBASE	46	OA	Drive for base of external bipolar
VBUS	47	IA	Incoming power supply 3.3V-> 6V
AUD3V3	3	PWR	On-chip Audio Amplifier Voltage Regulator Output
VID3V3	12	PWR	On-chip Video Supply Voltage Regulator Output
PORB	16	OA	Power-on Reset (Bar) Output.
DIGITAL VIDEO INTERFACE			
D[4] D[3] D[2] D[1] D[0]	36 35 34 33 32	ODT	Tri-stateable 5-wire output data bus. - D[4] is the most significant bit. - D[4:0] have programmable drive strengths 2, 4 and 6 mA
QCK	42	ODT	Tri-stateable data qualification clock.
LST/D[5]	37	ODT	Tri-stateable Line start output May be configured as tri-stateable output data bit 5 D[5].
FST/D[6]	38	ODT	Tri-stateable Frame start signal. May be configured as tri-stateable output data bit 6 D[6].
D[7]	41	ODT	Tri-stateable Data wire (ms data bit). May be configured as tri-stateable output data bit 6 D[6].
OEB	20	ID↓	Digital output (tri-state) enable.
DIGITAL CONTROL SIGNALS			

Name	Pin Number	Type	Description
RESETB	31	ID↑	System Reset. Active Low. May be configured as System Sync. Active Low.
SUSPEND	15	ID↑	USB Suspend Mode Control signal. Active High If this feature is not required then the support circuit must pull the pin to ground. The combination of an active high signal and pull up pad was chosen to limit current drawn by the device while in suspend mode.
SERIAL INTERFACE			
SCL	18	BI↑	Serial bus clock (input only).
SDA	17	BI↑	Serial bus data (bidirectional, open drain).
SYSTEM CLOCKS			
CLKI/CLKIP	39	ID↓	Schmitt Buffered Clock input or LVDS positive Clock input
CLKIN	40	BI↑	LVDS negative Clock input

Key			
A	Analog Input	D	Digital Input
OA	Analog Output	ID↑	Digital input with internal pull-up
BI	Bidirectional	ID↓	Digital input with internal pull-down
BI↑	Bidirectional with internal pull-up	OD	Digital Output
BI↓	Bidirectional with internal pull-down	ODT	Tri-stateable Digital Output

5.4 STV0676 Pin Details

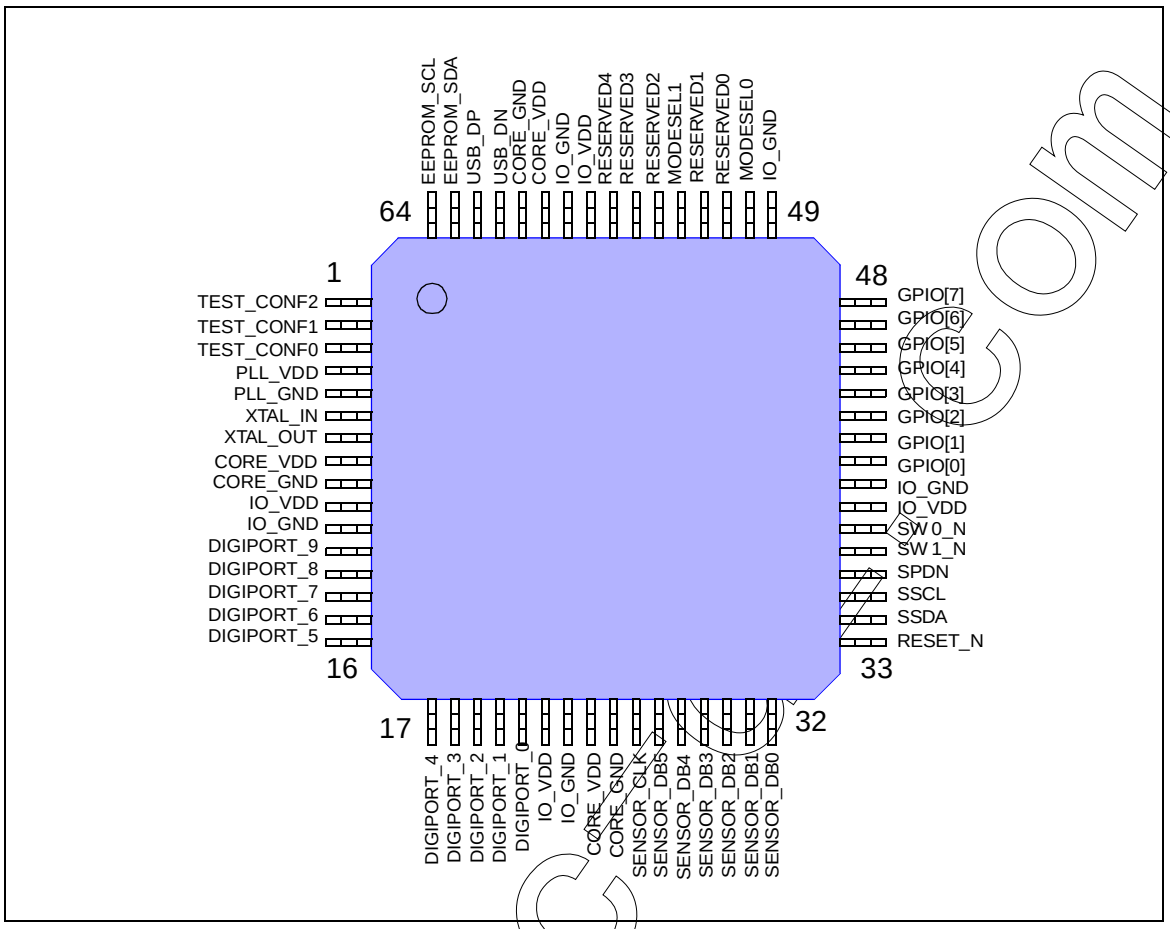


Figure 7 : STV0676 Pinout

Pin	Signal	Type	Description
POWER SUPPLIES			
1	TEST_CF0	INPUT	Test configuration bit - connect to VDD for normal operation
2	TEST_CF1	INPUT	Test configuration bit - connect to VDD for normal operation
3	TEST_CF2	INPUT	Test configuration bit - connect to VDD for normal operation
4	PLL_VDD	INPUT	VDD for internal phase locked loop
5	PLL_GND	INPUT	GND for internal phase locked loop
8	CORE_VDD	INPUT	VDD for core logic
9	CORE_VSS	INPUT	Ground for core logic
10	IO_VDD	INPUT	VDD for pad ring
11	IO_VSS	INPUT	Ground for pad ring
22	IO_VDD	INPUT	VDD for pad ring
23	IO_VSS	INPUT	Ground for pad ring

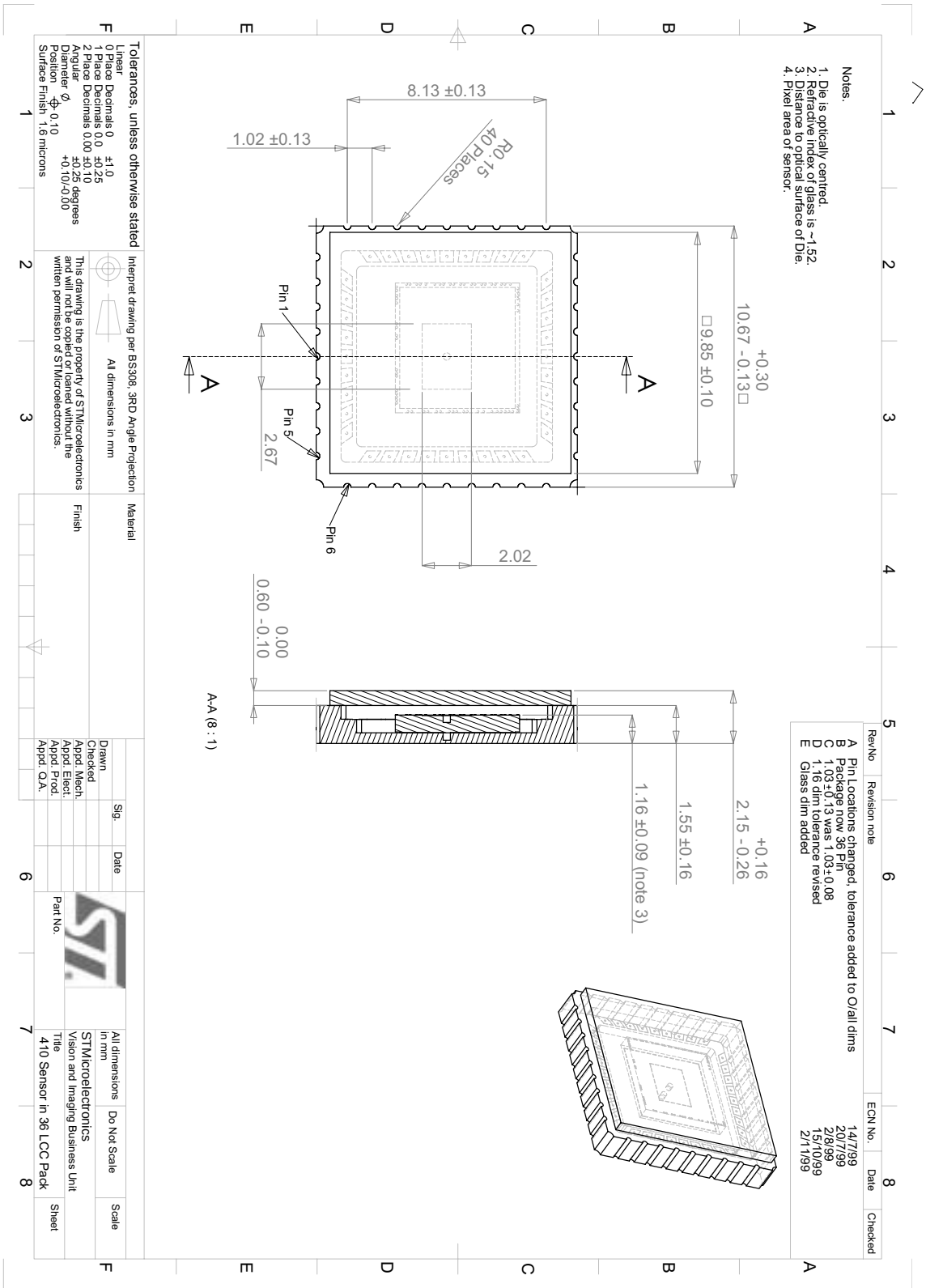
Pin	Signal	Type	Description
24	CORE_VDD	INPUT	VDD for core logic
25	CORE_VSS	INPUT	Ground for core logic
39	IO_VDD	INPUT	VDD for pad ring
40	IO_VSS	INPUT	Ground for pad ring
49	IO_VSS	INPUT	Ground for pad ring
57	CORE_VDD	INPUT	VDD for core logic
58	CORE_VSS	INPUT	Ground for core logic
59	IO_VDD	INPUT	VDD for pad ring
60	IO_VSS	INPUT	Ground for pad ring
DEVICE MASTER CLOCK AND RESET			
6	XTAL_IN	ANA	System clock pad
7	XTAL_OUT	OSC	System clock pad
33	RESET_N	SCHMITT	System, power-on-reset supplied by companion sensor
DIGIPORT/USB CONFIG INTERFACE[1]			
12	DIGIPORT_9[1]	BIDIR	Digiport operation
13	DIGIPORT_8[1]	BIDIR	Digiport operation
14	DIGIPORT_7[1]	BIDIR	Digiport operation /Programmable USB current consumption reported
15	DIGIPORT_6[1]	BIDIR	Digiport operation /Programmable USB current consumption reported
16	DIGIPORT_5[1]	BIDIR	Digiport operation /Programmable USB VID/PID
17	DIGIPORT_4[1]	BIDIR	Digiport operation /Programmable USB VID/PID
18	DIGIPORT_3[1]	BIDIR	Digiport operation /Programmable USB PID
19	DIGIPORT_2[1]	BIDIR	Digiport operation /Programmable USB PID
20	DIGIPORT_1[1]	BIDIR	Digiport operation /Programmable USB PID
21	DIGIPORT_0[1]	BIDIR	Digiport operation /Programmable USB PID
SENSOR INTERFACE			
26	SENSOR_CLK	BIDIR	VV6411/VV6410/VV6500 Sensor Clock
27	SENSOR_DB5	INPUT	VV6411/VV6410/VV6500 Sensor Data Bus [bit5]
28	SENSOR_DB4	INPUT	VV6411/VV6410/VV6500 Sensor Data Bus [bit4]
29	SENSOR_DB3	INPUT	VV6411/VV6410/VV6500 Sensor Data Bus [bit3]
30	SENSOR_DB2	INPUT	VV6411/VV6410/VV6500 Sensor Data Bus [bit2]
31	SENSOR_DB1	INPUT	VV6411/VV6410/VV6500 Sensor Data Bus [bit1]
32	SENSOR_DB0	INPUT	VV6411/VV6410/VV6500 Sensor Data Bus [bit0]
34	SSDA	3 state	VV6411/VV6410/VV6500 Sensor Serial Interface Data
35	SSCL	3 state	VV6411/VV6410/VV6500 Sensor Serial Interface Clock
36	SPDN	BIDIR	Control line to sensor to select ultra low power SUSPEND mode
MISC CONTROL			
37	$\overline{\text{SW 1}}$	INPUT	Remote wakeup
38	$\overline{\text{SW 0}}$	INPUT	Load TWAIN driver data upload
MICROPORT/GPIO INTERFACE			

Pin	Signal	Type	Description
41	GPIO[0]	BIDIR	General Purpose Input/Output
42	GPIO[1]	BIDIR	General Purpose Input/Output (GPIO)
43	GPIO[2]	BIDIR	General Purpose Input/Output (GPIO)
44	GPIO[3]	BIDIR	General Purpose Input/Output (GPIO)
45	GPIO[4]	BIDIR	General Purpose Input/Output (GPIO)
46	GPIO[5]	BIDIR	General Purpose Input/Output (GPIO)
47	GPIO[6]	BIDIR	General Purpose Input/Output (GPIO)
48	GPIO[7]	BIDIR	General Purpose Input/Output (GPIO)
50	MODESEL[0]	BIDIR	Along with ModeSel[1] used to configure I^2C interface and PID/VID selection. Please see Table 4 for further details
51	RESERVED[0]	BIDIR	Connect to VSS in reference design
52	RESERVED[1]	BIDIR	Connect to VDD in reference design
53	MODESEL[1]	BIDIR	Along with ModeSel[0] used to configure I^2C interface and PID/VID selection. Please see Table 4 for further details
54	RESERVED[2]	BIDIR	Connect to VDD in reference design
55	RESERVED3]	BIDIR	Connect to VSS in reference design
56	RESERVED[4]	BIDIR	Connect to VSS in reference design
USB INTERFACE			
61	USB_DN	BIDIR	USB data line
62	USB_DP	BIDIR	USB data line
EEPROM INTERFACE[2]			
63	EEPROM_SCL	OUTPUT	Serial clock to the EEPROM or slave I2C clock
64	EEPROM_SDA	BIDIR	Serial data to/from the EEPROM or slave I2C clock

1. **The DIGIPORT pins can be reconfigured, please contact STMicroelectronics for more details on this feature**
2. **The I^2C pins EEPROM_SCL and EEPROM_SDA can be reconfigured to act as a low speed I^2C slave device that allows the user to directly control the internal register space of the VP and VC modules.**

6. Package Details

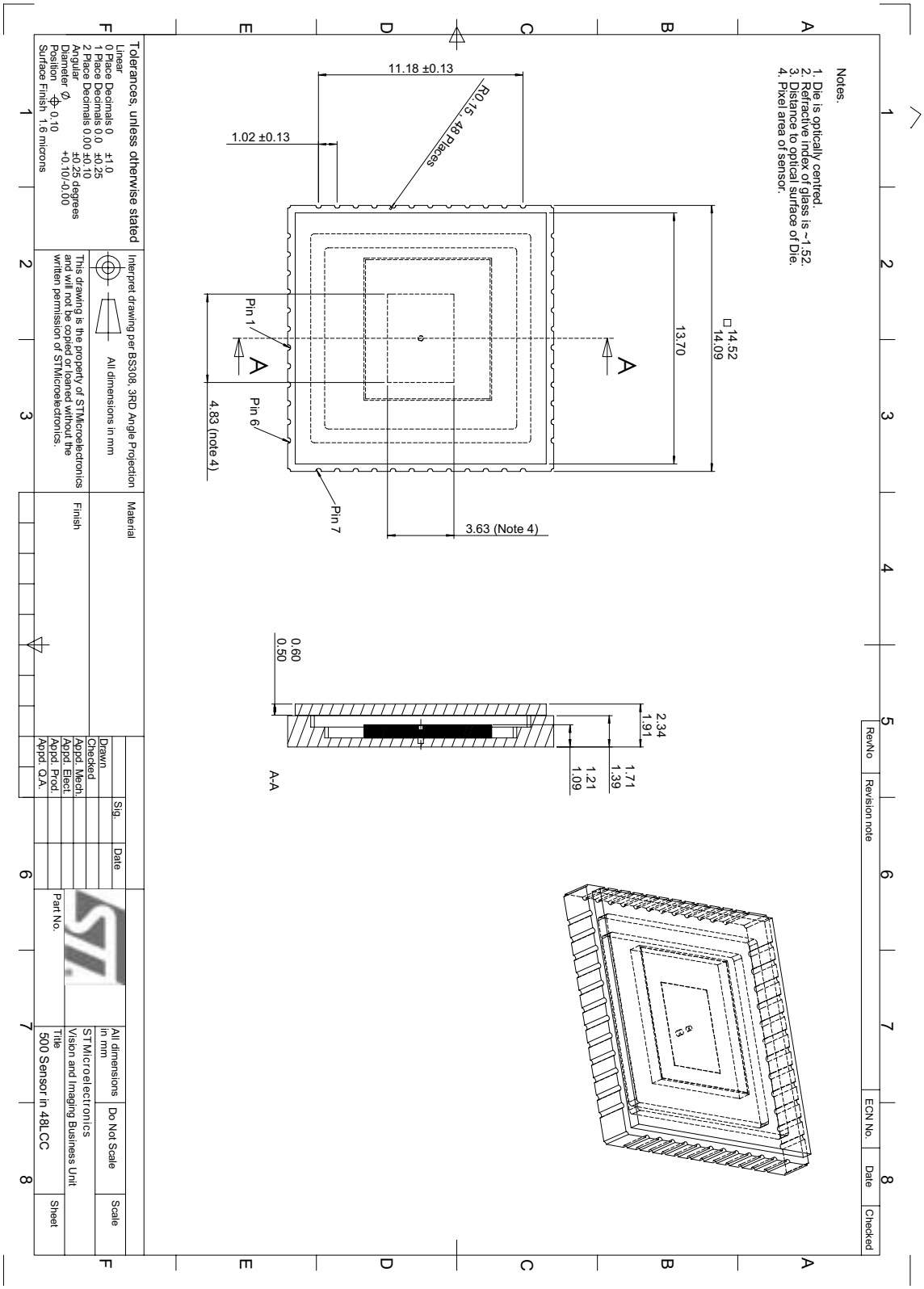
6.1 VV6411/V6410 (36pin CLCC)



6.2 VV6411/VV6410 (44pin OTQFP)

A package drawing for the 44pin OTQFP device will appear in a later version of this datasheet.

6.3 VV6500 (48pin CLCC)



6.4 STV0676 (64pin TQFP)

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.18	0.23	0.28	0.007	0.009	0.011
C	0.12	0.16	0.20	0.0047	0.0063	0.0079
D		12.00			0.472	
D1		10.00			0.394	
D3		7.50			0.295	
e		0.50			0.0197	
E		12.00			0.472	
E1		10.00			0.394	
E3		7.50			0.295	
H		5.89			0.232	
L	0.40	0.60	0.75	0.0157	0.0236	0.0295
L1		1.00			0.0393	
K	0° (min.), 7°(max.)					

OUTLINE AND MECHANICAL DATA

Body: 10 x 10 x 1.4mm

TQFP64

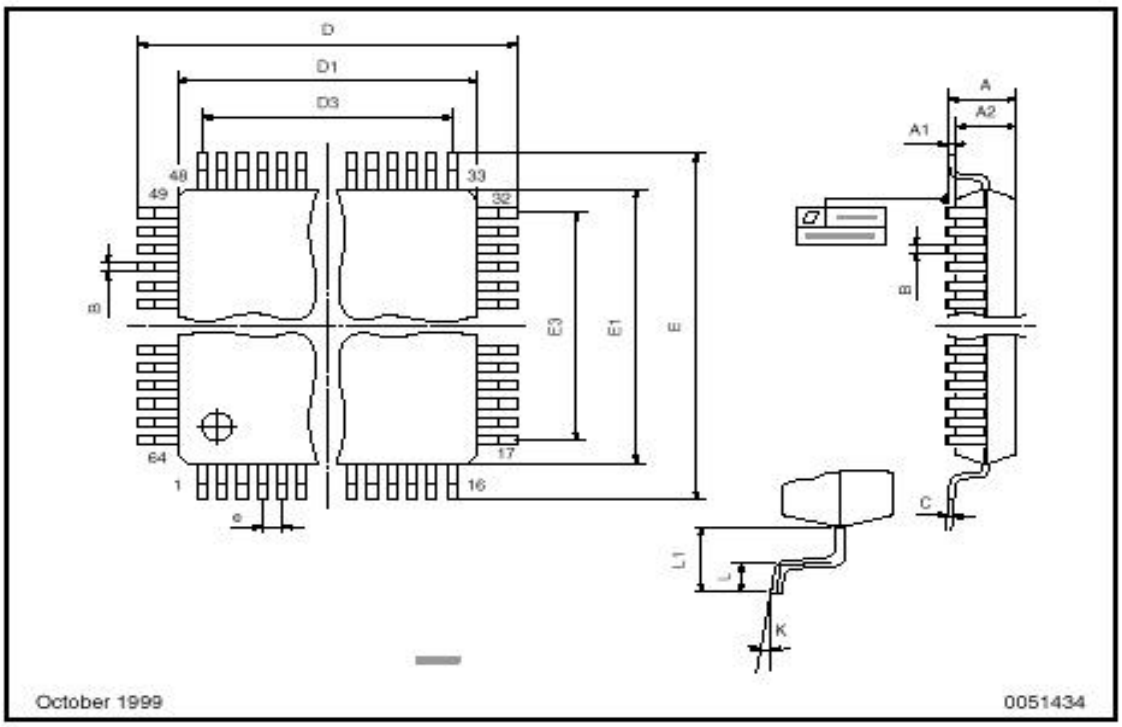
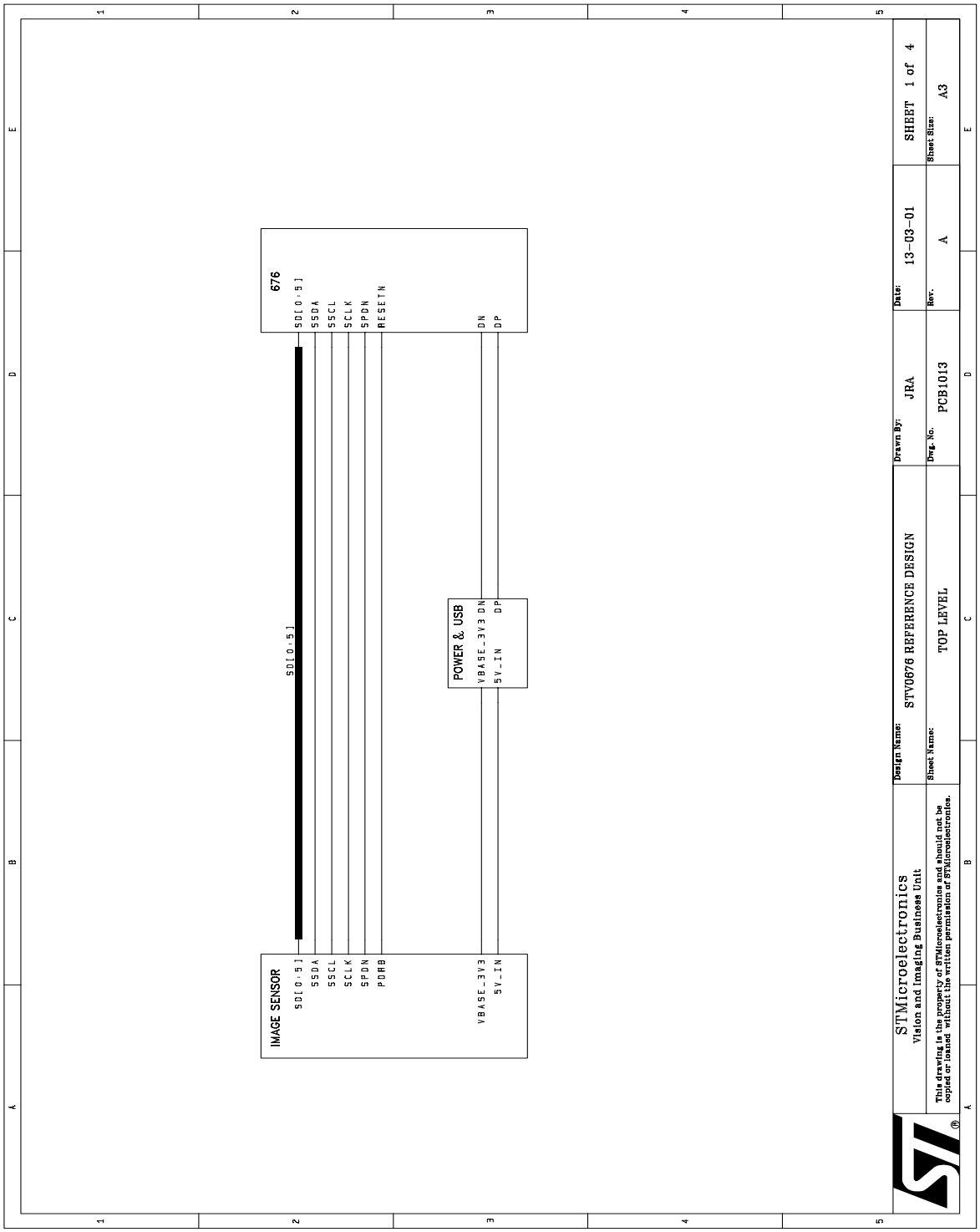


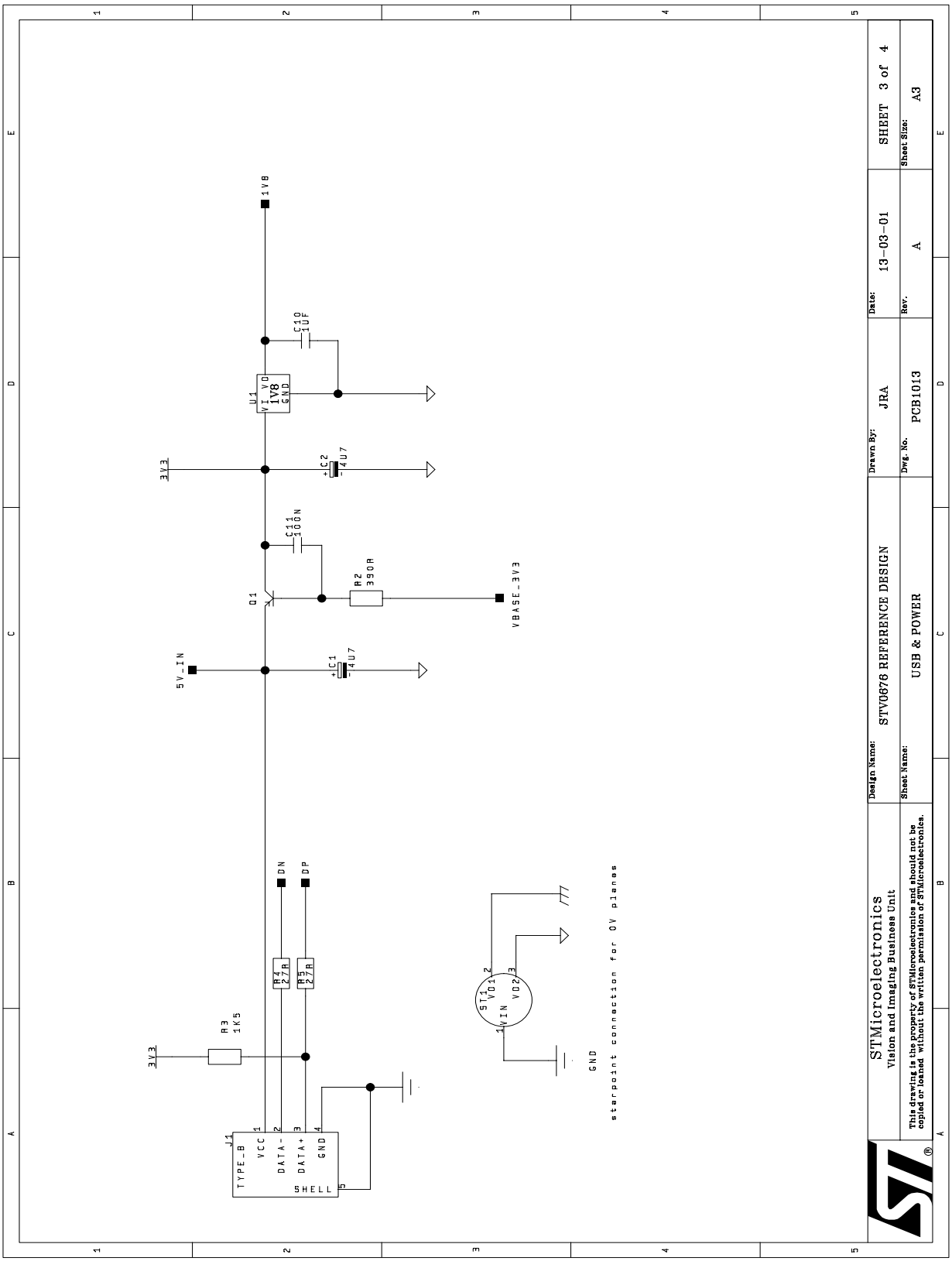
Figure 8 : STV0676 package details

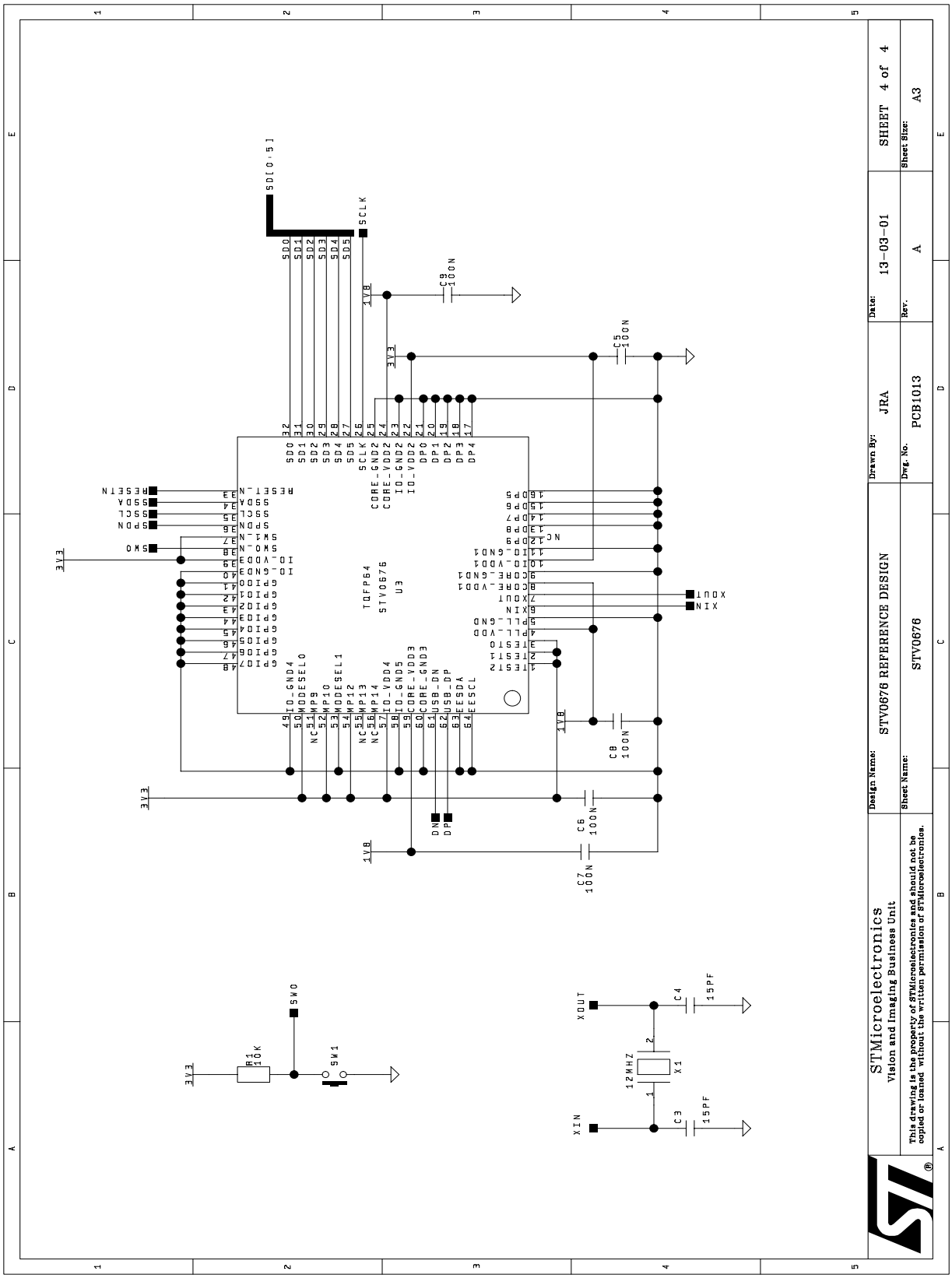
7. VV6411/V6410/VV6500+STV0676 Reference Design

STMicroelectronics will make a reference design available for the VV6411/VV6410/VV6500+STV0676 chipset. Contact STMicroelectronics for more details.

The schematic describing the reference design are included over the following 4 pages of the datasheet.







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southerneurope.imaging@st.com
ukeire.imaging@st.com
usa.imaging@st.com

8. Reference Design and Evaluation Kits (RDK's and EVK's)

STMicroelectronics supply a full range of supporting reference design kits for their range of sensors and coprocessors. The STV-USB /VGA-R (comprising the STV0676 coprocessor and the 6500 VGA resolution sensor) and STV-USB/CIF-R (comprising the STV0676 coprocessor and the 6411/6410 CIF resolution sensor) reference design kits allow direct interface to a PC via the USB port.

A full Evaluation Kit for the USB camera chipset will also be available in the future. Please contact STMicroelectronics for more details on this product.

Please contact STMicroelectronics for more details on how to order these support products.

9. Design Issues

The STV0676 has been designed utilising the most advanced video processor architecture available and has been fabricated with the latest 0.18µ HCMOS8 process.

STMicroelectronics will be mounting the STV0676 device “back to back” with an image sensor. Such a build was not recommended with the STV0672 device due to that devices relatively high power consumption affecting the image quality of the sensor. STMicroelectronics do not believe the power consumption of the STV0676 device will degrade the sensor image quality.

10. Ordering Details

For more information on the appropriate sensor choice please contact STMicroelectronics.

Part number	Description
VV6410C036	CIF image sensor, 36CLCC Package
VV6411C036	CIF image sensor, 36CLCC Package
TBD	CIF image sensor, 44 OTQFP Package
VV6500C001	VGA image sensor, 48CLCC Package
STV0676	Companion USB co-processor
STV-USB/CIF-R02	USB chipset, CIF resolution reference design kit
STV-USB/VGA-R02	USB chipset, VGA resolution reference design kit

Table 19 : Ordering details