Triacs logic level

BT131 series

GENERAL DESCRIPTION

Passivated, sensitive gate triacs in a plastic envelope, intended for use in general purpose bidirectional switching and phase control applications. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

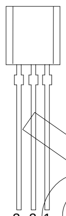
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BT131-	**600**	**800**	
V_{DRM}	Repetitive peak off-state voltages	600	800	V
$I_{T(RMS)}$	RMS on-state current	1	1	A
I_{TSM}	Non-repetitive peak on-state current	16	16	A

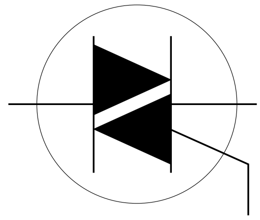
PINNING - TO92

PIN	DESCRIPTION
1	main terminal 2
2	gate
3	main terminal 1

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	MAX.	UNIT
				-600	**-800**	
V_{DRM}	Repetitive peak off-state voltages		-	600[1]	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{lead} \leq 74$ ˚C	-	1		A
I_{TSM}	Non-repetitive peak on-state current	full sine wave; $T_j = 25$ ˚C prior to surge				
		t = 20 ms	-	16		A
		t = 16.7 ms	-	17.6		A
I^2t	I^2t for fusing	t = 10 ms	-	1.28		A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 1.5$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs				
		T2+ G+	-	50		A/µs
		T2+ G-	-	50		A/µs
		T2- G-	-	50		A/µs
		T2- G+	-	10		A/µs
I_{GM}	Peak gate current		-	2		A
P_{GM}	Peak gate power		-	5		W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5		W
T_{stg}	Storage temperature		-40	150		˚C
T_j	Junction temperature		-	125		˚C

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 3 A/µs.

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}lead}$	Thermal resistance junction to lead	full cycle	-	-	60	K/W
		half cycle	-	-	80	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	pcb mounted;lead length = 4mm	-	150	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{GT}	Gate trigger current	V_D = 12 V; I_T = 0.1 A				
		T2+ G+	-	0.4	3	mA
		T2+ G-	-	1.3	3	mA
		T2- G-	-	1.4	3	mA
		T2- G+	-	3.8	7	mA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1 A				
		T2+ G+	-	1.2	5	mA
		T2+ G-	-	4.0	8	mA
		T2- G-	-	1.0	5	mA
		T2- G+	-	2.5	8	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.1 A	-	1.3	5	mA
V_T	On-state voltage	I_T = 2.0 A	-	1.2	1.5	V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A	-	0.7	1.5	V
		V_D = 400 V; I_T = 0.1 A; T_j = 125 ˚C	0.2	0.3	-	V
I_D	Off-state leakage current	$V_D = V_{DRM(max)}$; T_j = 125 ˚C	-	0.1	0.5	mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform; R_{GK} = 1 kΩ	5	15	-	V/μs
t_{gt}	Gate controlled turn-on time	I_{TM} = 1.5 A; $V_D = V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5 A/μs	-	2	-	μs

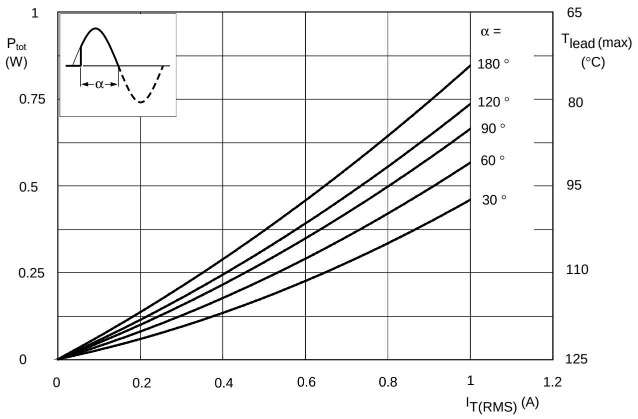


Fig.1. Maximum on-state dissipation, P_{tot}, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.

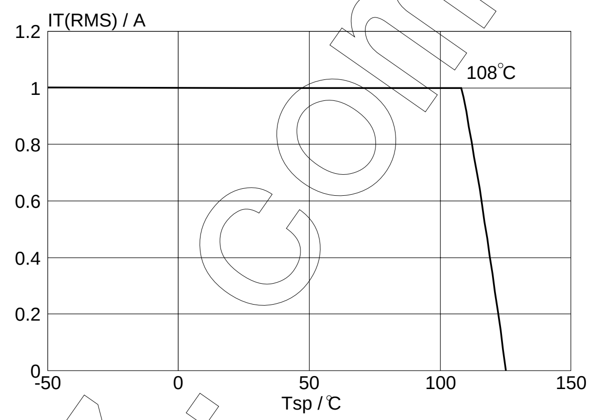


Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus lead temperature T_{lead}.

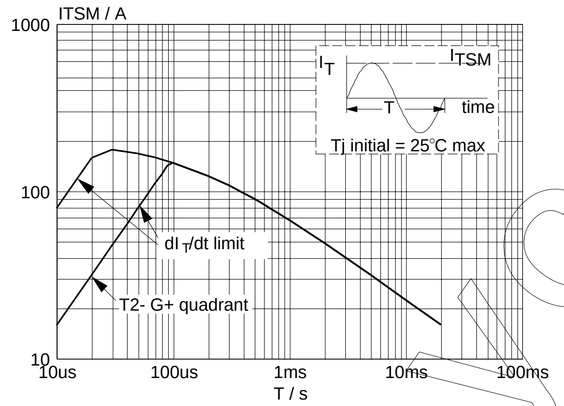


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq 20$ms.

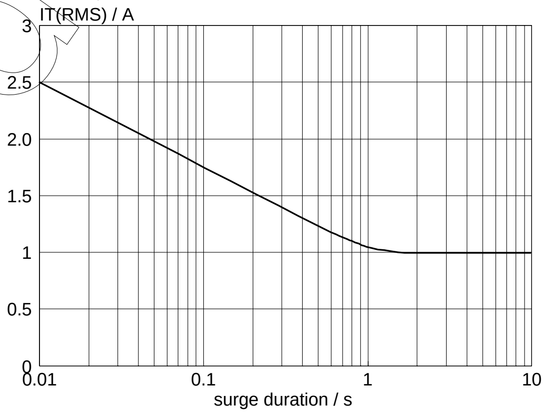


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{lead} \leq 51$°C.

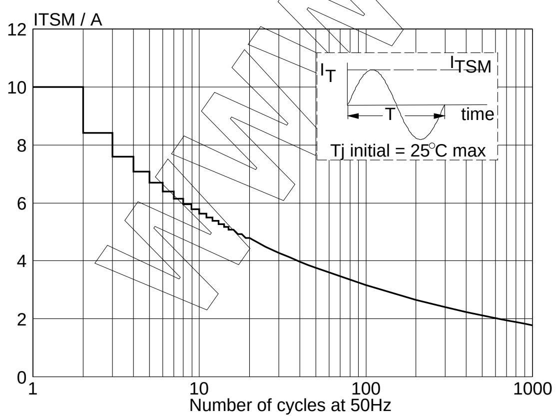


Fig.3. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

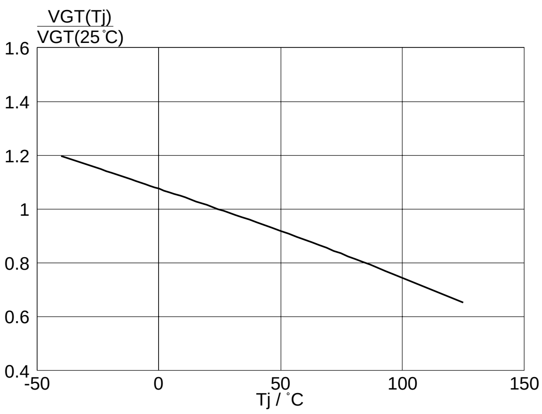


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)$/ V_{GT}(25°C), versus junction temperature T_j.

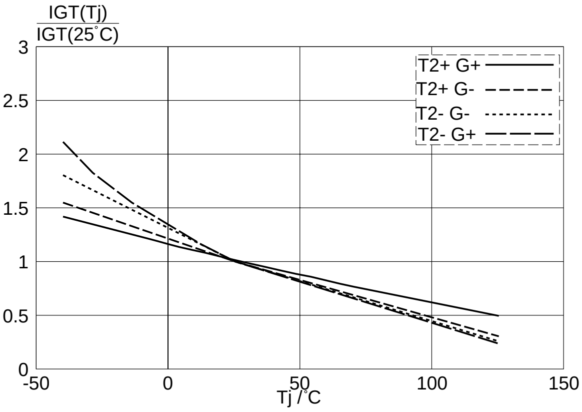


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25˚C)$, versus junction temperature T_j.

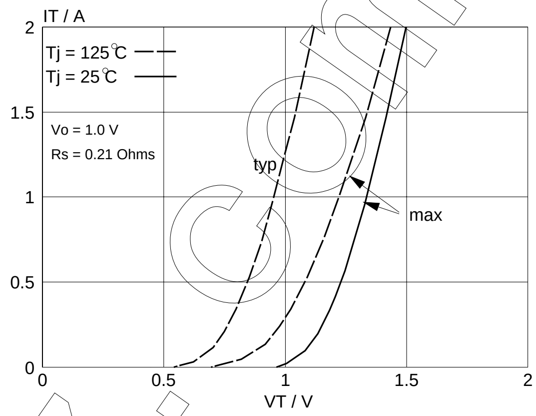


Fig.10. Typical and maximum on-state characteristic.

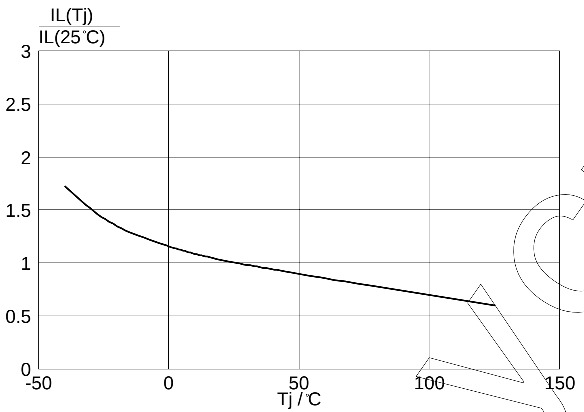


Fig.8. Normalised latching current $I_L(T_j)/ I_L(25˚C)$, versus junction temperature T_j.

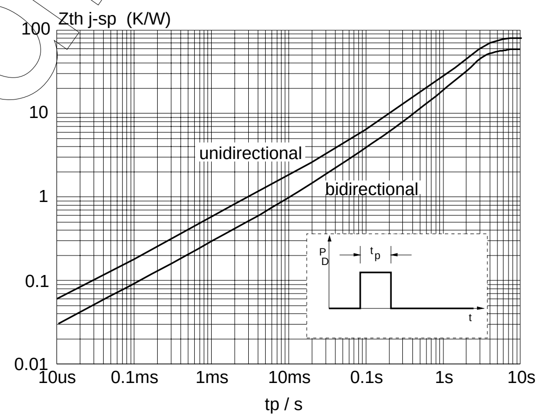


Fig.11. Transient thermal impedance $Z_{th\ j\text{-}lead}$, versus pulse width t_p.

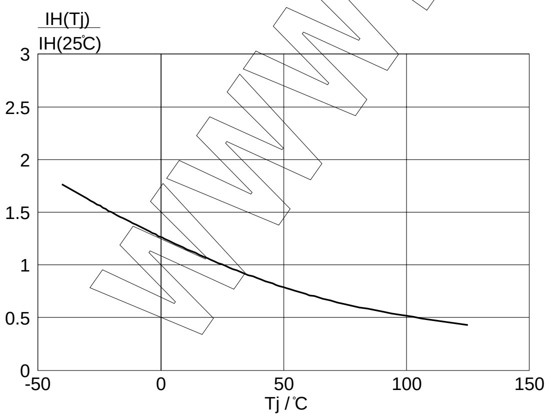


Fig.9. Normalised holding current $I_H(T_j)/ I_H(25˚C)$, versus junction temperature T_j.

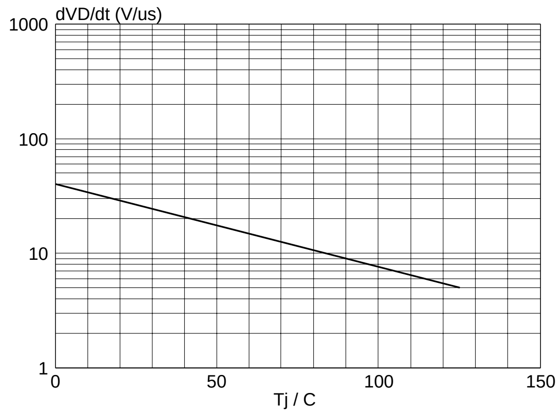
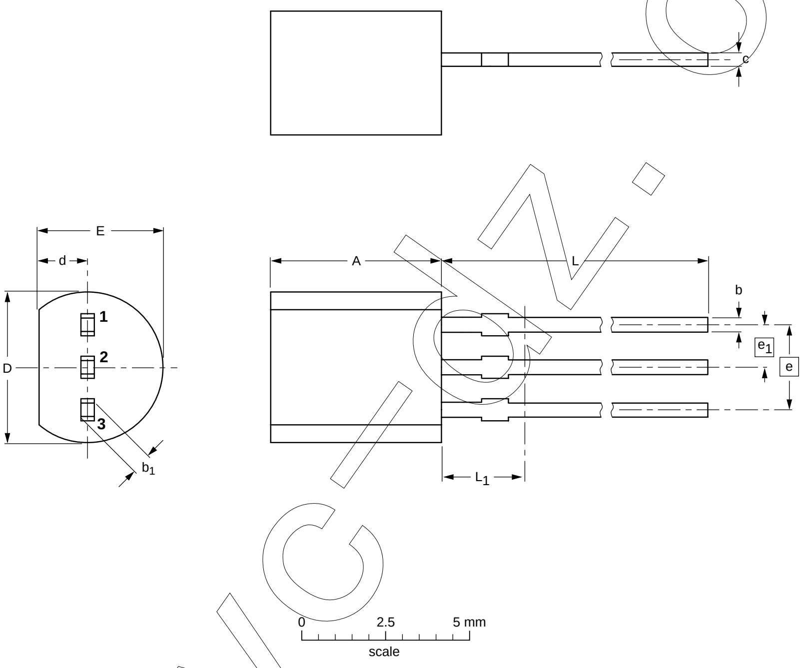


Fig.12. Typical, critical rate of rise of off-state voltage, dV_D/dt versus junction temperature T_j.

MECHANICAL DATA

Plastic single-ended leaded (through hole) package; 3 leads **SOT54**



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	b_1	c	D	d	E	e	e_1	L	$L_1^{(1)}$
mm	5.2 5.0	0.48 0.40	0.66 0.56	0.45 0.40	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5

Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT54		TO-92	SC-43			97-02-28

Fig.13. TO92 ; plastic envelope; Net Mass: 0.2 g

Notes

1. Epoxy meets UL94 V0 at 1/8".

DEFINITIONS

DATA SHEET STATUS		
DATA SHEET STATUS[2]	**PRODUCT STATUS**[3]	**DEFINITIONS**
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice
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Limiting values		
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.		
Application information		
Where application information is given, it is advisory and does not form part of the specification.		
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3 The product status of the device(s) described in this datasheet may have changed since this datasheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.