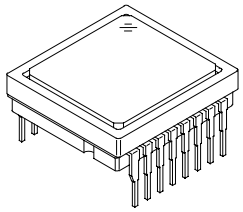
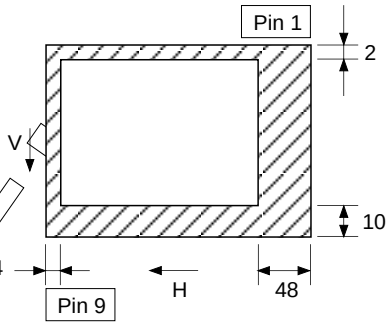
SONY

ICX284AQ

Diagonal 6.64mm (Type 1/2.7) Frame Readout CCD Image Sensor with Square Pixel for Color Cameras

16 pin DIP (Plastic)





Optical black position
(Top View)

Description

The ICX284AQ is a diagonal 6.64mm (Type 1/2.7) interline CCD solid-state image sensor with a square pixel array and 2.02M effective pixels. Frame readout allows all pixels' signals to be output independently within approximately 1/7.5 second. Also, the adoption of high frame rate readout mode supports 30 frames per second which is four times the speed in frame readout mode. This chip features an electronic shutter with variable charge-storage time. Adoption of a design specially suited for frame readout ensures a saturation signal level equivalent to when using field readout. High resolution and high color reproductivity are achieved through the use of R, G, B primary color mosaic filters. Further, high sensitivity and low dark current are achieved through the adoption of Super HAD CCD technology.

This chip is suitable for applications such as electronic still cameras, PC input cameras, etc.

Features

- Supports frame readout
- High horizontal and vertical resolution
- Supports high frame rate readout mode: 30 frames/s
- Square pixel
- Horizontal drive frequency: 18MHz
- No voltage adjustments (reset gate and substrate bias are not adjusted.)
- R, G, B primary color mosaic filters on chip
- High color reproductivity, high sensitivity, low smear
- Continuous variable-speed shutter
- Low dark current, excellent anti-blooming characteristics
- 16-pin high-precision plastic package (top/bottom dual surface reference possible)

Device Structure

- Interline CCD image sensor
- Image size: Diagonal 6.64mm (Type 1/2.7)
- Total number of pixels: 1688 (H) × 1248 (V) approx. 2.11M pixels
- Number of effective pixels: 1636 (H) × 1236 (V) approx. 2.02M pixels
- Number of active pixels: 1620 (H) × 1220 (V) approx. 1.98M pixels
- Chip size: 6.17mm (H) × 5.17mm (V)
- Unit cell size: 3.275µm (H) × 3.275µm (V)
- Optical black: Horizontal (H) direction: Front 4 pixels, rear 48 pixels
  Vertical (V) direction: Front 10 pixels, rear 2 pixels
- Number of dummy bits: Horizontal 28
  Vertical 1 (even fields only)
- Substrate material: Silicon

Super **HAD CCD** TM

*Super HAD CCD is a trademark of Sony Corporation. Super HAD CCD is a CCD that drastically improves sensitivity by introducing newly developed semiconductor technology by Sony Corporation into Sony's high-performance HAD (Hole-Accumulation Diode) sensor.

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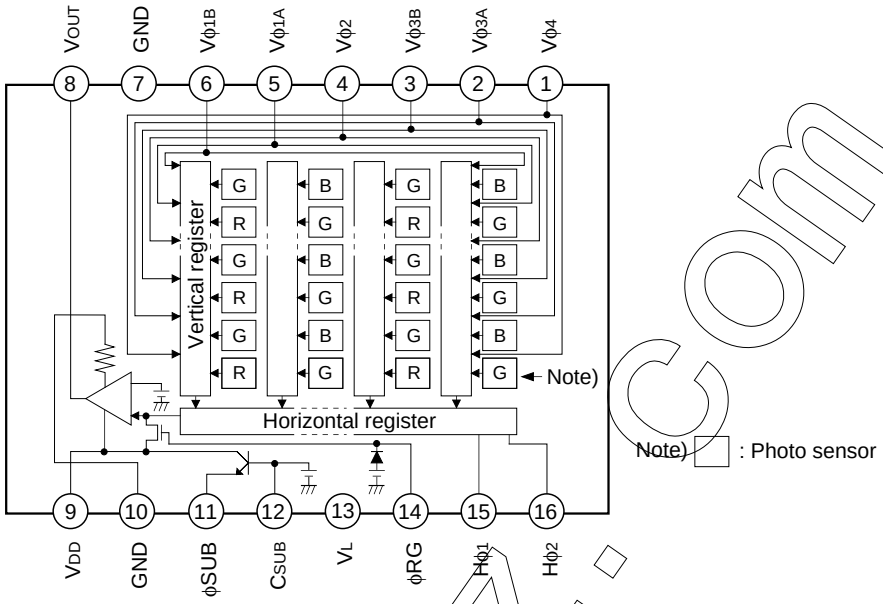
Block Diagram and Pin Configuration

(Top View)



Pin Description

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	Vφ4	Vertical register transfer clock	9	VDD	Supply voltage
2	Vφ3A	Vertical register transfer clock	10	GND	GND
3	Vφ3B	Vertical register transfer clock	11	φSUB	Substrate clock
4	Vφ2	Vertical register transfer clock	12	CSUB	Substrate bias*1
5	Vφ1A	Vertical register transfer clock	13	VL	Protective transistor bias
6	Vφ1B	Vertical register transfer clock	14	φRG	Reset gate clock
7	GND	GND	15	Hφ1	Horizontal register transfer clock
8	VOUT	Signal output	16	Hφ2	Horizontal register transfer clock

*1 DC bias is generated within the CCD, so that this pin should be grounded externally through a capacitance of 0.1µF.

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Absolute Maximum Ratings

Item		Ratings	Unit	Remarks
Against φSUB	V_{DD}, V_{OUT}, φRG – φSUB	–40 to +12	V	
	$V\phi_{1A}$, $V\phi_{1B}$, $V\phi_{3A}$, $V\phi_{3B}$ – φSUB	–50 to +15	V	
	$V\phi_2$, $V\phi_4$, V_L – φSUB	–50 to +0.3	V	
	$H\phi_1$, $H\phi_2$, GND – φSUB	–40 to +0.3	V	
	C_{SUB} – φSUB	–25 to	V	
Against GND	V_{DD}, V_{OUT}, φRG, C_{SUB} – GND	–0.3 to +22	V	
	$V\phi_{1A}$, $V\phi_{1B}$, $V\phi_2$, $V\phi_{3A}$, $V\phi_{3B}$, $V\phi_4$ – GND	–10 to +18	V	
	$H\phi_1$, $H\phi_2$ – GND	–10 to +6.5	V	
Against V_L	$V\phi_{1A}$, $V\phi_{1B}$, $V\phi_{3A}$, $V\phi_{3B}$ – V_L	–0.3 to +28	V	
	$V\phi_2$, $V\phi_4$, $H\phi_1$, $H\phi_2$, GND – V_L	–0.3 to +15	V	
Between input clock pins	Voltage difference between vertical clock input pins	to +15	V	*2
	$H\phi_1$ – $H\phi_2$	–6.5 to +6.5	V	
	$H\phi_1$, $H\phi_2$ – $V\phi_4$	–10 to +16	V	
Storage temperature		–30 to +80	°C	
Guaranteed temperature of performance		–10 to +60	°C	
Operating temperature		–10 to +75	°C	

*2 +24V (Max.) when clock width < 10µs, clock duty factor < 0.1%.
+16V (Max.) is guaranteed for turning on or off power supply.

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Bias Conditions

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply voltage	V_{DD}	14.55	15.0	15.45	V	
Protective transistor bias	V_L	*1				
Substrate clock	φSUB	*2				
Reset gate clock	φRG	*2				

*1 V_L setting is the V_{VL} voltage of the vertical transfer clock waveform, or the same voltage as the V_L power supply for the V driver should be used.

*2 Do not apply a DC bias to the substrate clock and reset gate clock pins, because a DC bias is generated within the CCD.

DC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply current	I_{DD}		6.5		mA	

Clock Voltage Conditions

Item	Symbol	Min.	Typ.	Max.	Unit	Waveform diagram	Remarks
Readout clock voltage	V_{VT}	14.55	15.0	15.45	V	1	
Vertical transfer clock voltage	V_{VH1}, V_{VH2}	–0.05	0	0.05	V	2	$V_{VH} = (V_{VH1} + V_{VH2})/2$
	V_{VH3}, V_{VH4}	–0.2	0	0.05	V	2	
	V_{VL1}, V_{VL2}, V_{VL3}, V_{VL4}	–8.0	–7.5	–7.0	V	2	$V_{VL} = (V_{VL3} + V_{VL4})/2$
	$V_{\phi V}$	6.8	7.5	8.05	V	2	$V_{\phi V} = V_{VHn} – V_{VLn}$ (n = 1 to 4)
	$V_{VH3} – V_{VH}$	–0.25		0.1	V	2	
	$V_{VH4} – V_{VH}$	–0.25		0.1	V	2	
	V_{VHH}			0.5	V	2	High-level coupling
	V_{VHL}			0.5	V	2	High-level coupling
	V_{VLH}			0.5	V	2	Low-level coupling
	V_{VLL}			0.5	V	2	Low-level coupling
Horizontal transfer clock voltage	$V_{\phi H}$	3.0	3.3	3.6	V	3	
	V_{HL}	–0.05	0	0.05	V	3	
	V_{CR}	0.5	1.65		V	3	Cross-point voltage
Reset gate clock voltage	$V_{\phi RG}$	3.0	3.3	3.6	V	4	
	$V_{RGLH} – V_{RGLL}$			0.4	V	4	Low-level coupling
	$V_{RGL} – V_{RGLm}$			0.5	V	4	Low-level coupling
Substrate clock voltage	$V_{\phi SUB}$	21.5	22.5	23.5	V	5	

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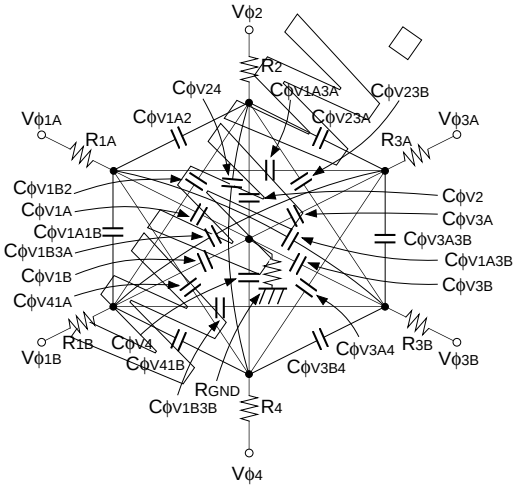
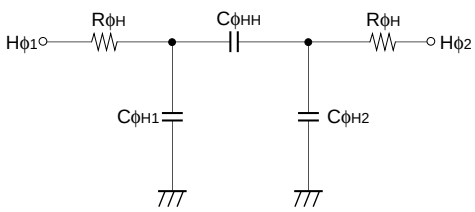
Clock Equivalent Circuit Constant

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Capacitance between vertical transfer clock and GND	$C_{\phi V1A}$, $C_{\phi V3A}$		390		pF	
	$C_{\phi V1B}$, $C_{\phi V3B}$		1200		pF	
	$C_{\phi V2}$, $C_{\phi V4}$		1500		pF	
Capacitance between vertical transfer clocks	$C_{\phi V1A2}$, $C_{\phi V3A4}$		120		pF	
	$C_{\phi V1B2}$, $C_{\phi V3B4}$		470		pF	
	$C_{\phi V23A}$, $C_{\phi V41A}$		62		pF	
	$C_{\phi V23B}$, $C_{\phi V41B}$		120		pF	
	$C_{\phi V1A3A}$		12		pF	
	$C_{\phi V1B3B}$		91		pF	
	$C_{\phi V1A3B}$, $C_{\phi V1B3A}$		30		pF	
	$C_{\phi V24}$		91		pF	
	$C_{\phi V1A1B}$, $C_{\phi V3A3B}$		30		pF	
Capacitance between horizontal transfer clock and GND	$C_{\phi H1}$		47		pF	
	$C_{\phi H2}$		47		pF	
Capacitance between horizontal transfer clocks	$C_{\phi HH}$		68		pF	
Capacitance between reset gate clock and GND	$C_{\phi RG}$		5		pF	
Capacitance between substrate clock and GND	$C_{\phi SUB}$		620		pF	
Vertical transfer clock series resistor	R_{1A}, R_{3A}		56		Ω	
	R_{1B}, R_{3B}		62		Ω	
	R_2, R_4		91		Ω	
Vertical transfer clock ground resistor	R_{GND}		18		Ω	
Horizontal transfer clock series resistor	$R_{\phi H}$		5		Ω	



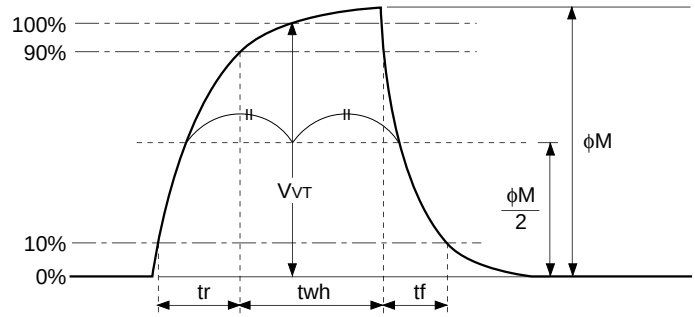
Vertical transfer clock equivalent circuit



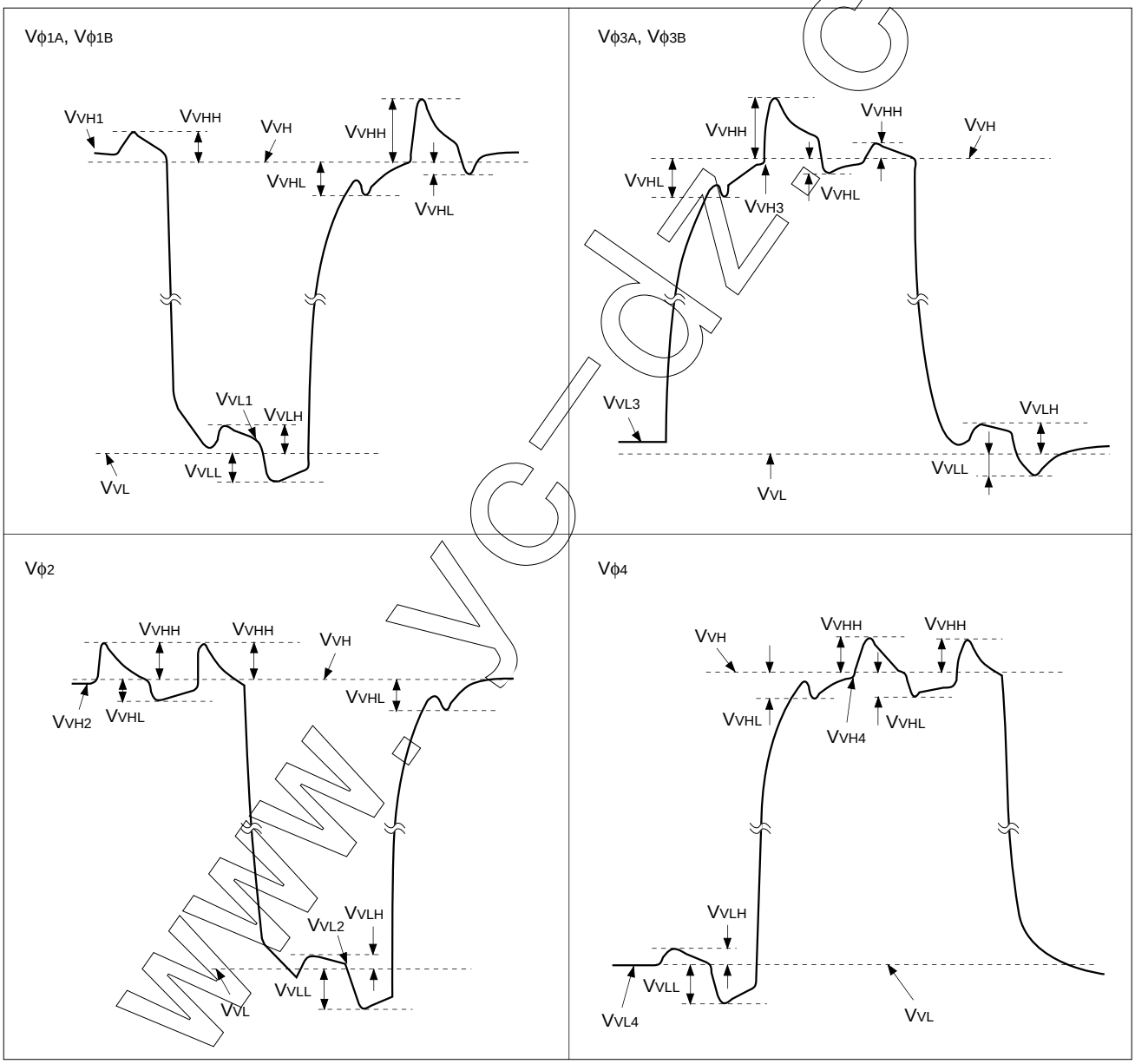
Horizontal transfer clock equivalent circuit

Drive Clock Waveform Conditions

(1) Readout clock waveform



(2) Vertical transfer clock waveform



$V_{VH} = (V_{VH1} + V_{VH2})/2$

$V_{VL} = (V_{VL3} + V_{VL4})/2$

$V_{\phi V} = V_{VHn} – V_{VLn}$ (n = 1 to 4)

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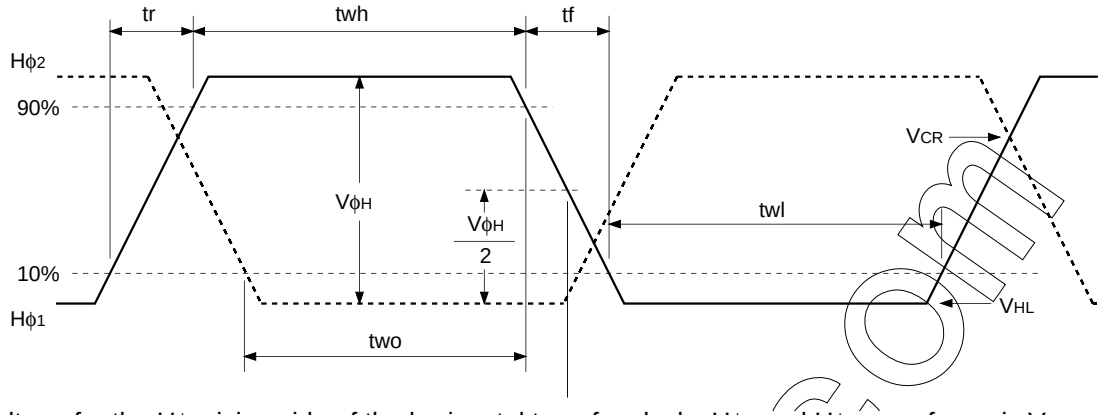
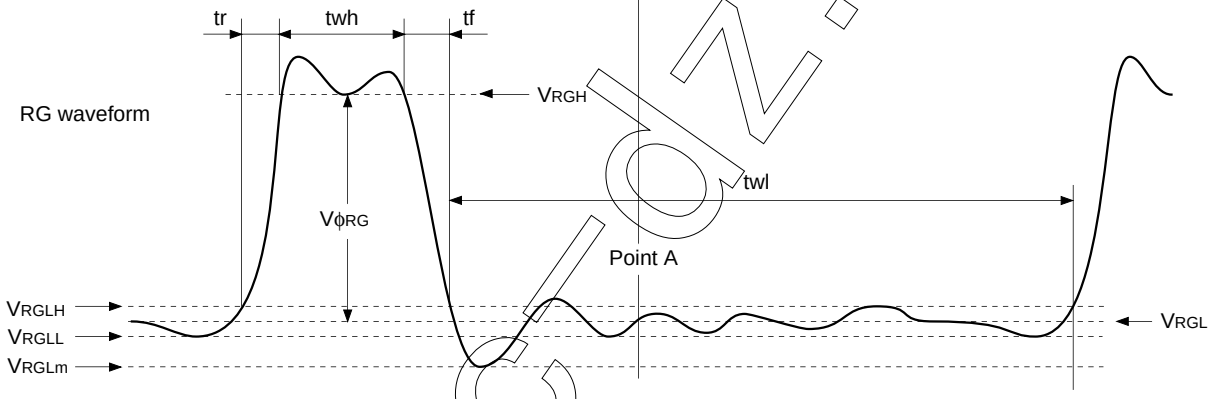
(3) Horizontal transfer clock waveform



Cross-point voltage for the Hϕ1 rising side of the horizontal transfer clocks Hϕ1 and Hϕ2 waveforms is VCR.
The overlap period for twh and twl of horizontal transfer clocks Hϕ1 and Hϕ2 is two.

(4) Reset gate clock waveform



VRGLH is the maximum value and VRGLL is the minimum value of the coupling waveform during the period from Point A in the above diagram until the rising edge of RG.
In addition, VRGL is the average value of VRGLH and VRGLL.

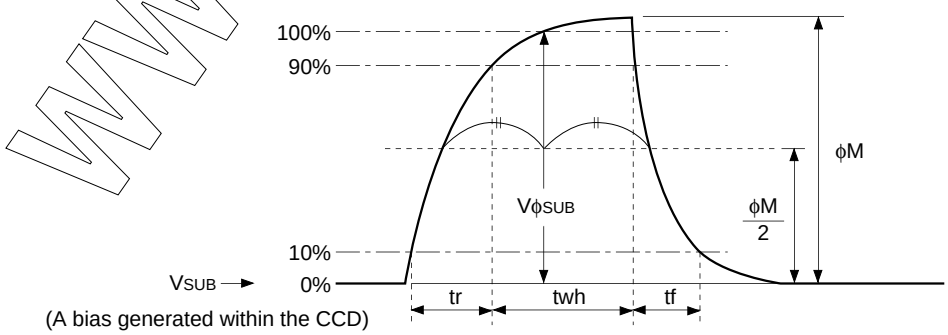
$$V_{RGL} = (V_{RGLH} + V_{RGLL})/2$$

Assuming VRGH is the minimum value during the interval twh, then:

$$V_{\phi RG} = V_{RGH} - V_{RGL}$$

Negative overshoot level during the falling edge of RG is VRGLm.

(5) Substrate clock waveform



(A bias generated within the CCD)

Clock Switching Characteristics (Horizontal drive frequency: 18MHz)

Item		Symbol	twh			twl			tr			tf			Unit	Remarks
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Readout clock		V_T	1.36	1.56						0.5			0.5		µs	During readout
Vertical transfer clock		$V\phi_{1A}$, $V\phi_{1B}$, $V\phi_2$, $V\phi_{3A}$, $V\phi_{3B}$, $V\phi_4$										15		250	ns	When using CXD1267AN
Horizontal transfer clock	During imaging	$H\phi_1$	14	19.5		14	19.5			8.5	14		8.5	14	ns	tf ≥ tr – 2ns
		$H\phi_2$	14	19.5		14	19.5			8.5	14		8.5	14		
	During parallel-serial conversion	$H\phi_1$		5.56						0.01			0.01		µs	
		$H\phi_2$					5.56			0.01			0.01			
Reset gate clock		ϕ_{RG}	7	10			37			4			5		ns	
Substrate clock		ϕ_{SUB}	1.7	3.6							0.5			0.5	µs	During drain charge

Item	Symbol	two			Unit	Remarks
		Min.	Typ.	Max.		
Horizontal transfer clock	$H\phi_1$, $H\phi_2$	12	19.5		ns	

Spectral Sensitivity Characteristics (excludes lens characteristics and light source characteristics)

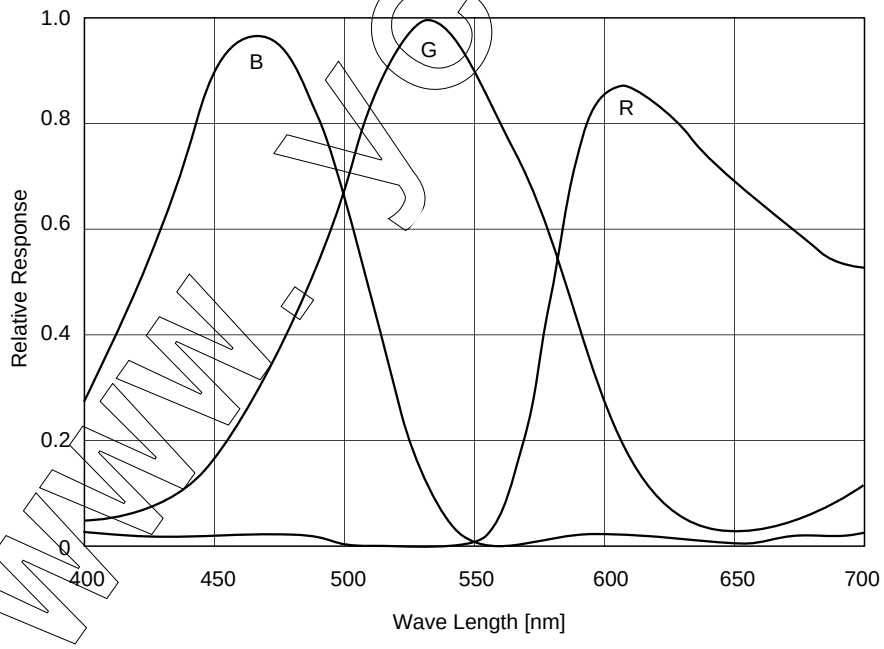


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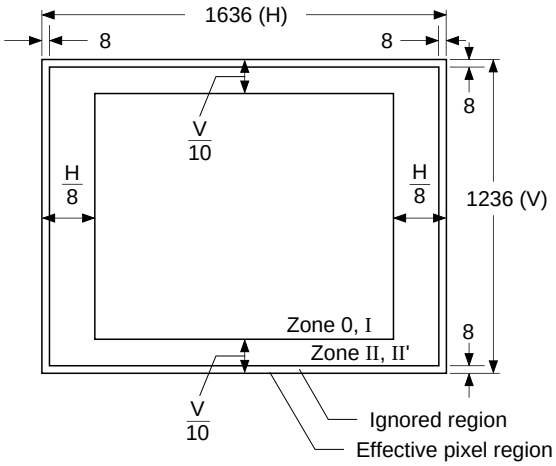
Image Sensor Characteristics (Ta = 25°C)

Item		Symbol	Min.	Typ.	Max.	Unit	Measurement method	Remarks
G sensitivity		Sg	175	220		mV	1	1/30s accumulation
Sensitivity comparison	R	Rr	0.33		0.59		1	
	B	Rb	0.43		0.7		1	
Saturation signal		Vsat	420			mV	2	Ta = 60°C
Smear		Sm		–90	–80	dB	3	Frame readout mode*1
				–78	–68			High frame rate readout mode
Video signal shading		SHg			20	%	4	Zone 0 and I
					25	%	4	Zone 0 to II'
Dark signal		Vdt			8	mV	5	Ta = 60°C, 7.5 frame/s
Dark signal shading		ΔVdt			4	mV	6	Ta = 60°C, 7.5 frame/s,*2
Line crawl G		Lcg			3.8	%	7	
Line crawl R		Lcr			3.8	%	7	
Line crawl B		Lcb			3.8	%	7	
Lag		Lag			0.5	%	8	

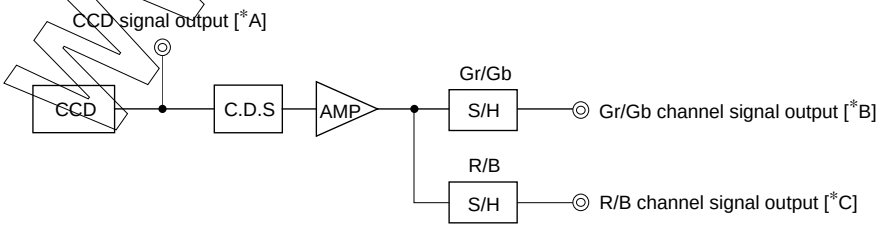
*1 After closing the mechanical shutter, the smear can be reduced to below the detection limit by performing vertical register sweep operation.

*2 Excludes vertical dark signal shading caused by vertical register high-speed transfer.

Zone Definition of Video Signal Shading



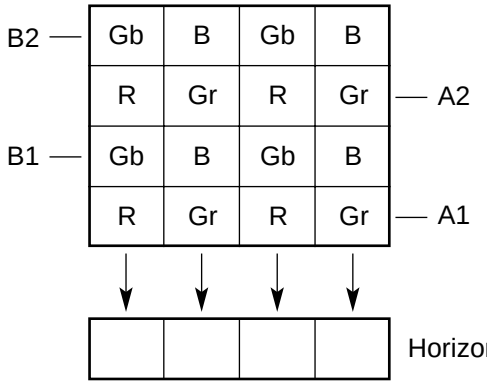
Measurement System



Note) Adjust the amplifier gain so that the gain between [*A] and [*B], and between [*A] and [*C] equals 1.

Image Sensor Characteristics Measurement Method

◎ **Color coding of this image sensor & Readout**

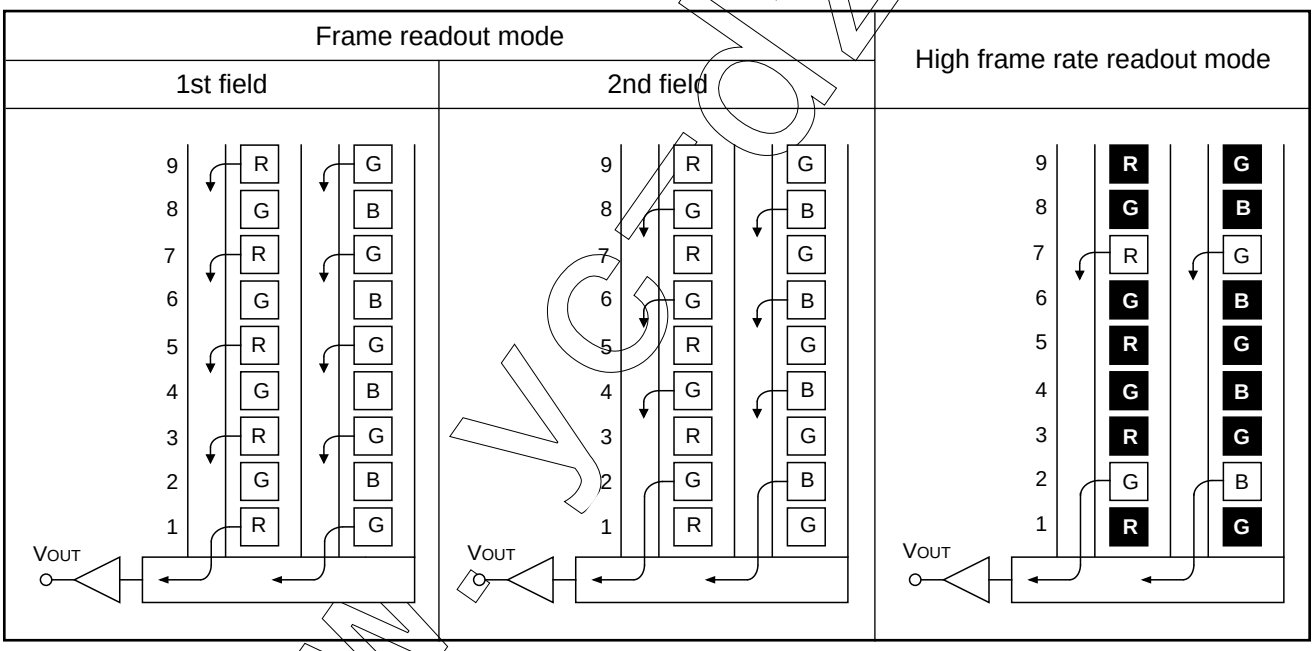


Color Coding Diagram

The primary color filters of this image sensor are arranged in the layout shown in the figure on the left (Bayer arrangement).
Gr and Gb denote the G signals on the same line as the R signal and the B signal, respectively.
For frame readout, the A1 and A2 lines are output as signals in the A field, and the B1 and B2 lines in the B field.

◎ **Readout modes**

The diagram below shows the output methods for the following two readout modes.



Note) Blacked out portions in the diagram indicate pixels which are not read out.
Output starts from the line 5 in high frame rate readout mode.

1. Frame readout mode
   In this mode, all pixel signals are divided into two fields and output.
   All pixel signals are read out independently, making this mode suitable for high resolution image capturing.

2. High frame rate readout mode
   All effective area signals are output in 1/4 the period for frame readout mode by reading out two lines for every eight lines. The number of output lines is 309 lines.
   This readout mode emphasizes processing speed over vertical resolution.

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◎ **Measurement conditions**

1) In the following measurements, the device drive conditions are at the typical values of the bias and clock voltage conditions, and the frame readout mode is used.

2) In the following measurements, spot blemishes are excluded and, unless otherwise specified, the optical black level (OB) is used as the reference for the signal output, which is taken as the value of the Gr/Gb channel signal output or the R/B channel signal output of the measurement system.

◎ **Definition of standard imaging conditions**

1) Standard imaging condition I:
Use a pattern box (luminance: 706cd/m^2, color temperature of 3200K halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t = 1.0mm) as an IR cut filter and image at F5.6. The luminous intensity to the sensor receiving surface at this point is defined as the standard sensitivity testing luminous intensity.

2) Standard imaging condition II:
Image a light source (color temperature of 3200K) with a uniformity of brightness within 2% at all angles. Use a testing standard lens with CM500S (t = 1.0mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

3) Standard imaging condition III:
Image a light source (color temperature of 3200K) with a uniformity of brightness within 2% at all angles. Use a testing standard lens (exit pupil distance –33mm) with CM500S (t = 1.0mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

1. G sensitivity, sensitivity comparison
Set to standard imaging condition I. After selecting the electronic shutter mode with a shutter speed of 1/100s, measure the signal outputs (V_{Gr}, V_{Gb}, V_R and V_B) at the center of each Gr, Gb, R and B channel screen, and substitute the values into the following formulas.

$V_G = (V_{Gr} + V_{Gb})/2$
$Sg = V_G \times 100/30$ [mV]
$Rr = V_R/V_G$
$Rb = V_B/V_G$

2. Saturation signal
Set to standard imaging condition II. After adjusting the luminous intensity to 20 times the intensity with the average value of the Gr signal output, 150mV, measure the minimum values of the Gr, Gb, R and B signal outputs.

3. Smear
Set to standard imaging condition II. With the lens diaphragm at F5.6 to F8, first adjust the average value of the Gr signal output to 150mV. Measure the average values of the Gr signal output, Gb signal output, R signal output and B signal output (Gra, Gba, Ra, Ba), and then adjust the luminous intensity to 500 times the intensity with the average value of the Gr signal output, 150mV. After the readout clock is stopped and the charge drain is executed by the electronic shutter at the respective H blankings, measure the maximum value (V_{Sm} [mV]) independent of the Gr, Gb, R and B signal outputs, and substitute the values into the following formula.

$$Sm = 20 \times \log \left(Vsm \div \frac{Gra + Gba + Ra + Ba}{4} \times \frac{1}{500} \times \frac{1}{10} \right) \text{ [dB] (1/10V method conversion value)}$$

4. Video signal shading
   Set to standard imaging condition III. With the lens diaphragm at F5.6 to F8, adjust the luminous intensity so that the average value of the Gr signal output is 150mV. Then measure the maximum (Grmax [mV]) and minimum (Grmin [mV]) values of the Gr signal output and substitute the values into the following formula.

   $SHg = (Grmax - Grmin)/150 \times 100$ [%]

5. Dark signal
   Measure the average value of the signal output (Vdt [mV]) with the device ambient temperature 60°C and the device in the light-obstructed state, using the horizontal idle transfer level as a reference.

6. Dark signal shading
   After measuring 5, measure the maximum (Vdmax [mV]) and minimum (Vdmin [mV]) values of the dark signal output and substitute the values into the following formula.

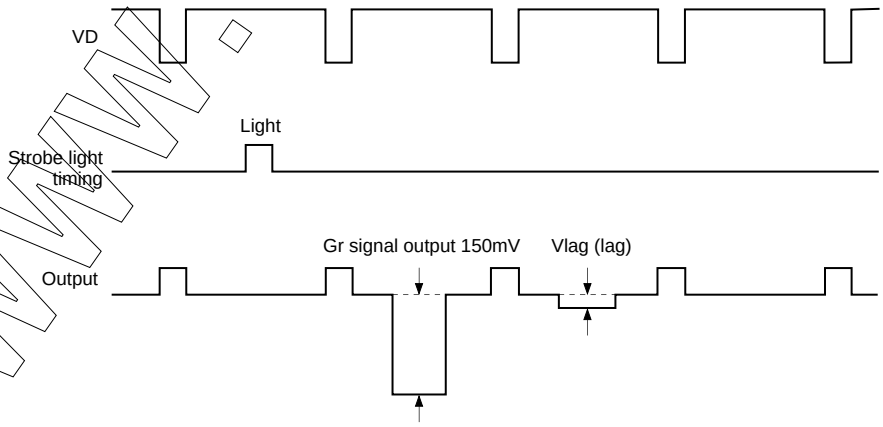
   $\Delta Vdt = Vdmax - Vdmin$ [mV]

7. Line crawl
   Set to standard imaging condition II. Adjusting the luminous intensity so that the average value of the Gr signal output is 150mV, and then insert R, G and B filters and measure the difference between G signal lines (ΔGlr, ΔGlg, ΔGlb [mV]) as well as the average value of the G signal output (Gar, Gag, Gab). Substitute the values into the following formula.

   $Lci = \Delta Gli/Gai \times 100$ [%] (i = r, g, b)

8. Lag
   Adjust the Gr signal output value generated by strobe light to 150mV. After setting the strobe light so that it strobes with the following timing, measure the residual signal (Vlag). Substitute the value into the following formula.

   $Lag = (Vlag/150) \times 100$ [%]



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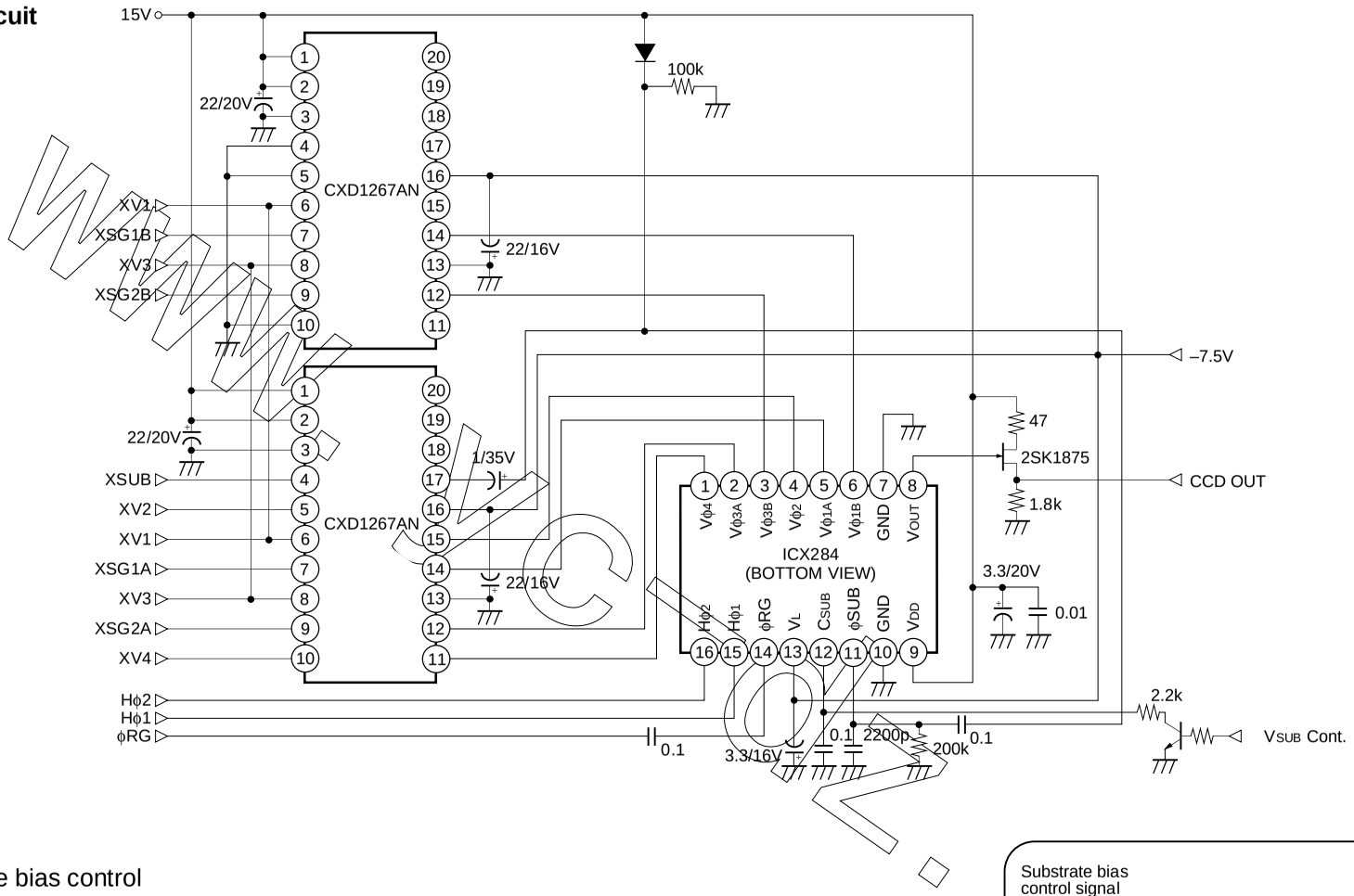
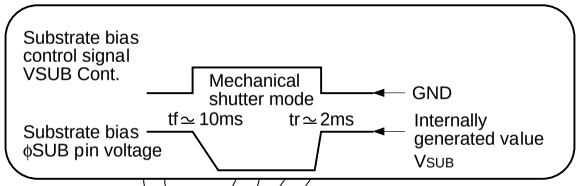
Drive Circuit



Notes)

Substrate bias control

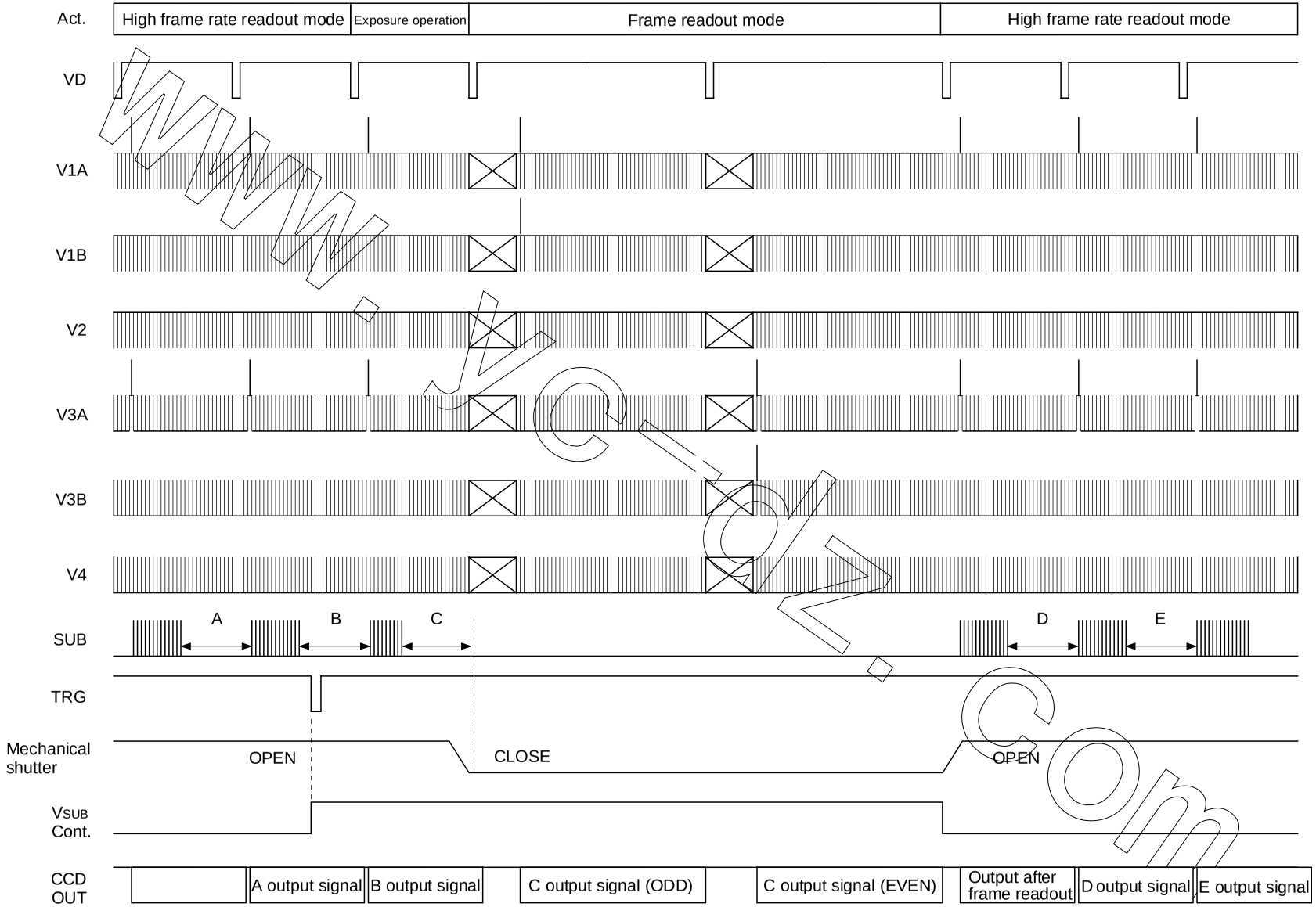
1. The saturation signal level decreases when exposure is performed using the mechanical shutter, so control the substrate bias.
2. A saturation signal level equivalent to that for continuous exposure can be assured by connecting a 2.2kΩ grounding resistor to the CCD C_{SUB} pin.



Drive timing precautions

1. Blooming occurs in modes (monitoring, etc.) that do not use the mechanical shutter, so do not ground the connected 2.2kΩ resistor.
2. tf is slow, so the internally generated voltage V_{SUB} may not drop to a sufficiently low level if the substrate bias control signal is not set to high level 20ms before entering the exposure period and the 2.2kΩ resistor connected to the C_{SUB} pin is not grounded.
3. The blooming signal generated during exposure in mechanical shutter mode is swept by providing one field or more of idle transfer through vertical register high-speed sweep transfer from the time the mechanical shutter closes until sensor readout is performed. However, note that the V_L potential and the φSUB pin DC voltage sag at this time.

Drive Timing Chart (Vertical Sequence) High Frame Rate Readout Mode → Frame Readout Mode/Electronic Shutter Normal Operation



Note) The B output signal contains a blooming component and should therefore not be used.

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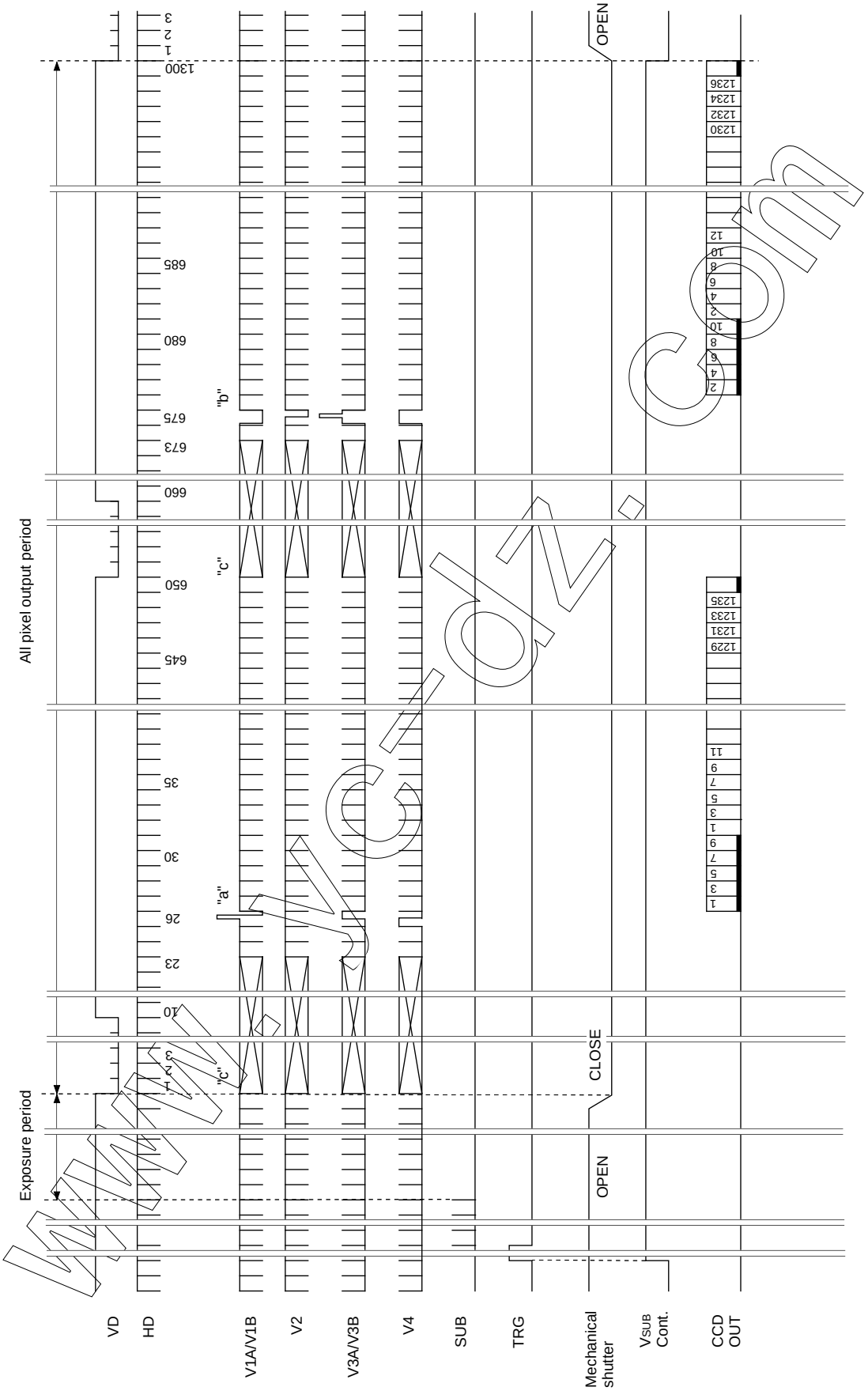
Drive Timing Chart (Vertical Sync) Frame Readout Mode



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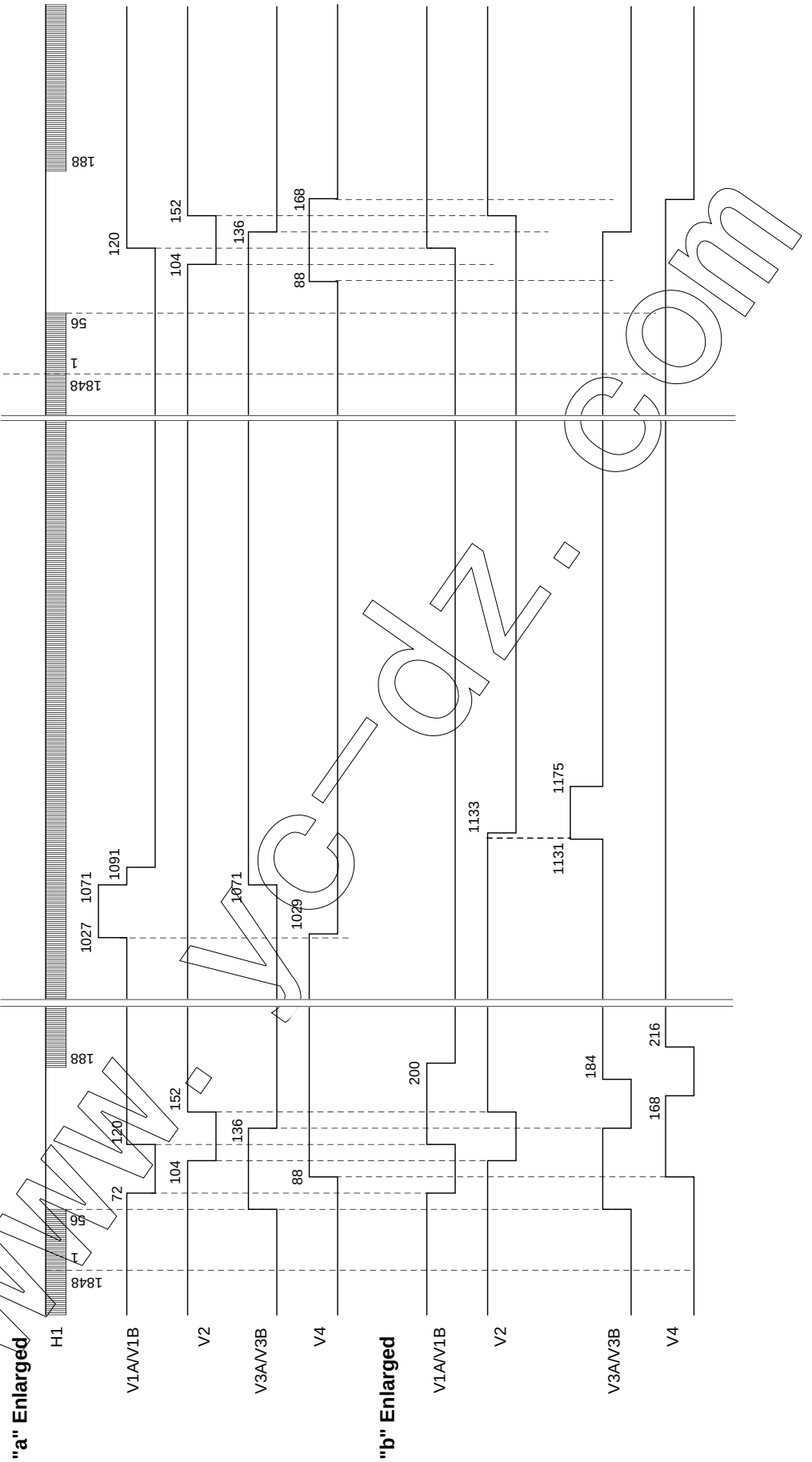
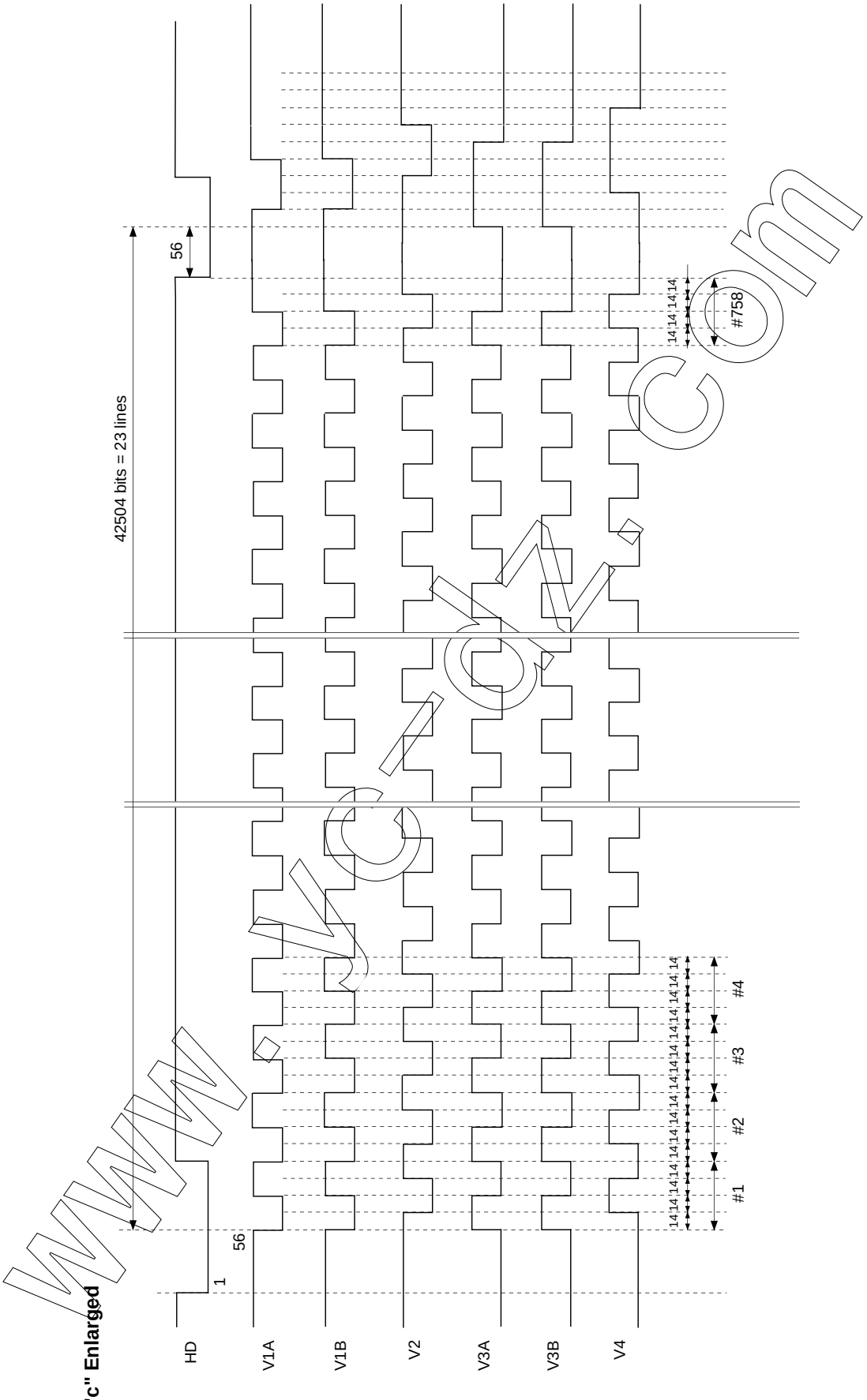
Drive Timing Chart (Vertical Sync) Frame Readout Mode



www.vc-dz.com

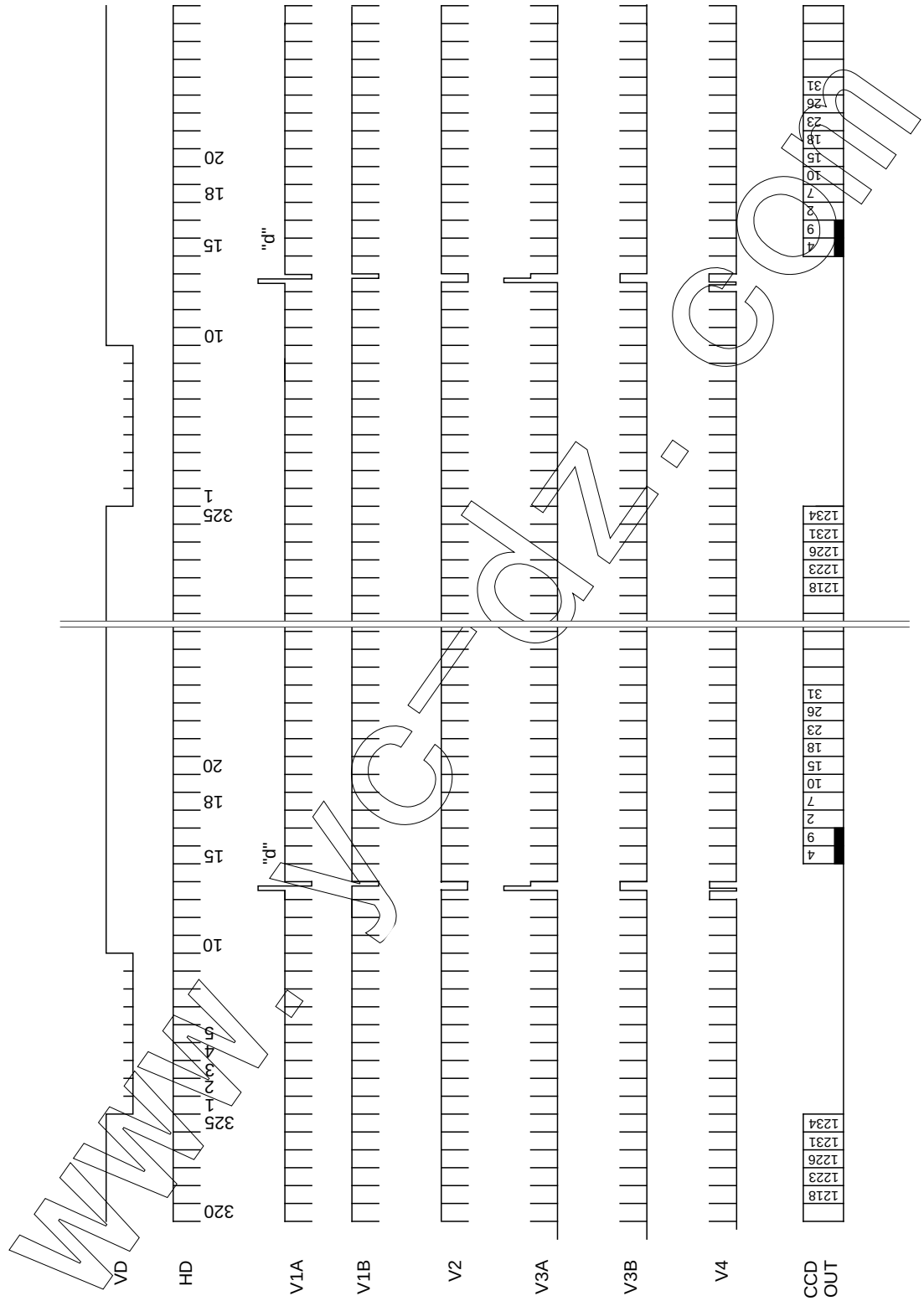
Drive Timing Chart (Vertical Sync) Frame Readout Mode

"c" Enlarged



www.vcore.com

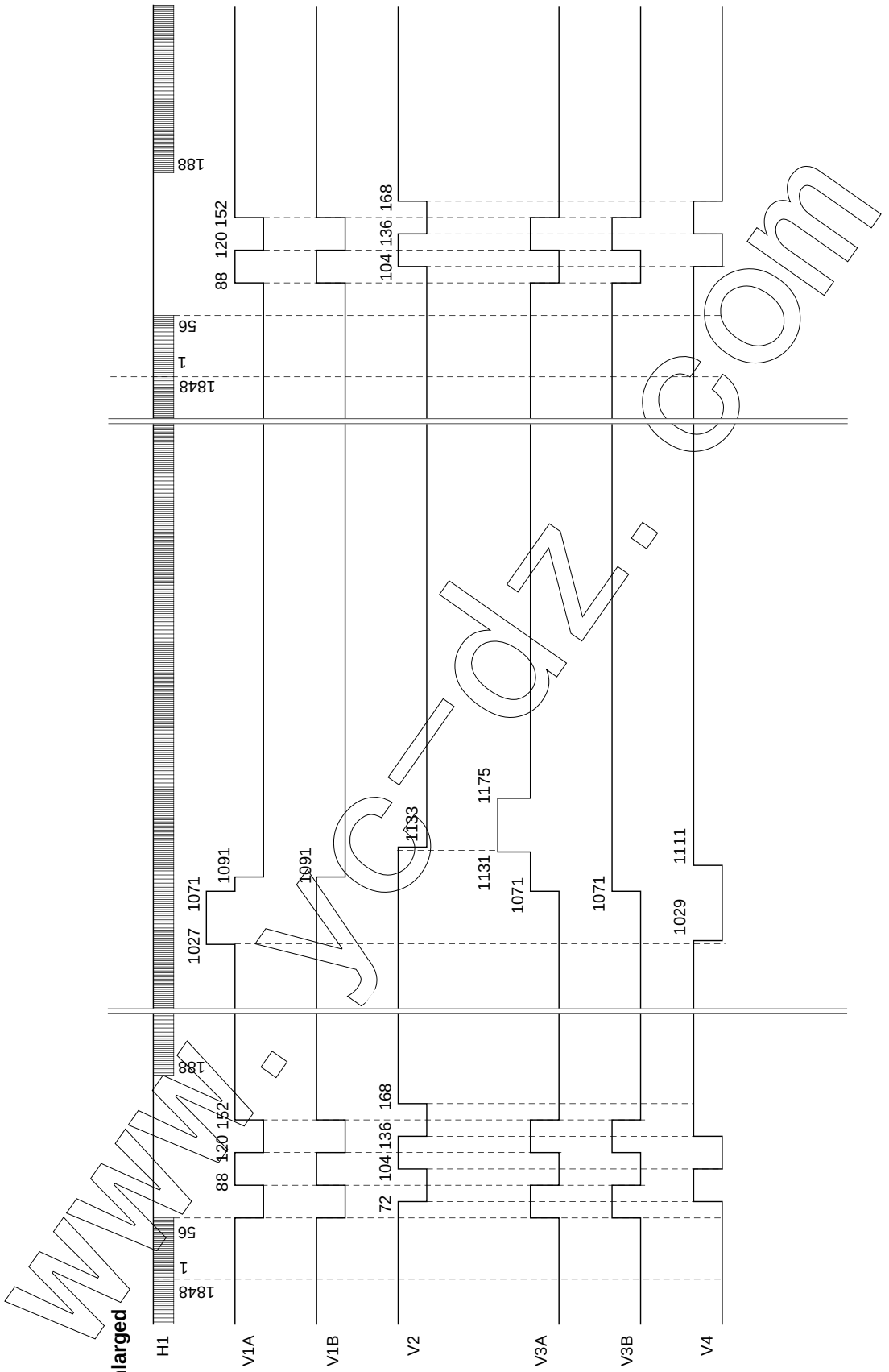
Drive Timing Chart (Vertical Sync) High Frame Rate Readout Mode



www.icdz.com

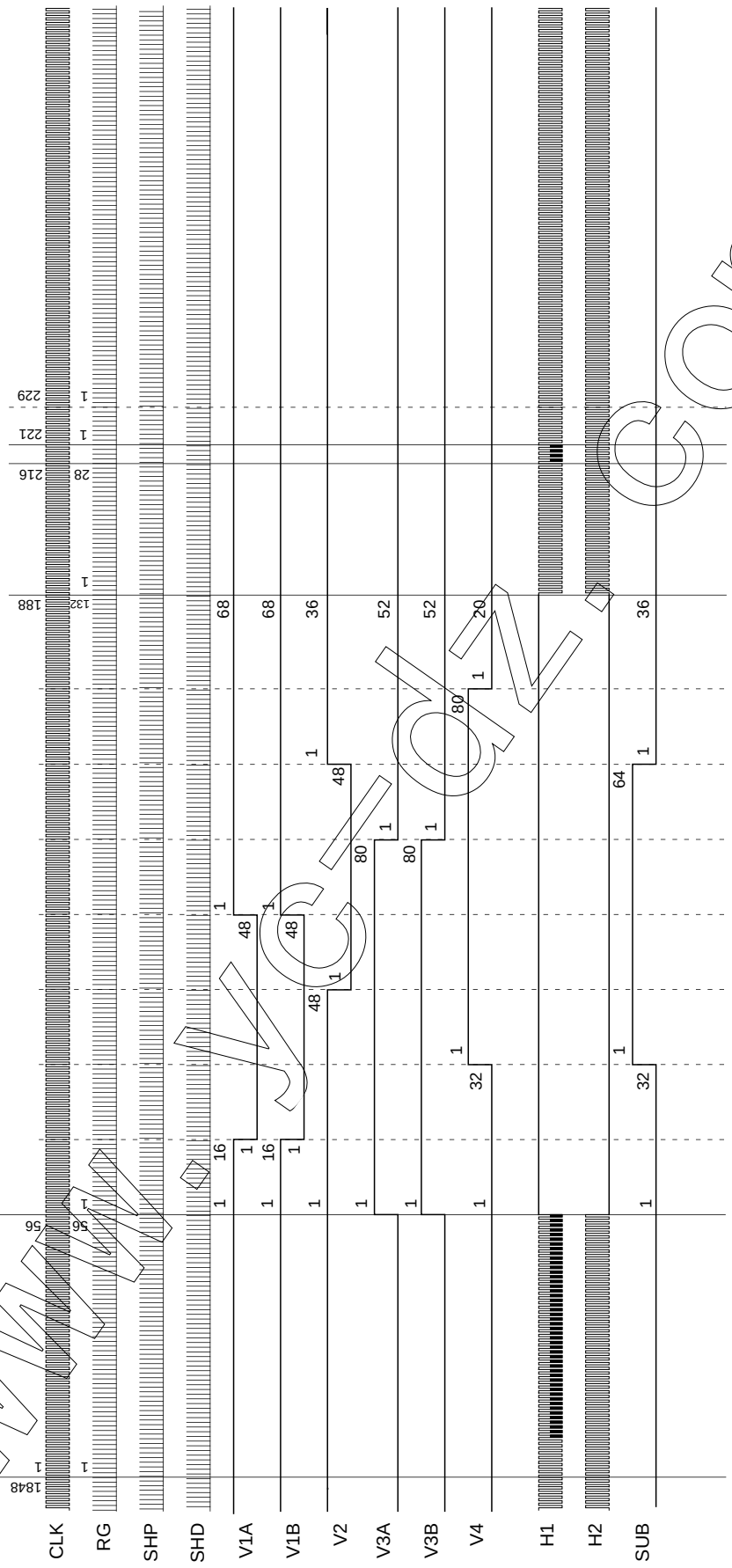
Drive Timing Chart (Vertical Sync) High Frame Rate Readout Mode

"d" Enlarged



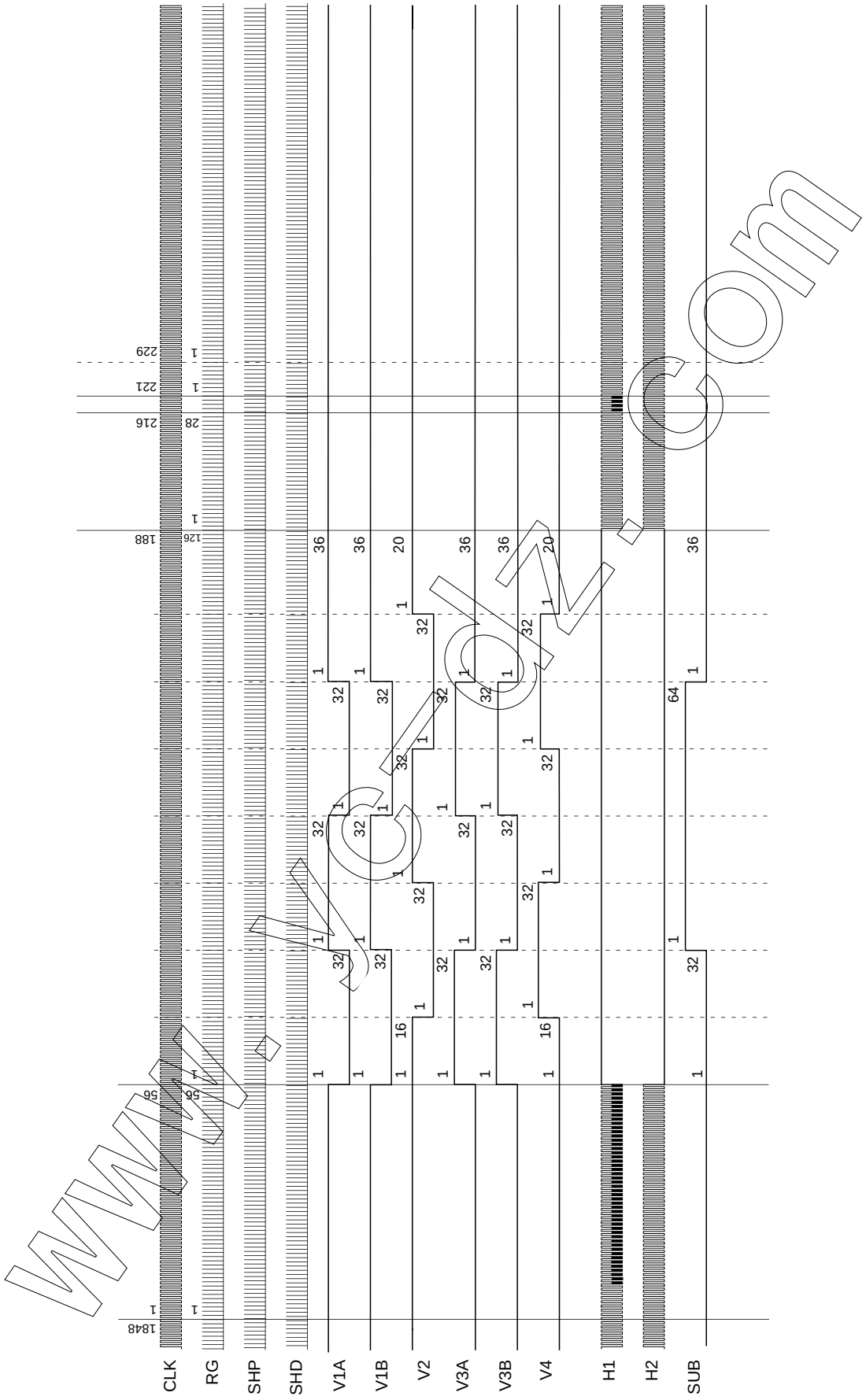
www.xc-dz.com

Drive Timing Chart (Horizontal Sync) Frame Readout Mode



www.ycgz.com

Drive Timing Chart (Horizontal Sync) High Frame Rate Readout Mode



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Notes on Handling

1) Static charge prevention

CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

a) Either handle bare handed or use non-chargeable gloves, clothes or material.
Also use conductive shoes.

b) When handling directly use an earth band.

c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.

d) Ionized air is recommended for discharge when handling CCD image sensors.

e) For the shipment of mounted substrates, use boxes treated for the prevention of static charges.

2) Soldering

a) Make sure the package temperature does not exceed 80°C.

b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a ground 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount, cool sufficiently.

c) To dismount an image sensor, do not use a solder suction equipment. When using an electric desoldering tool, use a thermal controller of the zero-cross On/Off type and connect it to ground.

3) Dust and dirt protection

Image sensors are packed and delivered by taking care of protecting its glass plates from harmful dust and dirt. Clean glass plates with the following operations as required, and use them.

a) Perform all assembly operations in a clean room (class 1000 or less).

b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface, blow it off with an air blower. (For dirt stuck through static electricity ionized air is recommended.)

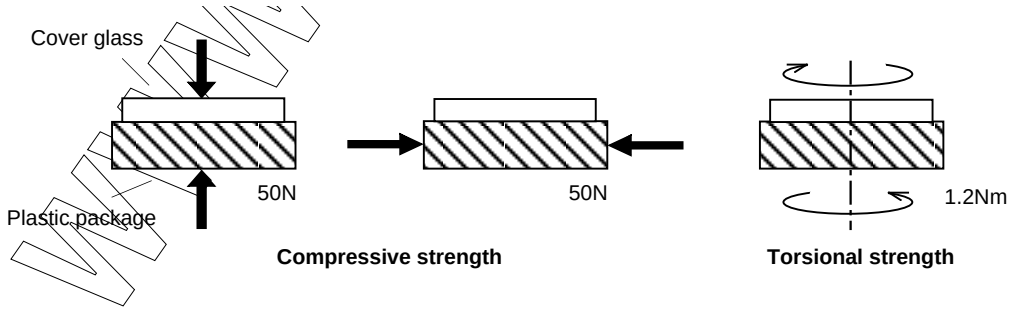
c) Clean with a cotton bud and ethyl alcohol if grease stained. Be careful not to scratch the glass.

d) Keep in a case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.

e) When a protective tape is applied before shipping, just before use remove the tape applied for electrostatic protection. Do not reuse the tape.

4) Installing (attaching)

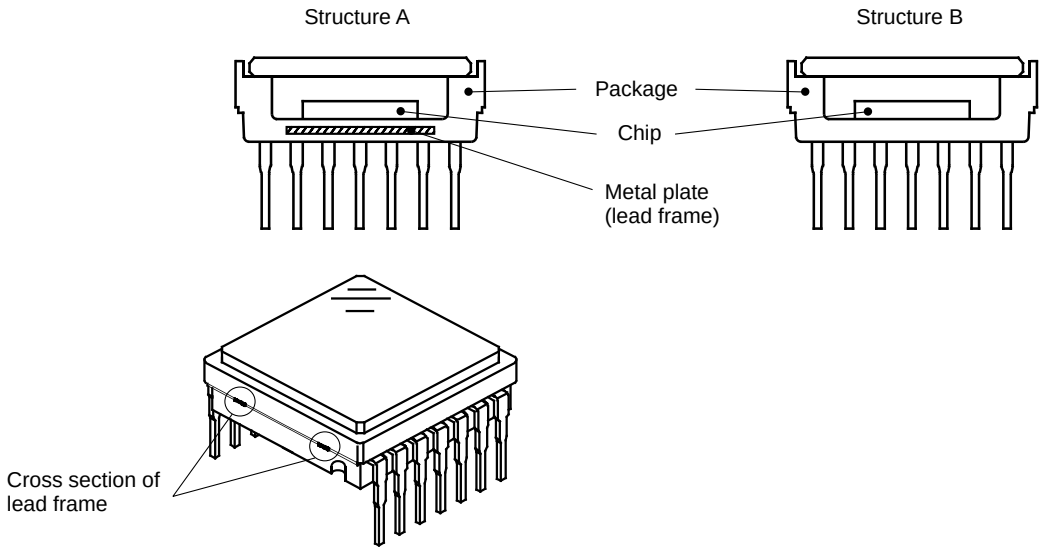
a) Remain within the following limits when applying a static load to the package. Do not apply any load more than 0.7mm inside the outer perimeter of the glass portion, and do not apply any load or impact to limited portions. (This may cause cracks in the package.)



b) If a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the bottom of the package. Therefore, for installation, use either an elastic load, such as a spring plate, or an adhesive.

c) The adhesive may cause the marking on the rear surface to disappear, especially in case the regulated voltage value is indicated on the rear surface. Therefore, the adhesive should not be applied to this area, and indicated values should be transferred to other locations as a precaution.
d) The notch of the package is used for directional index, and that can not be used for reference of fixing. In addition, the cover glass and seal resin may overlap with the notch of the package.
e) If the leads are bent repeatedly and metal, etc., clash or rub against the package, the dust may be generated by the fragments of resin.
f) Acrylate anaerobic adhesives are generally used to attach CCD image sensors. In addition, cyano-acrylate instantaneous adhesives are sometimes used jointly with acrylate anaerobic adhesives. (reference)

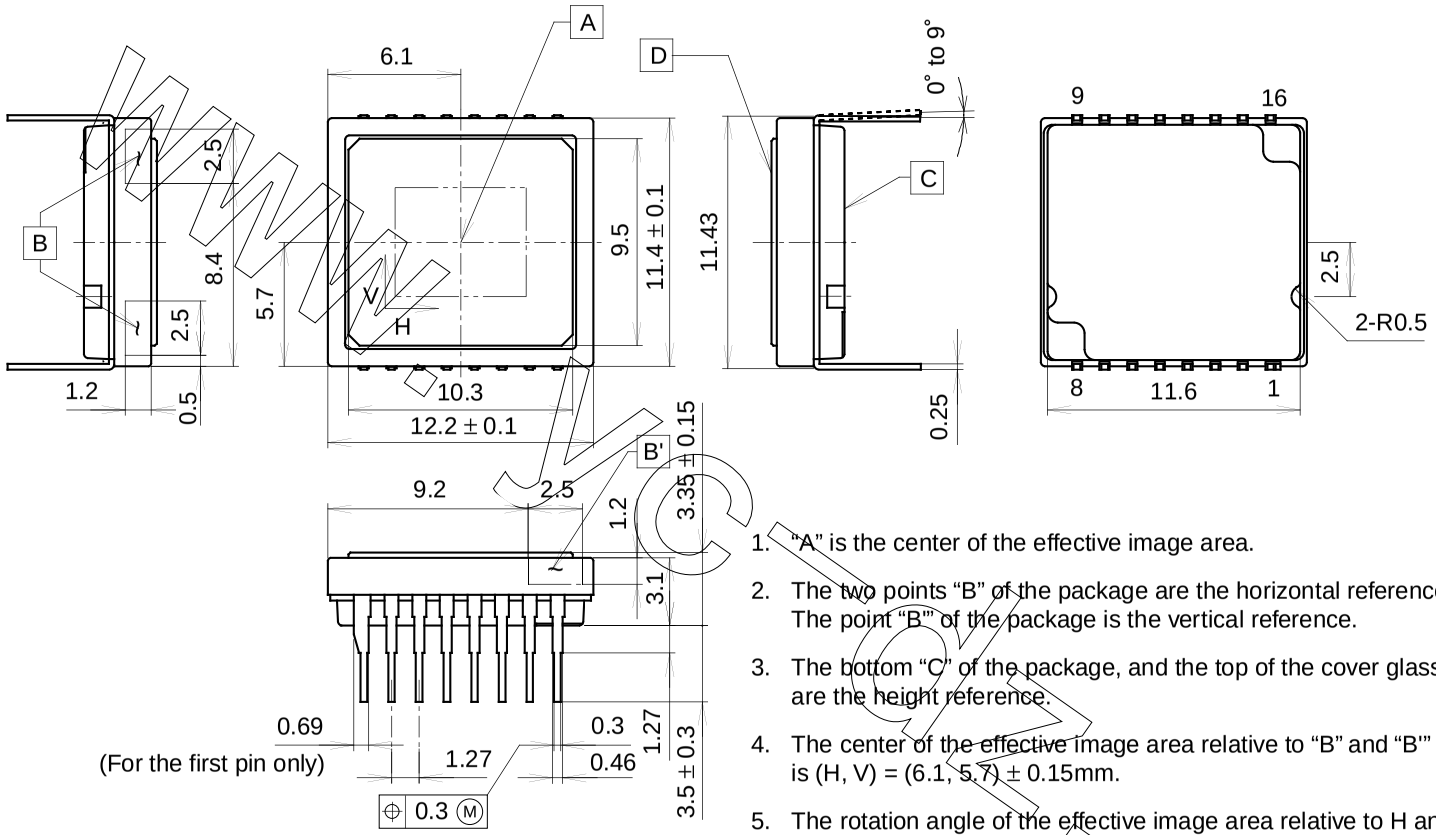
5) Others
a) Do not expose to strong light (sun rays) for long periods, as color filters will be discolored. When high luminous objects are imaged with the exposure level controlled by the electronic iris, the luminance of the image-plane may become excessive and discoloring of the color filter will possibly be accelerated. In such a case, it is advisable that taking-lens with the automatic-iris and closing of the shutter during the power-off mode should be properly arranged. For continuous using under cruel condition exceeding the normal using condition, consult our company.
b) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.
c) Brown stains may be seen on the bottom or side of the package. But this does not affect the CCD characteristics.
d) This package has 2 kinds of internal structure. However, their package outline, optical size, and strength are the same.



The cross section of lead frame can be seen on the side of the package for structure A.

Package Outline Unit: mm

16 pin DIP (450mil)



1. "A" is the center of the effective image area.
2. The two points "B" of the package are the horizontal reference.
   The point "B'" of the package is the vertical reference.
3. The bottom "C" of the package, and the top of the cover glass "D" are the height reference.
4. The center of the effective image area relative to "B" and "B'" is (H, V) = (6.1, 5.7) ± 0.15mm.
5. The rotation angle of the effective image area relative to H and V is ± 1°.
6. The height from the bottom "C" to the effective image area is 1.41 ± 0.10mm.
   The height from the top of the cover glass "D" to the effective image area is 1.94 ± 0.15mm.
7. The tilt of the effective image area relative to the bottom "C" is less than 50µm.
   The tilt of the effective image area relative to the top "D" of the cover glass is less than 50µm.
8. The thickness of the cover glass is 0.75mm, and the refractive index is 1.5.
9. The notches on the bottom of the package are used only for directional index, they must not be used for reference of fixing.

PACKAGE STRUCTURE

PACKAGE MATERIAL	Plastic
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	0.90g
DRAWING NUMBER	AS-C2.2-01(E)

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