TOSHIBA

TOSHIBA Original CMOS 32-Bit Microcontroller

TLCS-900/H2 Series

TMP94C251A

TOSHIBA CORPORATION

Semiconductor Company

CMOS 32-Bit Microcontroller

TMP94C251AF

1. Outline and Device Characteristics

TMP94C251A is high-speed advanced 32-bit microcontroller developed for controlling equipment which processes mass data.

TMP94C251A is a microcontroller which has a high-performance CPU (900/H2 CPU) and various built-in I/Os. And TMP94C251A is enhanced memory interface functions. TMP94C251AF is housed in an 144-pin mini flat package.

Device characteristics are as follows:

(1) CPU: 32-bit CPU (900/H2 CPU)
- Compatible with TLCS-900, 900/L, 900/L1, 900/H's instruction code
- 16 Mbytes of linear address space
- General-purpose registers and register banks
- Micro DMA: 8 channels (250 ns/4 bytes at 20 MHz)

(2) Minimum instruction execution time: 50 ns (at 20 MHz)

(3) Internal memory
- Internal RAM: 2 Kbytes (can use for code section)
- Internal ROM: None

(4) External memory expansion
- Expandable up to 16 Mbytes (shared program/data area)
- Can simultaneously support 8-/16-bit width external data bus

(5) Memory controller
- Chip select output: 6 channels

(6) DRAM Controller: 2 channels
- Direct interface (supported 8-/16-bit external data bus)

(7) 8-bit timer: 4 channels

(8) 16-bit timer: 4 channels

(9) Serial interface: 2 channels

(10) 10-bit AD converter: 8 channels (with sample hold circuit)

(11) 8-bit DA converter: 2 channels (with CMOS-AMP)

(12) Watchdog timer

(13) Interrupt controller

- 18 internal interrupts
- 10 external interrupts

(14) I/O port: 64 pins

(15) Package: 144-pin QFP (P-QFP144-2020-0.50)

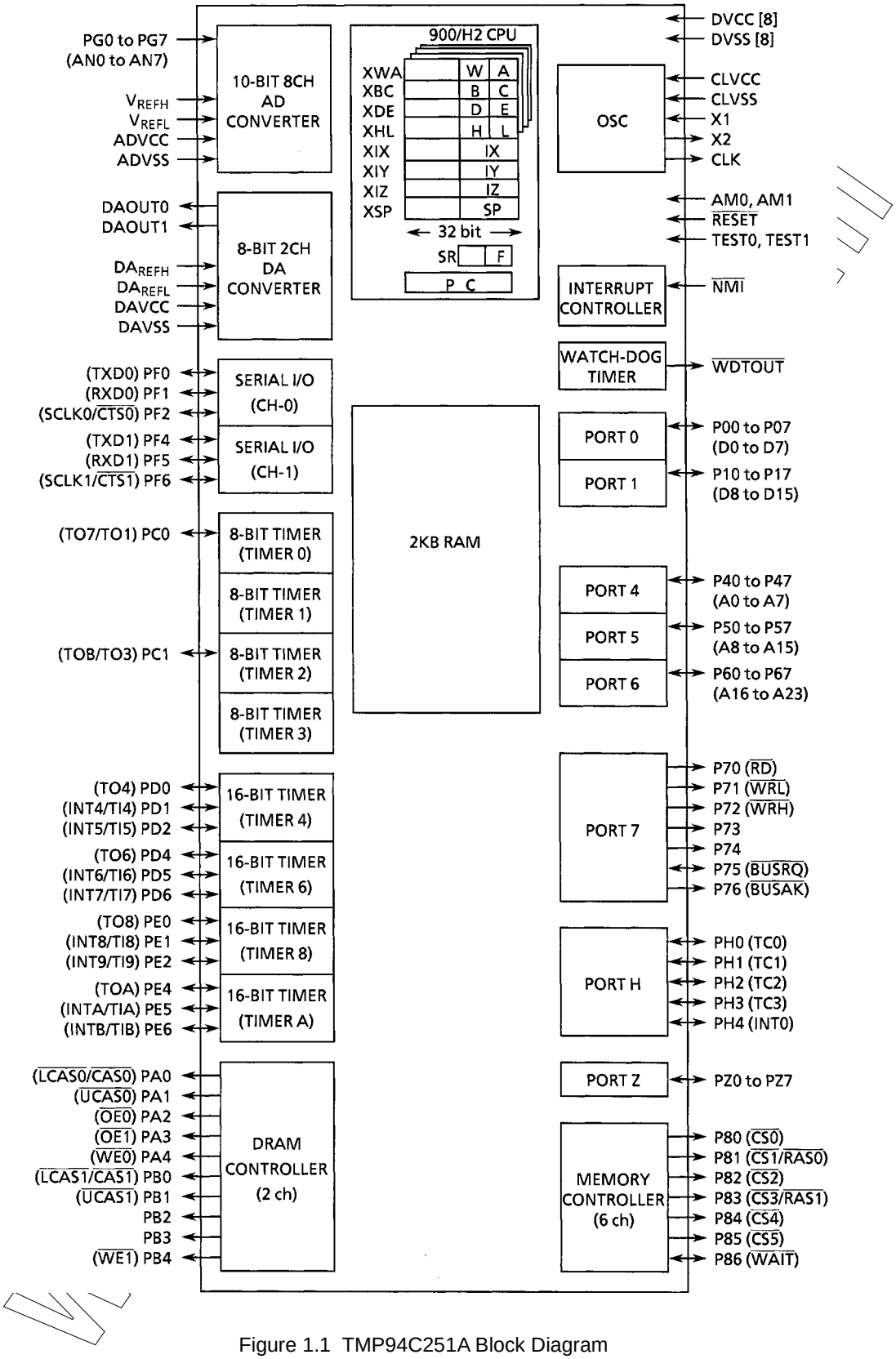


Figure 1.1 TMP94C251A Block Diagram

2. Pin Assignment and Functions

2.1 Pin Assignment (Top view)

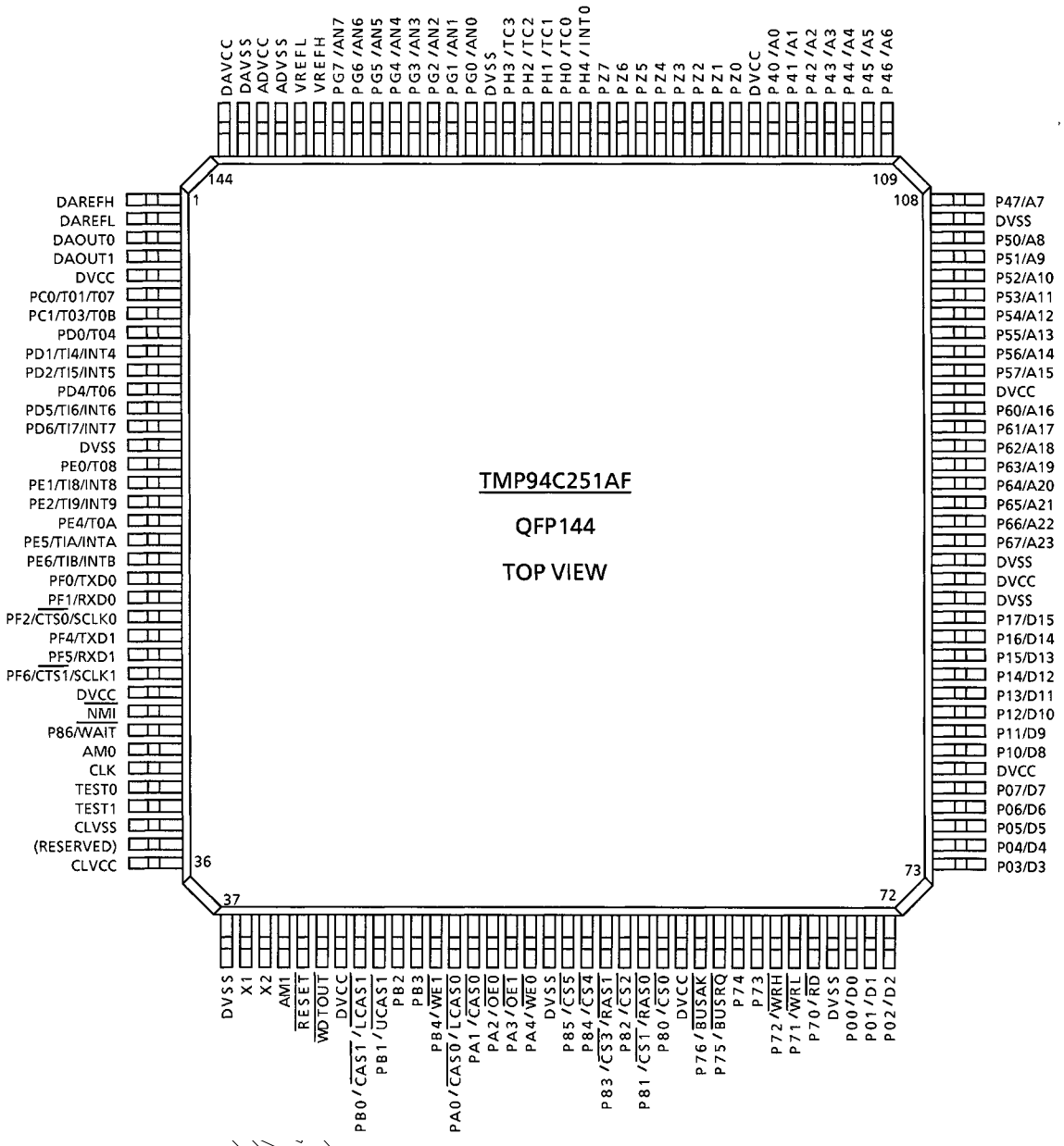


Figure 2.1.1 Pin Assignment

2.2 Pin Names and Functions

The names of input/output pins and their functions are described below.

Table 2.2.1 Pin Names and Functions (1/6)

Pin Name	Number of Pins	I/O	Functions
P00 to P07 D0 to D7	8 (TTL)	I/O I/O	Port 0: I/O port Data: 0 to 7 for data bus TMP94C251A is external ROM type, these pins are initialized to this function. When TMP94C251A doesn't access external memories, these pins are put in the high-impedance state.
P10 to P17 D8 to D15	8 (TTL)	I/O I/O	Port 1: I/O port Data: 8 to15 for data bus If TMP94C251A is external ROM type and is start with 16-bit data bus, these pins are initialized to this function. When TMP94C251A doesn't access external memories, these pins are put in the high-impedance state.
P40 to P47 A0 to A7	8	I/O Output	Port 4: I/O port Address: 0 to 7 for address bus TMP94C251A is external ROM type, these pins are initialized to this function. When TMP94C251A doesn't access external memories, these pins don't change.
P50 to P57 A8 to A15	8	I/O Output	Port 5: I/O port Address: 8 to 15 for address bus TMP94C251A is external ROM type, these pins are initialized to this function. When TMP94C251A doesn't access external memories, these pins don't change.
P60 to P67 A16 to A23	8	I/O Output	Port 6: I/O port Address: 16 to 23 for address bus TMP94C251A is external ROM type, these pins are initialized to this function. When TMP94C251A doesn't access external memories, these pins don't change.
P70 $\overline{RD}$	1	Output Output	Port 70: Output port (output "high" when initialized) Read: Strobe signal for reading external memory When TMP94C251A doesn't access external memory, doesn't output strobe. TMP94C251A is external ROM type, these pins are initialized to this function.
P71 $\overline{WRL}$	1	Output Output	Port 71: Output port (output "high" when initialized) Write LL: Strobe signal for writing data on pins D0 to D7 When TMP94C251A doesn't access external memory, doesn't output strobe.
P72 $\overline{WRH}$	1	Output Output	Port 72: Output port (output "high" when initialized) Write LH: Strobe signal for writing data on pins D8 to D15 When TMP94C251A doesn't access external memory, doesn't output strobe.
P73	1	Output	Port 73: Output port (output "high" when initialized)
P74	1	Output	Port 74: Output port (output "high" when initialized)

Table 2.2.2 Pin Names and Functions (2/6)

Pin Name	Number of Pins	I/O	Functions
P75 $\overline{BUSRQ}$	1	I/O Input	Port 75: I/O port Bus request: Signal used to request high impedance for memory interface signals. If these signals are used as port, there are not change. The memory interface signals are follows: A0 to A23, D0 to D15, $\overline{RD}$, $\overline{WRLL}$, $\overline{WRLH}$ The output signals of memory controller.
P76 $\overline{BUSAK}$	1	Output Output	Port 76: Output port (output “high” when initialized) Bus acknowledge: Signal indicating that request of $\overline{BUSRQ}$ signal is accepted.
P80 $\overline{CS0}$	1	Output Output	Port 80: Output port (output “high” when initialized) Chip select 0: Outputs “low” if address is within specified address area.
P81 $\overline{CS1}$ $\overline{RAS0}$	1	Output Output Output	Port 81: Output port (output “high” when initialized) Chip select 1: Outputs “low” if address is within specified address area. Row address strobe 0: Outputs $\overline{RAS}$ strobe for DRAM if address is within specified address area.
P82 $\overline{CS2}$	1	Output Output	Port 82: Output port (output “high” when initialized) Chip select 2: Outputs “low” if address is within specified address area.
P83 $\overline{CS3}$ $\overline{RAS1}$	1	Output Output Output	Port 83: Output port (output “high” when initialized) Chip select 3: Outputs “low” if address is within specified address area. Row address strobe 1: Outputs $\overline{RAS}$ strobe for DRAM if address is within specified address area.
P84 $\overline{CS4}$	1	Output Output	Port 84: Output port (output “high” when initialized) Chip select 4: Outputs “low” if address is within specified address area.
P85 $\overline{CS5}$	1	Output Output	Port 85: Output port (output “high” when initialized) Chip select 5: Outputs “low” if address is within specified address area.
P86 $\overline{WAIT}$	1	I/O Input	Port 86: I/O port Wait: Signal used to request CPU bus wait.

Table 2.2.3 Pin Names and Functions (3/6)

Pin Name	Number of Pins	I/O	Functions
PA0	1	Output	Port A0: Output port (output “high” when initialized)
$\overline{CAS0}$		Output	Column address strobe 0: Outputs $\overline{CAS}$ strobe for DRAM if address is within specified address area.
$\overline{LCAS0}$		Output	Lower column address strobe 0: Outputs lower $\overline{CAS}$ strobe for DRAM if address is within specified address area.
PA1	1	Output	Port A1: Output port (output “high” when initialized)
$\overline{UCAS0}$		Output	Upper Column address strobe 0: Outputs upper $\overline{CAS}$ strobe for DRAM if address is within specified address area.
PA2	1	Output	Port A2: Output port (output “high” when initialized)
$\overline{OE0}$		Output	Output enable 0: Outputs read enable signal for DRAM.
PA3	1	Output	Port A3: Output port (output “high” when initialized)
$\overline{OE1}$		Output	Output enable 1: Outputs read enable signal for DRAM.
PA4	1	Output	Port A4: Output port (output “high” when initialized)
$\overline{WE0}$		Output	Write enable 0: Outputs write enable signal for DRAM.
PB0	1	Output	Port B0: Output port (output “high” when initialized)
$\overline{CAS1}$		Output	Column address strobe 1: Outputs $\overline{CAS}$ strobe for DRAM if address is within specified address area.
$\overline{LCAS1}$		Output	Lower column address strobe 1: Outputs lower $\overline{CAS}$ strobe for DRAM if address is within specified address area.
PB1	1	Output	Port B1: Output port (output “high” when initialized)
$\overline{UCAS1}$		Output	Upper Column address strobe 1: Outputs upper $\overline{CAS}$ strobe for DRAM if address is within specified address area.
PB2	1	Output	Port B2: Output port (output “high” when initialized)
PB3	1	Output	Port B3: Output port (output “high” when initialized)
PB4	1	Output	Port B4: Output port (output “high” when initialized)
$\overline{WE1}$		Output	Write enable 1: Outputs write enable signal for DRAM.

Table 2.2.4 Pin Names and Functions (4/6)

Pin Name	Number of Pins	I/O	Functions
PC0	1	I/O	Port C0: I/O port
TO1		Output	Timer output 1: 8-bit timer 0 or 1 output
TO7		Output	Timer output 7: 16-bit timer 7 output
PC1	1	I/O	Port C1: I/O port
TO3		Output	Timer output 3: 8-bit timer 2 or 3 output
TOB		Output	Timer output B: 16-bit timer B output
PD0	1	I/O	Port D0: I/O port
TO4		Output	Timer output 4: 16-bit timer 4 output
PD1	1	I/O	Port D1: I/O port
TI4		Input	Timer input 4: 16-bit timer 4 input
INT4		Input	Interrupt request pin 4: Interrupt request pin with programmable rising/falling edge
PD2	1	I/O	Port D2: I/O port
TI5		Input	Timer input 5: 16-bit timer 4 input
INT5		Input	Interrupt request pin 5: Interrupt request pin with rising edge
PD4	1	I/O	Port D4: I/O port
TO6		Output	Timer output 6: 16-bit timer 6 output
PD5	1	I/O	Port D5: I/O port
TI6		Input	Timer input 6: 16-bit timer 6 input
INT6		Input	Interrupt request pin 6: Interrupt request pin with programmable rising/falling edge
PD6	1	I/O	Port D6: I/O port
TI7		Input	Timer input 7: 16-bit timer 6 input
INT7		Input	Interrupt request pin 7: Interrupt request pin with rising edge
PE0	1	I/O	Port E0: I/O port
TO8		Output	Timer output 8: 16-bit timer 8 output
PE1	1	I/O	Port E1: I/O port
TI8		Input	Timer input 8: 16-bit timer 8 input
INT8		Input	Interrupt request pin 8: Interrupt request pin with programmable rising/falling edge
PE2	1	I/O	Port E2: I/O port
TI9		Input	Timer input 9: 16-bit timer 8 input
INT9		Input	Interrupt request pin 9: Interrupt request pin with rising edge
PE4	1	I/O	Port E4: I/O port
TOA		Output	Timer output A: 16-bit timer A output
PE5	1	I/O	Port E5: I/O port
TIA		Input	Timer input A: 16-bit timer A input
INTA		Input	Interrupt request pin A: Interrupt request pin with programmable rising/falling edge
PE6	1	I/O	Port E6: I/O port
TIB		Input	Timer input B: 16-bit timer A input
INTB		Input	Interrupt request pin B: Interrupt request pin with rising edge

Table 2.2.5 Pin Names and Functions (5/6)

Pin Name	Number of Pins	I/O	Functions
PF0 TXD0	1	I/O Output	Port F0: I/O port Serial send data 0
PF1 RXD0	1	I/O Input	Port F1: I/O port Serial receive data 0
PF2 $\overline{CTS0}$ SCLK0	1	I/O Input I/O	Port F2: I/O port Serial data receive enable 0 Serial clock I/O 0
PF4 TXD1	1	I/O Output	Port F4: I/O port Serial send data 1
PF5 RXD1	1	I/O Input	Port F5: I/O port Serial receive data 1
PF6 $\overline{CTS1}$ SCLK1	1	I/O Input I/O	Port F6: I/O port Serial data receive enable 1 Serial clock I/O 1
PG0 to PG7 AN0 to AN7	8	Input Input	Port G: Input port Analog input: Input to 10-bit AD converter
DAOUT0	1	Output	DA output 0: Output from 8-bit DA converter 0
DAOUT1	1	Output	DA output 1: Output from 8-bit DA converter 1
PH0 TC0	1	I/O Output	Port H0: I/O port Terminal count 0: Outputs “high” strobe when counter value of micro-DMA channel 0 is “0”.
PH1 TC1	1	I/O Output	Port H1: I/O port Terminal count 1: Outputs “high” strobe when counter value of micro-DMA channel 1 is “0”.
PH2 TC2	1	I/O Output	Port H2: I/O port Terminal count 2: Outputs “high” strobe when counter value of micro-DMA channel 2 is “0”.
PH3 TC3	1	I/O Output	Port H3: I/O port Terminal count 3: Outputs “high” strobe when counter value of micro-DMA channel 3 is “0”.
PH4 INT0	1	I/O Input	Port H4: I/O port (schmitt input) Interrupt request pin 0: Interrupt request pin with programmable level/rising edge. (schmitt input)
PZ0 to PZ7	8	I/O	Port Z: I/O port
$\overline{NMI}$	1	Input	Non-maskable interrupt request pin: Interrupt request pin with falling edge. Can also be operated at rising edge by program. (schmitt input)
$\overline{WDTOUT}$	1	Output	Watchdog timer output pin

Table 2.2.6 Pin Names and Functions (6/6)

Pin Name	Number of Pins	I/O	Functions
AM0, 1	2	Input	Address mode: Selects external data bus width. AM1 = "low" AM0 = "low": Start with 8-bit external data bus AM1 = "low" AM0 = "high": Start with 16-bit external data bus AM1 = "high" AM0 = "low": Don't use this setting AM1 = "high" AM0 = "high": Don't use this setting
TEST0, 1	2	Input	Test: Input "low" when using
CLK	1	Output	Clock output: Outputs system clock
X1/X2	2	I/O	Oscillator connecting pin
$\overline{\text{RESET}}$	1	Input	Reset: Initializes LSI (with pull-up resistor) (schmitt input)
VREFH	1	Input	Pin for reference voltage input to AD converter ("high" level)
VREFL	1	Input	Pin for reference voltage input to AD converter ("low" level)
DAREFH	1	Input	Pin for reference voltage input to DA converter ("high" level)
DAREFL	1	Input	Pin for reference voltage input to DA converter ("low" level)
ADVCC	1	–	Power supply pin for 10-bit AD converter
ADVSS	1	–	GND pin for 10-bit AD converter (0 V)
DAVCC	1	–	Power supply pin for 8-bit DA converter
DAVSS	1	–	GND pin for 8-bit DA converter (0 V)
CLVCC	1	–	Power supply pin for clock doubler
CLVSS	1	–	GND pin for clock doubler
DVCC	8	–	Power supply pin (+5 V) (Connect all DVCC pins to +5V)
DVSS	8	–	GND pin (0 V) (Connect all DVSS pins to GND(0V).)

3. Operation

The following is a block-by-block description of the functions and basic operation of TMP94C251A.

3.1 CPU

TMP94C251A contains an advanced, high-speed 32-bit CPU (900/H2 CPU).

3.1.1 CPU Outline

900/H2 CPU is high-speed and high-performance CPU based on 900/H CPU. 900/H2 CPU has expanded 32-bit internal data bus to process instructions more quickly.

Functional differences between 900/H2 CPU and 900/H CPU are as follows:

	900/H2 CPU
Width of CPU Address Bus	24-bit
Width of CPU Data Bus	32-bit
Internal Operating Frequency	20 MHz
Minimum Bus Cycle	1-clock access (50 ns @ 20 MHz)
Bus Sizing Function	8/16-bit
Internal RAM	32-bit 1-clock access
Internal I/O	8/16/32-bit 2-clock access
External Device	8/16-bit 2-clock access (can insert some waits)
Minimum Instruction Execution Cycle	1-clock (50 ns @20 MHz)
Conditional Jump	2-clock (100 ns @20 MHz)
Instruction Queue Buffer	12-byte
Instruction Set	No MIN instruction No LDX instruction
CPU mode	No MIN (minimum) mode
Micro DMA	8-channel

3.1.2 Reset Operation

When resetting the TMP94C251A microcontroller, ensure that the power supply voltage is within the operating voltage range, and that the internal high-frequency oscillator has stabilized. Then set the $\overline{\text{RESET}}$ input to low level at least for 10 system clocks (2 μs at 10 MHz). Thus, when turn on the switch, be set to the power supply voltage is within the operating voltage range, and that the internal high-frequency oscillator has stabilized. Then hold the $\overline{\text{RESET}}$ input to low level at least for 10 system clocks.

Clock gear is initialized 1/16 mode by reset operation. It means that the system clock mode f_{SYS} is set to fc/32 (= fc/16 × 1/2).

When the reset is accepted, the CPU:

- Set the program counter (PC) to the reset vector stored at addresses FFFF00H to FFFF02H.

  PC (7:0) ← Value at address FFFF00H
  PC (15:8) ← Value at address FFFF01H
  PC (23:16) ← Value at address FFFF02H
- Sets the stack pointer (XSP) to 00000000H
- Sets bits IFF2 to IFF0 of the status register (SR) to 111 (This sets the interrupt level mask register to level 7).
- Clears bits RFP1 to RFP0 of the status register (SR) to 00 (This sets the register banks to 0).

After reset is released, the CPU begins execution from the instruction at the location specified in the PC. Other than the changes described above, reset does not alter any internal CPU registers.

When reset is accepted, processing of the internal I/O, port, and other pins are as follows:

- Initializes the internal I/O registers as table of “Special Function Register” in section 5.
- Set ports pins to general-purpose input port mode.
- Sets the $\overline{\text{WDTOUT}}$ pin to “Low”. (However, when reset is released, sets to “High”.)

When external reset is released, built-in clock doubler begins operation and after the stable time (1.6384 ms at 20 MHz) elapse of the circuit, internal reset is released.

The operation of memory controller and DRAM controller cannot be insured until power supply becomes stable after power-on reset. The external RAM data provided before turning on the TMP94C251A may be spoiled because the control signals are unstable until power supply becomes stable after power on reset.

3.1.3 Data Bus Size after Reset Release

The start data bus size is determined depending on the state of a AM1/AM0 pins just after reset release. Then the external memory is accessed as follows.

AM1	AM0	Start mode
"0"	"0"	8 bit data bus (1wait)
"0"	"1"	16 bit data bus (1wait)
"1"	"0"	Don't use this setting
"1"	"1"	Don't use this setting

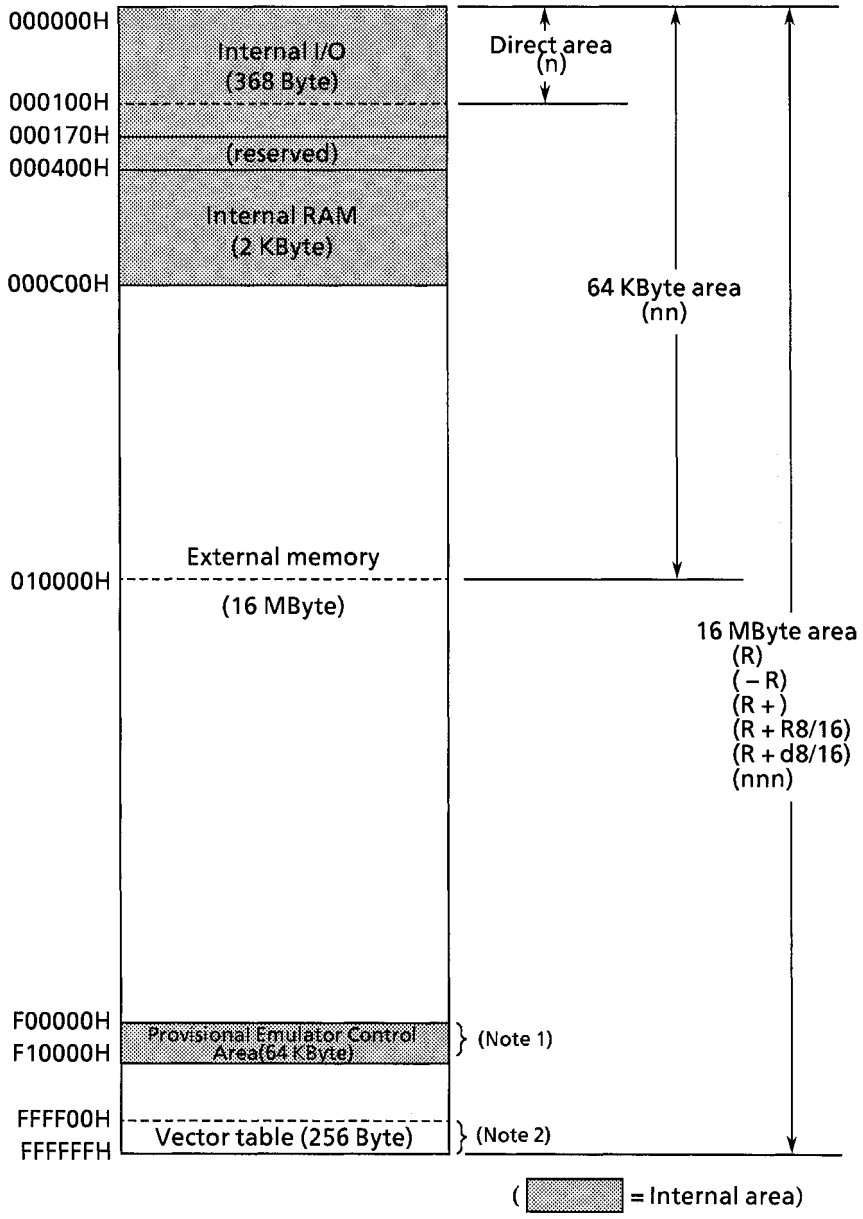
For the details, refer to chapter 3.6 "Memory Controller".

3.1.4 Setting of TEST0, TEST1

Connect TEST0, TEST1 pin to "GND" to use.

3.2 Memory Map

Figure 3.2.1 is a memory map of the TMP94C251A.



Note 1: Emulator control area is for emulator, it is mapped F00000H to F10000H address. Don't use this area. This area is reserved.

Note 2: Don't use the last 16-byte area (FFFFF0H to FFFFFFH). This area is reserved.

Figure 3.2.1 Memory Map

4. Electrical Characteristics

4.1 Maximum Ratings

Symbol	Parameter	Rating	Unit
V cc	Power Supply Voltage	– 0.5 to 6.5	V
V IN	Input Voltage	– 0.5 to Vcc + 0.5	V
Σ IOL	Output Current (total)	120	mA
Σ IOH	Output Current (total)	– 120	mA
P D	Power Dissipation (Ta = 70°C)	600	mW

Note: The maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no maximum rating value will ever be exceeded.

4.2 DC Electrical Characteristics

Vcc = 5 V ± 10%, TA = –20 to 70°C
X1 = 8 to 10 MHz (Internal operation = 16 to 20 MHz)

Symbol	Parameter	Min	Max	Unit	Test Condition
V IL0	Input Low Voltage P00 to P07 (D0 to 7) P10 to P17 (D8 to 15) P20 to P27 (D16 to 23) P30 to P37 (D24 to 31)	– 0.3	0.8	V	
V IL1	Input Low Voltage P40 to P47 P50 to P57 P60 to P67 P75 P86 PC0, PC1 PD0 to PD2, PD4 to PD6 PE0 to PE2, PE4 to PE6 PF0 to PF2, PF4 to PF6 PG0 to PG7 PH0 to PH3 PZ0 to PZ7	– 0.3	0.3*Vcc	V	
V IL2	Input Low Voltage PH4 (INT0) $\overline{\text{NMI}}$ $\overline{\text{RESET}}$	– 0.3	0.25*Vcc	V	
V IL3	Input Low Voltage AM0, AM1 TEST0, TEST1	– 0.3	0.3	V	
V IL4	Input Low Voltage X1	– 0.3	0.2*Vcc	V	
V IH0	Input High Voltage P00 to P07 (D0 to 7) P10 to P17 (D8 to 15) P20 to P27 (D16 to 23) P30 to P37 (D24 to 31)	2.2	Vcc + 0.3	V	

Note: Typical value are for Ta = 25 °C and Vcc = 5 V unless otherwise noted.

Symbol	Parameter	Min	Max	Unit	Test Condition
V IH1	Input High Voltage P40 to P47 P50 to P57 P60 to P67 P75 P86 PC0, PC1 PD0 to PD2, PD4 to PD6 PE0 to PE2, PE4 to PE6 PF0 to PF2, PF4 to PF6 PG0 to PG7 PH0 to PH3 PZ0 to PZ7	0.7*Vcc	Vcc + 0.3	V	
V IH2	Input High Voltage $\overline{\text{PH4}}$ (INT0) $\overline{\text{NMI}}$ $\overline{\text{RESET}}$	0.75*Vcc	Vcc + 0.3	V	
V IH3	Input High Voltage AM0, AM1 TEST0, TEST1	Vcc − 0.3	Vcc + 0.3	V	
V IH4	Input High Voltage X1	0.8*Vcc	Vcc + 0.3	V	
V OL	Output Low Voltage		0.45	V	IOL = 1.6 mA
V OH0	Operating Cururent (NORMAL)	2.4		V	IOH = − 400 μA
V OH1	Output High Voltage	0.75*Vcc		V	IOH = − 100 μA
V OH2	Output High Voltage	0.9*Vcc		V	IOH = − 20 μA
I LI	Input Leakage Current	0.02 (typ.)	± 5	μA	0.0V ≦ Vin ≦ Vcc
I LO	Output Leakage Current	0.05 (typ.)	± 10	μA	0.2V ≦ Vin ≦ Vcc − 0.2 V
I cc0	Operating Current (NORMAL)	90	108	mA	X1 = 10 MHz (Internal 20 MHz)
I cc1	RUN	50	70	mA	X1 = 10 MHz (Internal 20 MHz)
I cc2	IDLE	5	20	mA	X1 = 10 MHz (Internal 20 MHz)
I cc3	STOP	0.5	50	μA	0.2 V ≦ Vin ≦ Vcc − 0.2 V Ta = − 20~70°C
I cc4	STOP		10	μA	0.2 V ≦ Vin ≦ Vcc − 0.2 V Ta = 0~50°C
V STOP	Power Down Voltage @ STOP (for internal RAM back-up)	2.0	6.0	V	VIL2 = 0.2*Vcc VIH2 = 0.8*Vcc
RRST	Pull Up Registance $\overline{\text{RESET}}$	50	150	kΩ	
CIO	Pin Capacitance		10	pF	fc = 1 MHz
VTH	Schmitt Width $\overline{\text{PH4}}$ (INT0) $\overline{\text{NMI}}$ $\overline{\text{RESET}}$	0.4	1.0 (typ)	V	

4.3 AC Electrical Characteristics

4.3.1 Basic Bus Cycle

(1) Read cycle

No.	Symbol	Parameter	Min	Max	at 20 MHz	at 16 MHz	Unit
1	t_{OSC}	OSC period (X1/X2)	100	125	100	125	ns
2	t_{CYC}	System Clock Period (= T)	50	62.5	50	62.5	ns
3	t_{CL}	CLK Low Width	0.5 × T – 15		10	16	ns
4	t_{CH}	CLK High Width	0.5 × T – 15		10	16	ns
5-1	t_{AD}	A0 to A23 → D0 to D31 Input at 0 waits		2.0 × T – 50	50	75	ns
5-2	t_{AD3}	A0 to A23 → D0 to D31 Input at 1 wait		3.0 × T – 50	100	138	ns
6-1	t_{RD}	$\overline{RD}$ Fall → D0 to D31 Input at 0 waits		1.5 × T – 45	30	49	ns
6-2	t_{RD3}	$\overline{RD}$ Fall → D0 to D31 Input at 1 wait		2.5 × T – 45	80	111	ns
7-1	t_{RR}	$\overline{RD}$ Low Width at 0 waits	1.5 × T – 20		55	74	ns
7-2	t_{RR3}	$\overline{RD}$ Low Width at 1 wait	2.5 × T – 20		105	136	ns
8	t_{AR}	A0 to A23 Valid → $\overline{RD}$ Fall	0.5 × T – 20		5	11	ns
9	t_{RK}	$\overline{RD}$ Fall → CLK Fall	0.5 × T – 20		5	11	ns
10	t_{HA}	A0 to A23 Invalid → D0 to D31 Hold	0		0	0	ns
11	t_{HR}	$\overline{RD}$ Rise → D0 to D31 Hold	0		0	0	ns
12	t_{APR}	A0 to A23 Valid → PORT Input		2.0 × T – 120	–20	5	ns
13	t_{APH}	A0 to A23 Valid → PORT Hold	2.0 × T		100	125	ns
14	t_{TK}	$\overline{WAIT}$ Setup Time	15		15	15	ns
15	t_{KT}	$\overline{WAIT}$ Hold Time	5		5	5	ns

(2) Write cycle

No.	Symbol	Parameter	Min	Max	at 20 MHz	at 16 MHz	Unit
1	t_{OSC}	OSC Period (X1/X2)	100	125	100	125	ns
2	t_{CYC}	System Clock Period (= T)	50	62.5	50	62.5	ns
3	t_{CL}	CLK Low Width	0.5 × T – 15		10	16	ns
4	t_{CH}	CLK High Width	0.5 × T – 15		10	16	ns
5-1	t_{DW}	D0 to D31 Valid → $\overline{WRx}$ Rise at 0 waits	1.25 × T – 35		28	43	ns
5-2	t_{DW3}	D0 to D31 Valid → $\overline{WRx}$ Rise at 1 wait	2.25 × T – 35		78	106	ns
6-1	t_{WW}	$\overline{WRx}$ Low Width at 0 waits	1.25 × T – 30		33	48	ns
6-2	t_{WW3}	$\overline{WRx}$ Low Width at 1 wait	2.25 × T – 30		83	111	ns
7	t_{AW}	A0 to A23 Valid → $\overline{WRx}$ Fall	0.5 × T – 20		5	11	ns
8	t_{WK}	$\overline{WRx}$ Fall → CLK Fall	0.5 × T – 20		5	11	ns
9	t_{WA}	$\overline{WRx}$ Rise → A0 to A23 Hold	0.25 × T – 5		8	11	ns
10	t_{WD}	$\overline{WRx}$ Rise → D0 to D31 Hold	0.25 × T – 5		8	11	ns
11	t_{APW}	A0 to A23 Valid → PORT Output		2.0 × T + 70	170	195	ns
12	t_{TK}	$\overline{WAIT}$ Setup Time	15		15	15	ns
13	t_{KT}	$\overline{WAIT}$ Hold Time	5		5	5	ns
14	t_{RDO}	$\overline{RD}$ Rise → D0 to D15 Output	0.5 × T – 5		20	26	ns

AC Condition

Output: P0 to P3 (D0 to D31), P4 to P6 (A0 to A23), P70 ($\overline{RD}$), P71 to P74 ($\overline{WRx}$)

High = 2.0 V, Low = 0.8 V, CL = 50 pF

Others

High = 2.0 V, Low = 0.8 V, CL = 50 pF

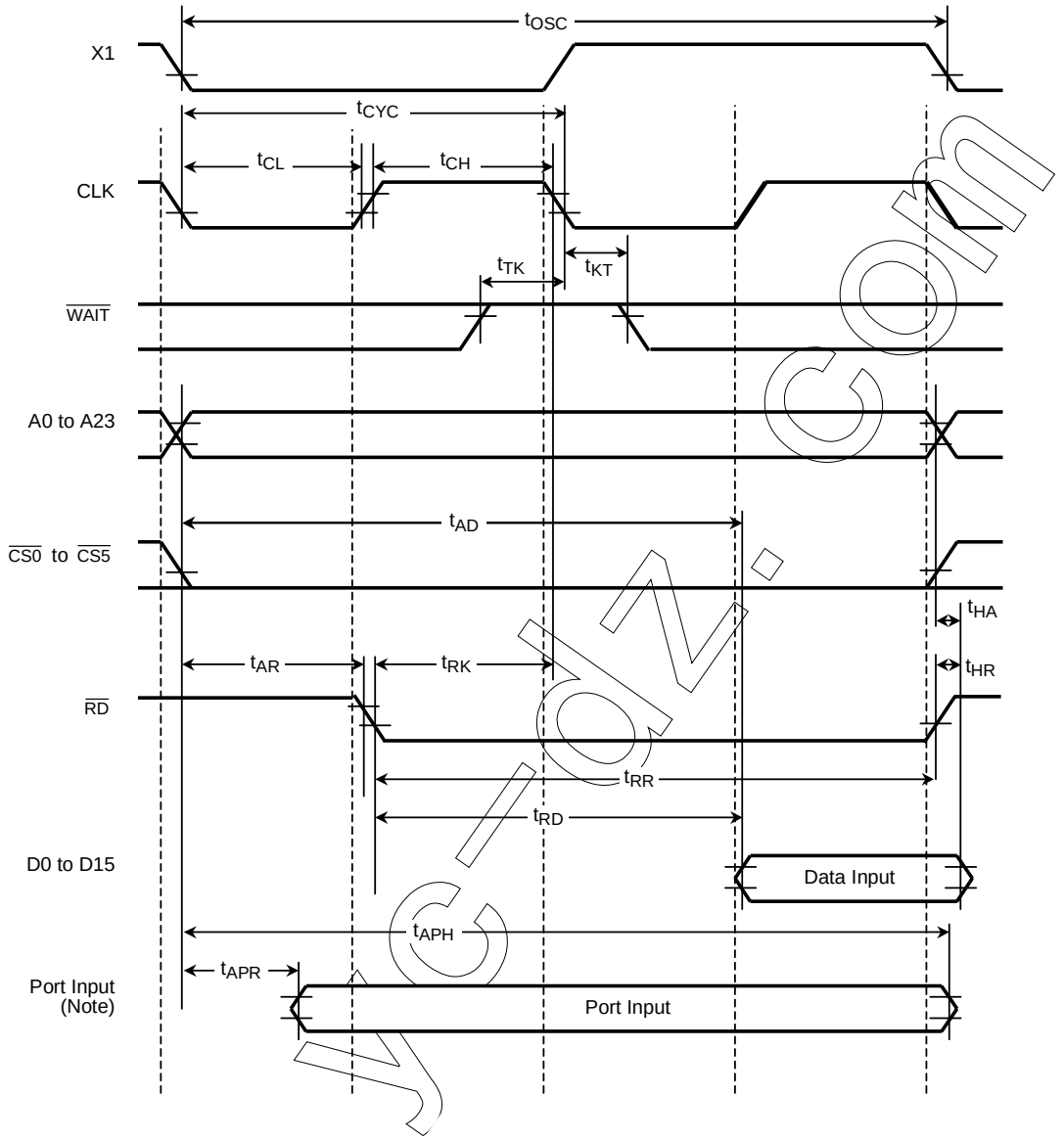
Input: P0 to P3 (D0 to D31)

High = 2.4 V, Low = 0.45 V

Others

High = 0.8 Vcc, Low = 0.2 Vcc

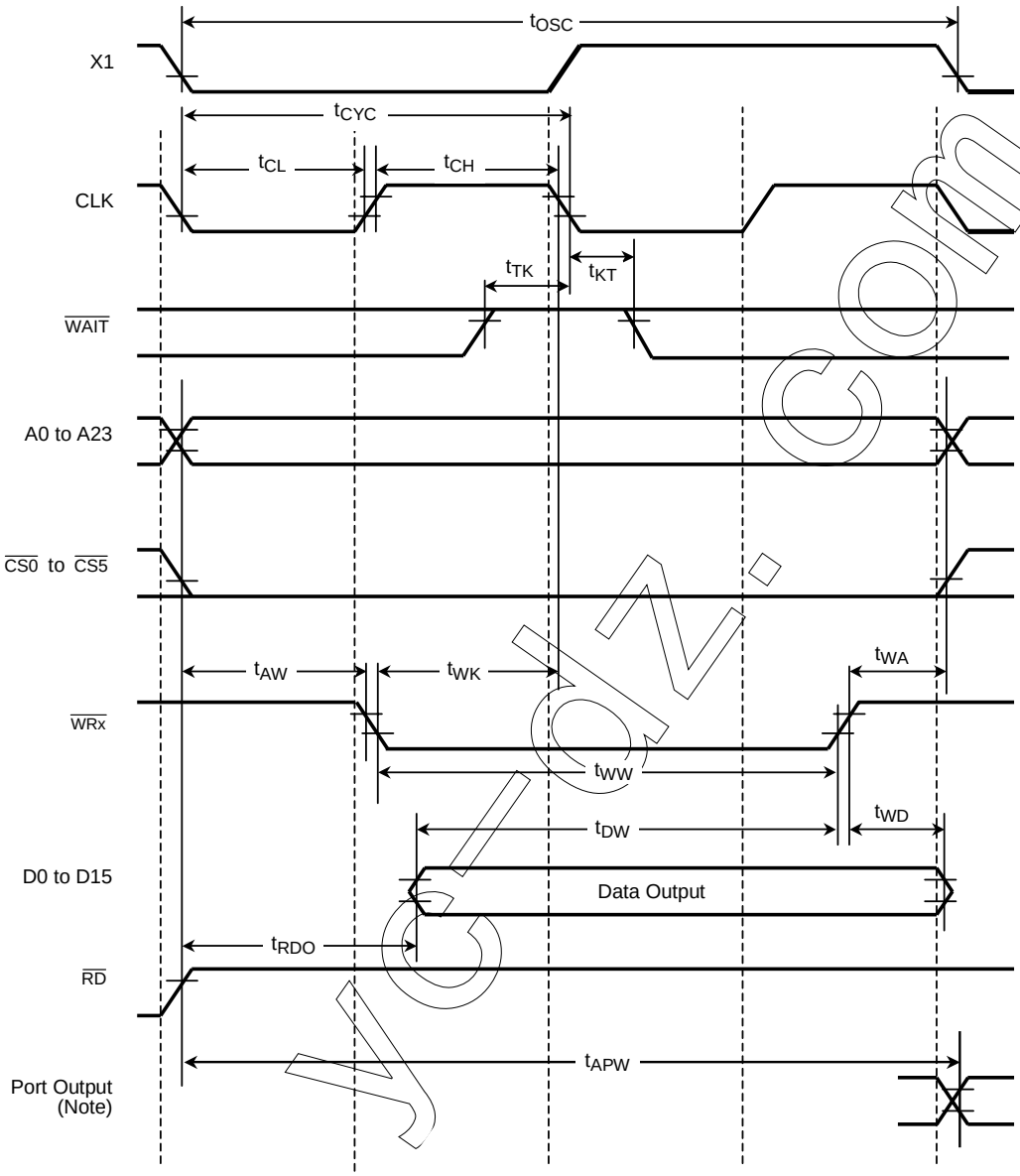
(1) Read cycle (0 waits)



Note 1: The phase relation between X1 input signal and the other signals is unsettled. The timing chart above is an example.

Note 2: Since the CPU accesses the internal area to read data from a port, the control signals of external pins such as $\overline{RD}$ and $\overline{CS}$ are not enabled. Therefore, the above waveform diagram should be regarded as depicting internal operation. Please also note that the timing and AC characteristics of port input/output shown above are typical representation. For details, contact your local Toshiba sales representative.

(2) Write cycle (0 waits)

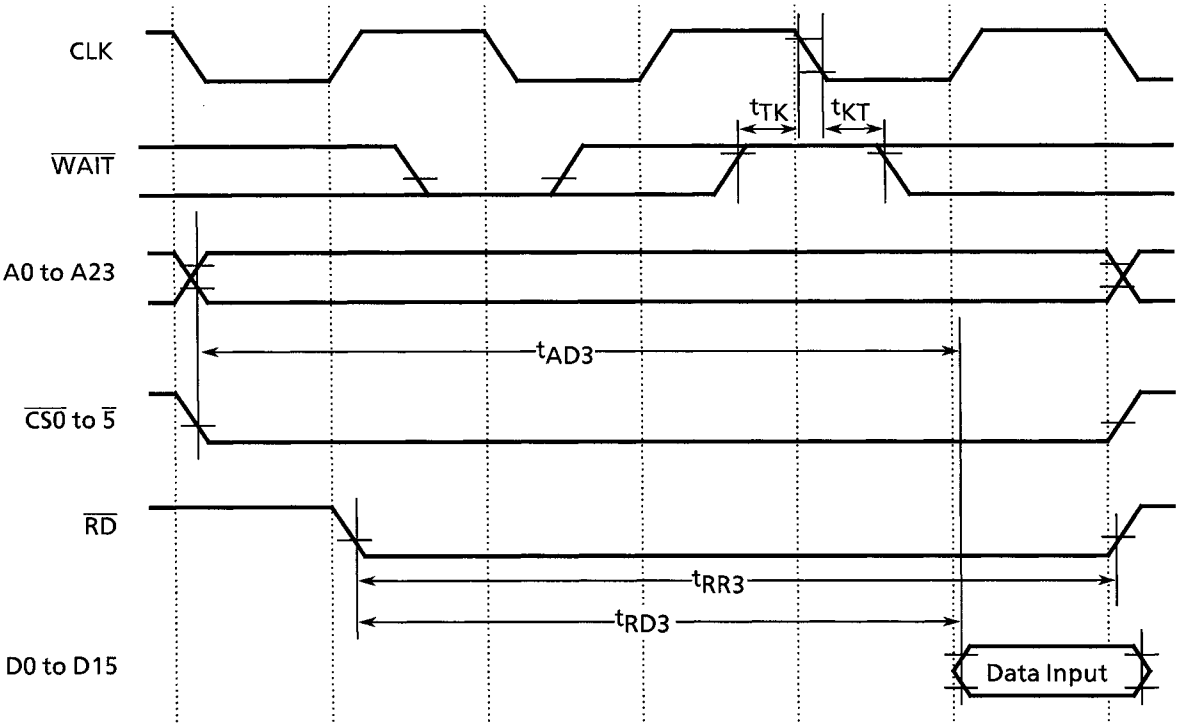


Note 1: The phase relation between X1 input signal and the other signals is unsettled. The timing chart above is an example.

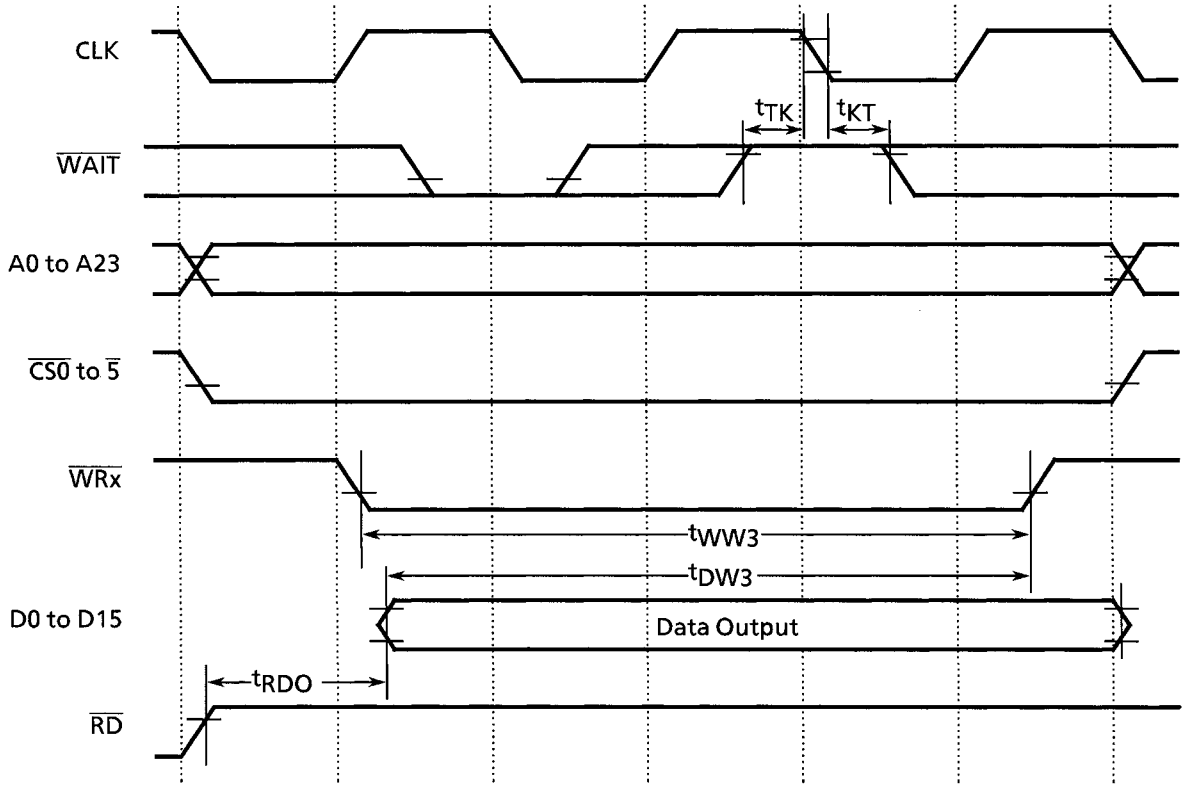
Note 2: $\overline{WRx}$ shows $\overline{WRL}$, $\overline{WRH}$.

Note 3: Since the CPU accesses the internal area to write data to a port, the control signals of external pins such as $\overline{WR}$ and $\overline{CS}$ are not enabled. Therefore, the above waveform diagram should be regarded as depicting internal operation. Please also note that the timing and AC characteristics of port input/output shown above are typical representation. For details, contact your local Toshiba sales representative.

(3) Read cycle (1 wait)



(4) Write cycle (1 wait)



4.3.2 Page ROM Read Cycle

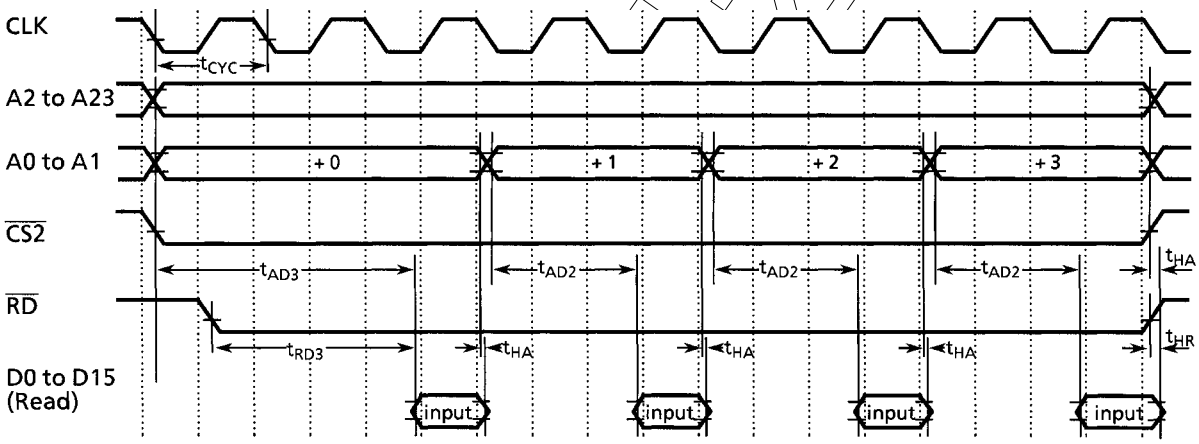
(1) 3-2-2-2 mode

No.	Symbol	Parameter	Min	Max	@20 MHz	@16 MHz	Unit
1	t_{CYC}	System Clock Period (= T)	50	62.5	50	62.5	ns
2	t_{AD2}	A0, A1 → D0 to D15 Input		1.0 × T-50	50	75	ns
3	t_{AD3}	A2 to A23 → D0 to D15 Input		3.0 × T-50	100	138	ns
4	t_{RD3}	$\overline{RD}$ Fall → D0 to D15 Input		2.5 × T-45	80	111	ns
5	t_{HA}	A0 to A23 Invalid → D0 to D15 Hold	0		0	0	ns
6	t_{HR}	$\overline{RD}$ Rise → D0 to D15 Hold	0		0	0	ns

AC Condition

Output: P4 to P6 (A0 to A23), P70 ($\overline{RD}$)
High = 2.0 V, Low = 0.8 V, CL = 50 pF
CLK, P82 ($\overline{CS2}$)
High = 2.0 V, Low = 0.8 V, CL = 50 pF
Input: P0 to P1 (D0 to D15)
High = 2.4 V, Low = 0.45 V

(2) Page ROM read cycle (3-2-2-2 mode)



4.3.3 DRAM Bus Cycle

No.	Symbol	Parameter	Min	Max	@ 20 MHz	@ 16 MHz	Unit
1	t_{CYC}	System Clock Period (= T)	50	62.5	50	62.5	ns
2	t_{RC}	$\overline{RAS}$ Cycle Time	3.00 × T		150	188	ns
3	t_{PC}	Page Mode Cycle Time	2.00 × T		100	125	ns
4-1	t_{RAC}	$\overline{RAS}$ Access Time		1.75 × T – 45	43	64	ns
4-2	t_{RAC4}	$\overline{RAS}$ Access Time @ 4 Clock Access		2.75 × T – 45	93	127	ns
5	t_{CAC}	$\overline{CAS}$ Access Time		1.00 × T – 40	10	23	ns
6-1	t_{AA}	Column Address Access Time		1.25 × T – 45	18	33	ns
6-2	t_{AA2}	Column Address Access Time @ Page Mode		2.00 × T – 45	55	80	ns
6-3	t_{AA4}	Column Address Access Time @ 4 Clock Access		2.25 × T – 45	68	96	ns
7	t_{CPA}	$\overline{CAS}$ Pre-charge Access Time		2.00 × T – 45	55	80	ns
8	t_{OFF}	Input Data Hold Time	0		0	0	ns
9	t_{RP}	$\overline{RAS}$ Pre-charge Time	1.25 × T – 20		43	58	ns
10-1	t_{RAS}	$\overline{RAS}$ Width	1.75 × T – 20		68	89	ns
10-2	t_{RAS4}	$\overline{RAS}$ Width @ 4 Clock Access	2.75 × T – 20		118	152	ns
11	t_{RSH}	$\overline{RAS}$ Hold Time	1.00 × T – 20		30	43	ns
12	t_{RHCP}	$\overline{CAS}$ Pre-charge to $\overline{RAS}$ Hold Time	2.00 × T – 20		80	105	ns
13-1	t_{CSH}	$\overline{CAS}$ Hold Time	1.75 × T – 20		68	89	ns
13-2	t_{CSH4}	$\overline{CAS}$ Hold Time @ 4 Clock Access	2.75 × T – 20		118	152	ns
14	t_{CAS}	$\overline{CAS}$ Width	1.00 × T – 20		30	43	ns
15	t_{RCD}	$\overline{RAS}$ – $\overline{CAS}$ Delay Time	0.75 × T – 17		21	30	ns
16	t_{RAD}	$\overline{RAS}$ – Column Address Delay Time		0.50 × T + 20	45	51	ns
17	t_{CRP}	$\overline{CAS}$ – $\overline{RAS}$ Pre-charge Time	1.25 × T – 20		43	58	ns
18-1	t_{CP}	$\overline{CAS}$ Pre-charge Time @ Refresh	0.50 × T – 15		10	16	ns
18-2	t_{CP2}	$\overline{CAS}$ Pre-charge Time @ Page Mode	1.00 × T – 20		30	43	ns
19	t_{ASR}	Row Address Set-up Time	1.25 × T – 40		23	38	ns
20	t_{RAH}	Row Address Hold Time	0.50 × T – 15		10	16	ns
21-1	t_{ASC}	Column Address Set-up Time	0.25 × T – 12		1	4	ns
21-2	t_{ASC2}	Column Address Set-up Time @ Page Mode	1.00 × T – 20		30	43	ns
22	t_{CAH}	Column Address Hold Time	1.00 × T – 20		30	43	ns
23	t_{AR}	Column Address Hold Time from $\overline{RAS}$	1.75 × T – 20		68	89	ns
24	t_{RAL}	Column Address $\overline{RAS}$ Read Time	1.25 × T – 20		43	58	ns
25	t_{RCS}	Read Command Set-up Time	2.00 × T – 40		60	85	ns
26	t_{RCH}	Read Command Hold Time from $\overline{CAS}$	0.50 × T – 20		5	11	ns
27	t_{RRH}	Read Command Hold Time from $\overline{RAS}$	0.50 × T – 20		5	11	ns
28	t_{WCH}	Write Command Hold Time	1.00 × T – 20		30	43	ns
29	t_{WCR}	Write Command Hold Time from $\overline{RAS}$	1.75 × T – 20		68	89	ns
30	t_{WP}	Write Command Time	1.50 × T – 20		55	74	ns
31	t_{RWL}	Write Command $\overline{RAS}$ Read Time	1.50 × T – 20		55	74	ns
32	t_{CWL}	Write Command $\overline{CAS}$ Read Time	1.50 × T – 20		55	74	ns
33	t_{DS}	Data Output Set-up Time	1.50 × T – 30		45	58	ns

No.	Symbol	Parameter	Min	Max	@20 MHz	@16 MHz	Unit
34	t_{DH}	Data Output Hold Time	1.00 × T-25		25	38	ns
35	t_{DHR}	Data Output Hold Time from $\overline{RAS}$	1.75 × T-5		83	104	ns
36	t_{WCS}	Write Command Set-up Time	0.50 × T-20		5	11	ns
37	t_{CSR}	$\overline{CAS}$ Set-up Time	0.75 × T-20		18	27	ns
38	t_{CHR}	$\overline{CAS}$ Hold Time	1.75 × T-20		68	89	ns
39	t_{RPC}	$\overline{RAS}$ Pre-charge $\overline{CAS}$ Active Time	0.50 × T-20		5	11	ns
40	t_{ROH}	$\overline{RAS}$ Hold Time from $\overline{OE}$	1.00 × T-20		30	43	ns
41	t_{OEA}	$\overline{OE}$ Access Time		1.00 × T-40	10	23	ns
42	t_{OEZ}	Input Data Hold Time from $\overline{OE}$	0		0	0	ns
43	t_{RPS}	$\overline{RAS}$ Pre-charge Time @ Release Self Refresh Cycle	2.25 × T-20		93	121	ns
44	t_{CHS}	$\overline{CAS}$ Hold Time @ Release Self Refresh Cycle	− 15		− 15	− 15	ns

AC Condition

Output: P0 to P1 (D0 to D15), P4 to P6 (A0 to A23), P70 ($\overline{RD}$), P71 to P74 ($\overline{WRx}$)

High = 2.0 V, Low = 0.8 V, CL = 50 pF

Others

High = 2.0 V, Low = 0.8 V, CL = 50 pF

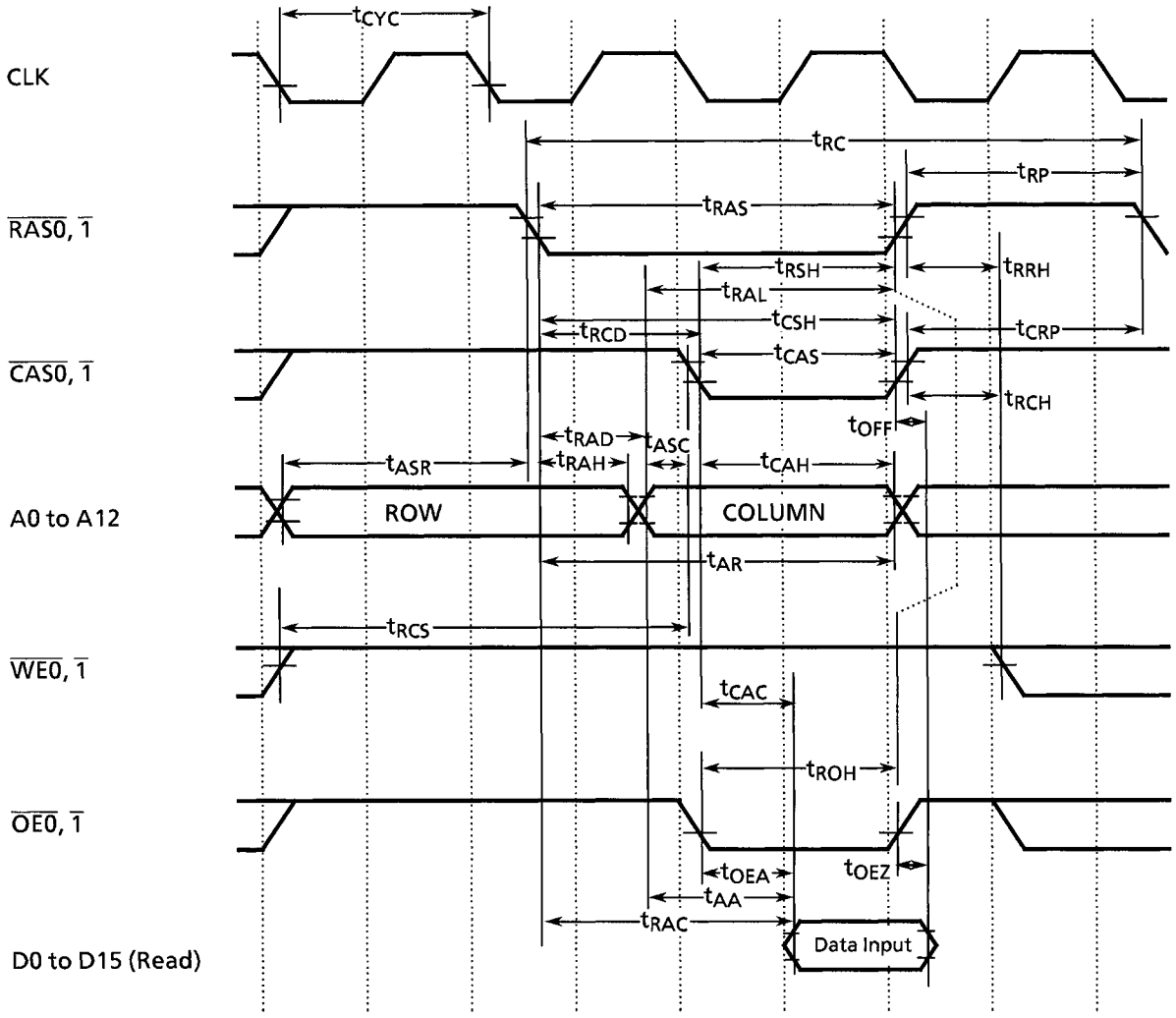
Input: P0 to P1 (D0 to D15)

High = 2.4 V, Low = 0.45 V

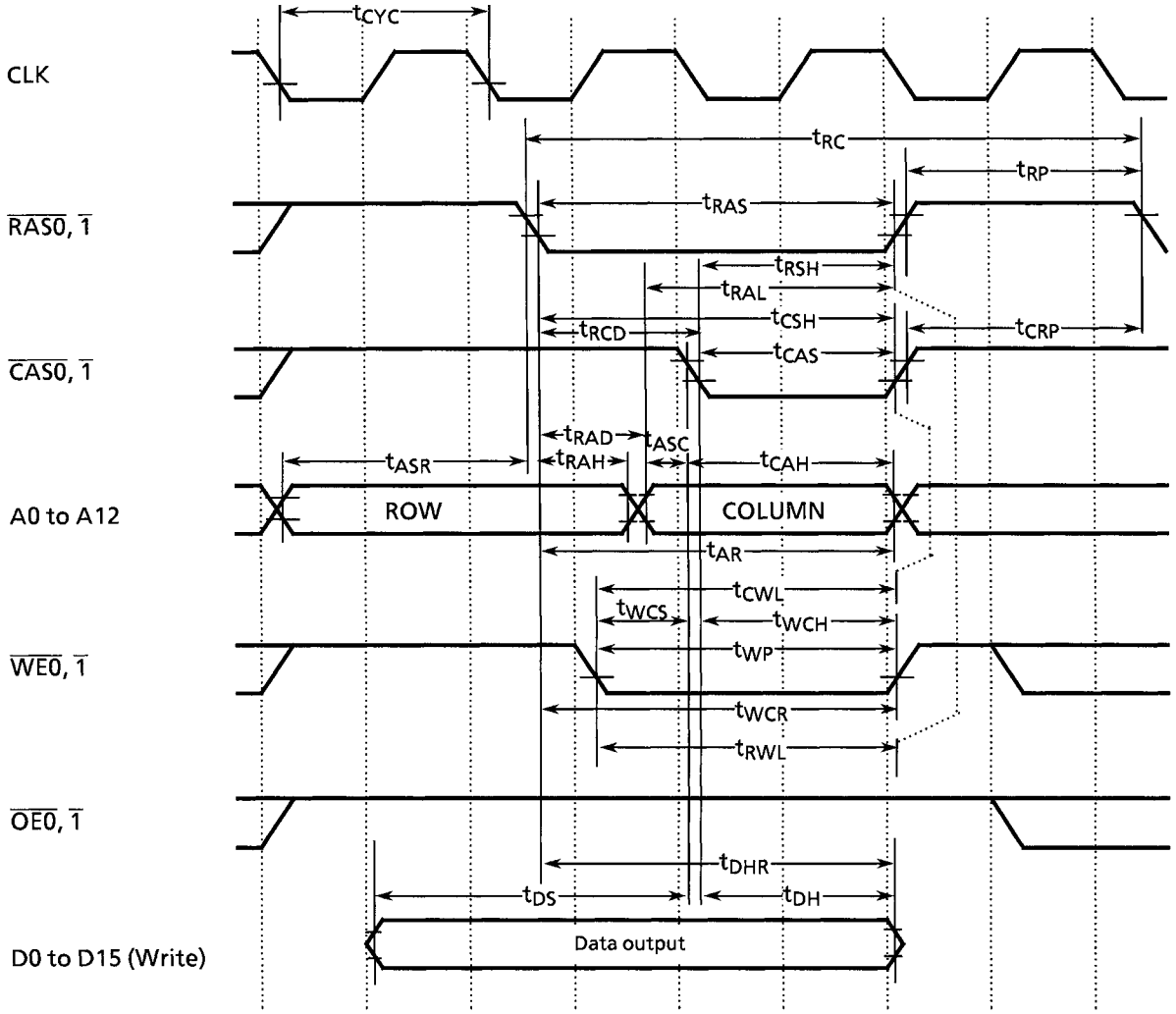
Others

High = 0.8 Vcc, Low = 0.2 Vcc

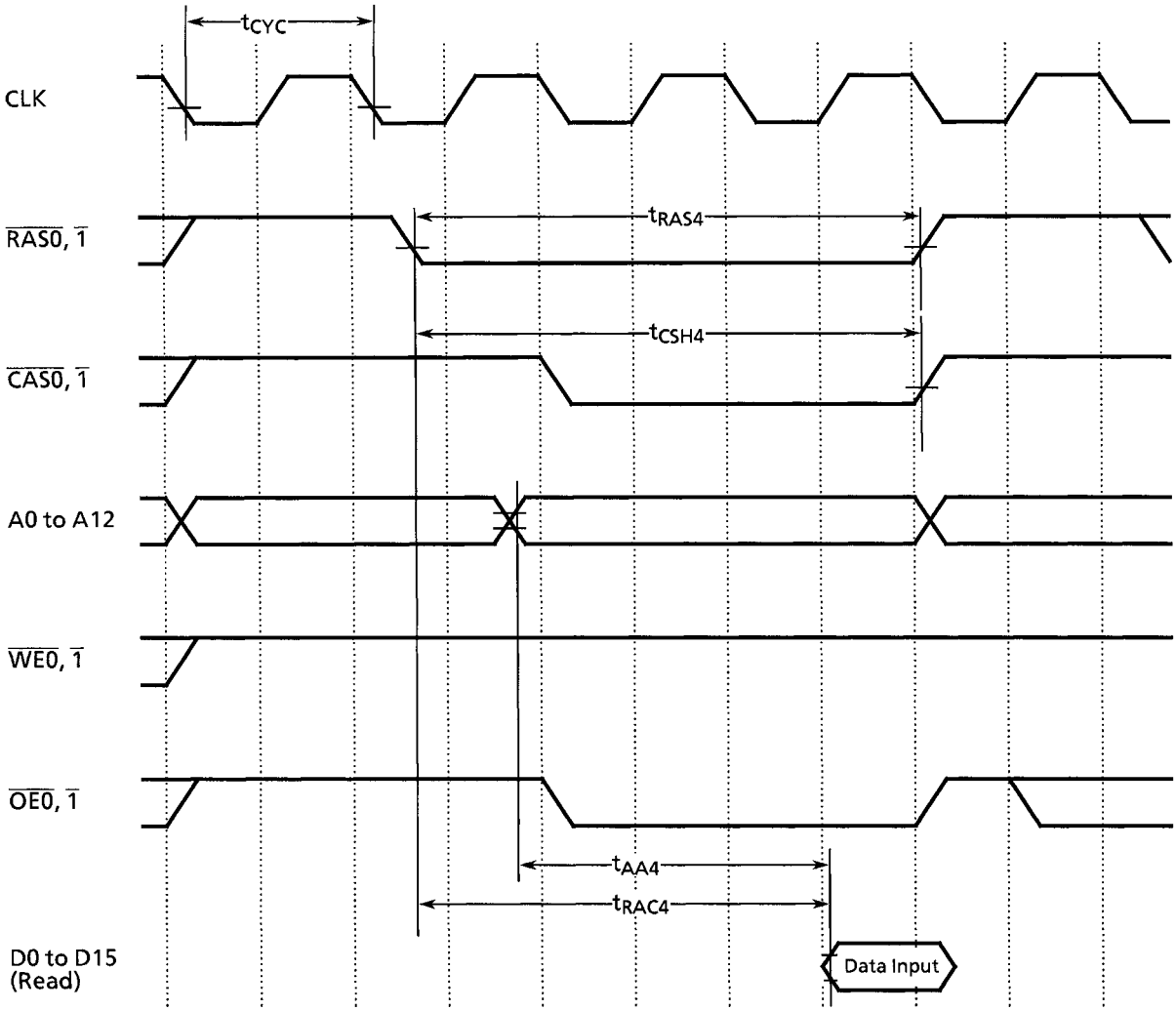
(1) DRAM read cycle (3 clock access)



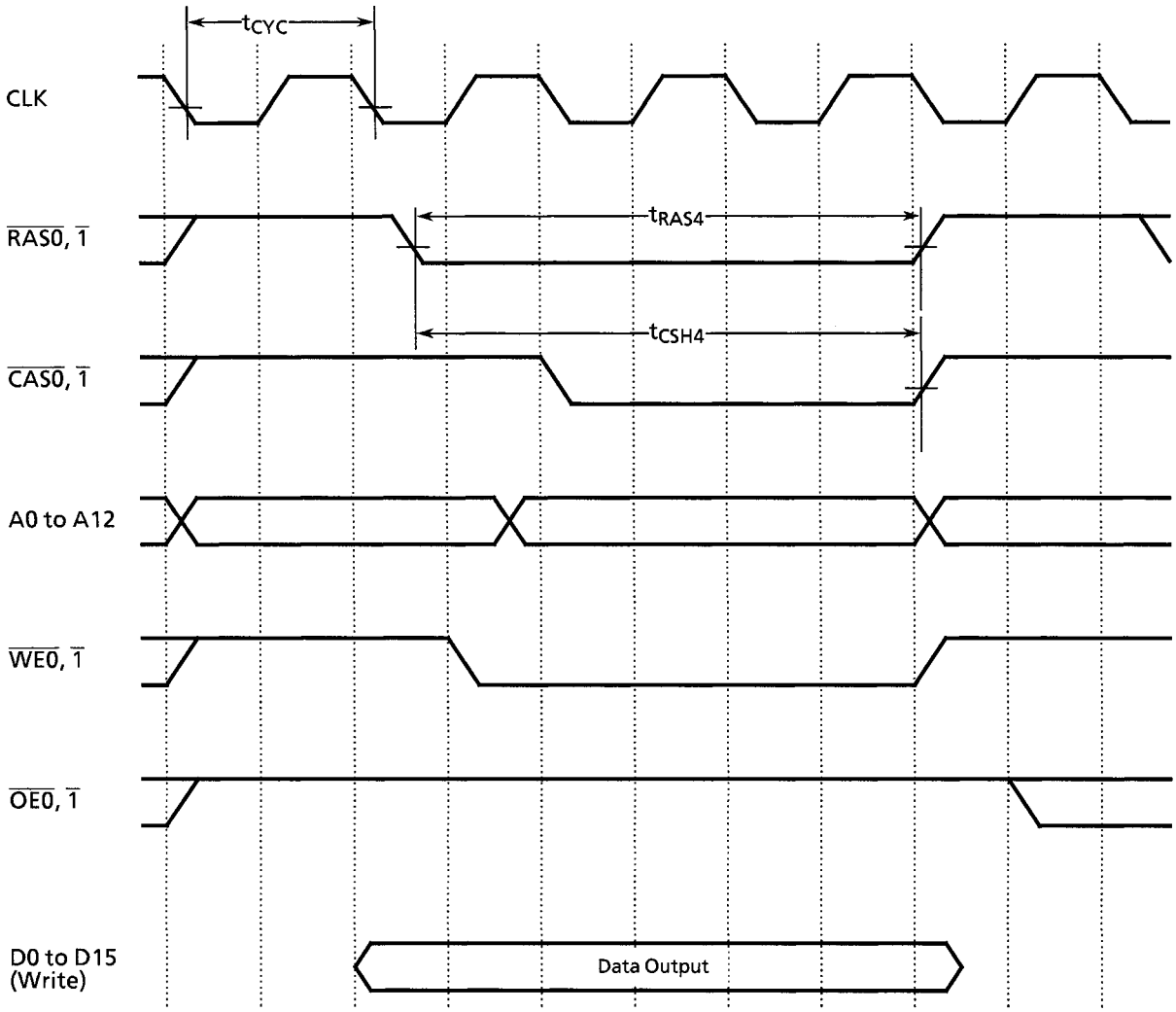
(2) DRAM write cycle (3 clock access)



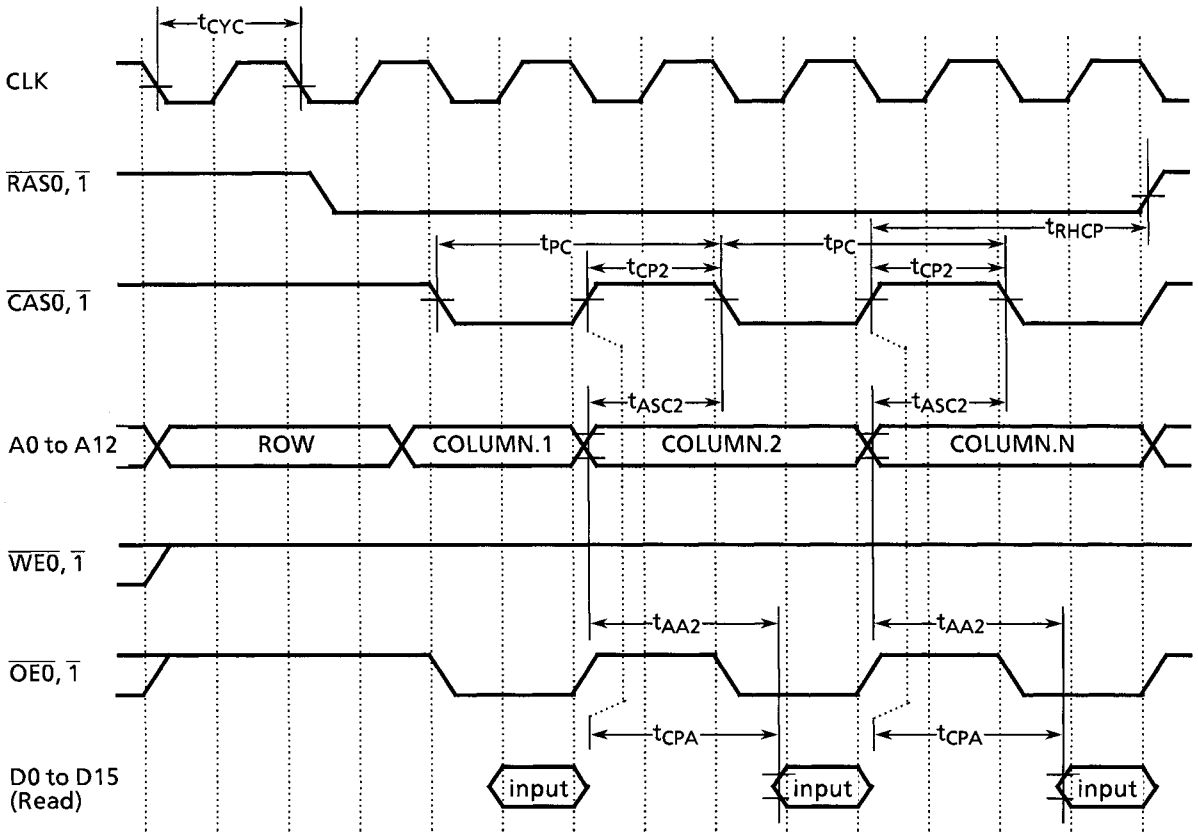
(3) DRAM read cycle (4 clock access)



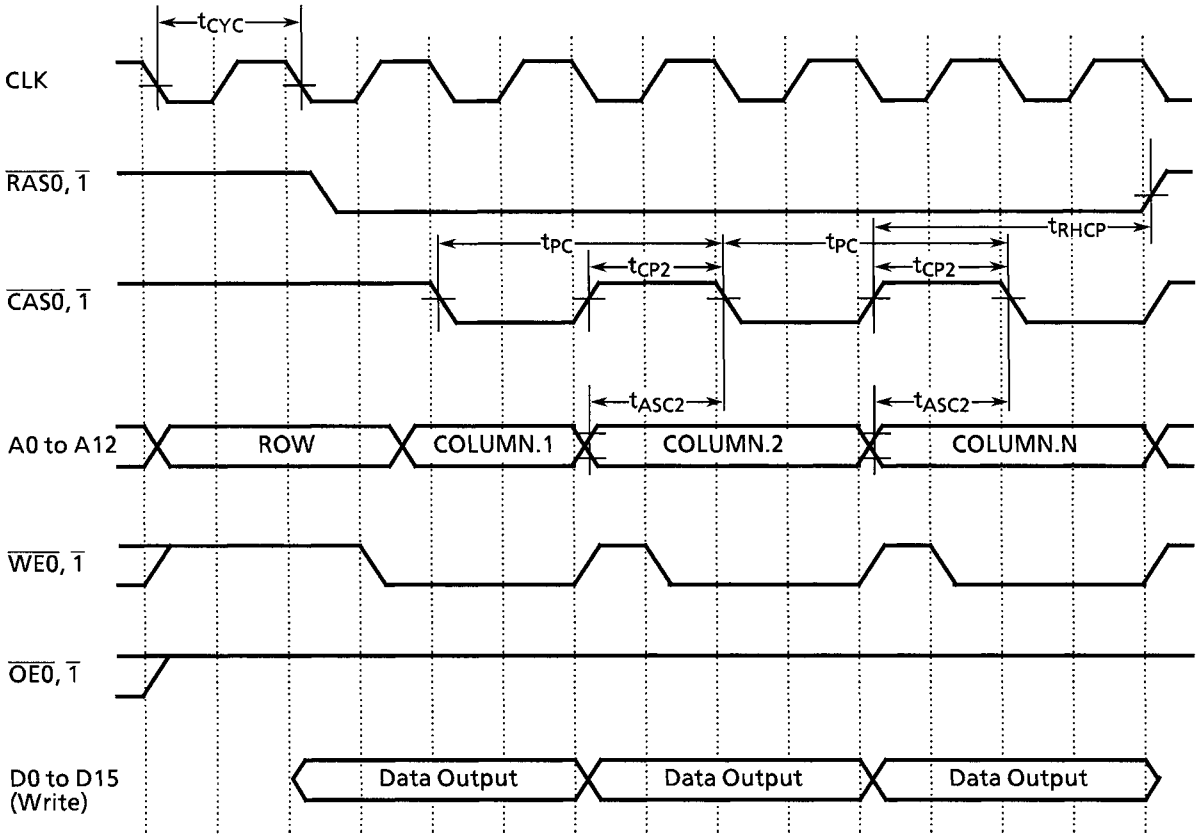
(4) DRAM write cycle (4 clock access)



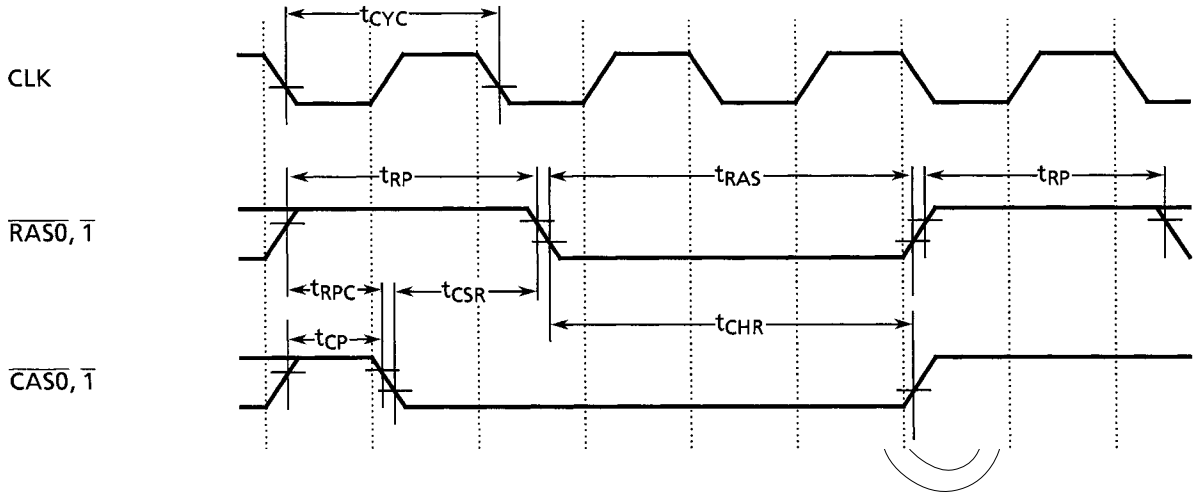
(5) DRAM page mode read cycle (3-2-2-2 mode)



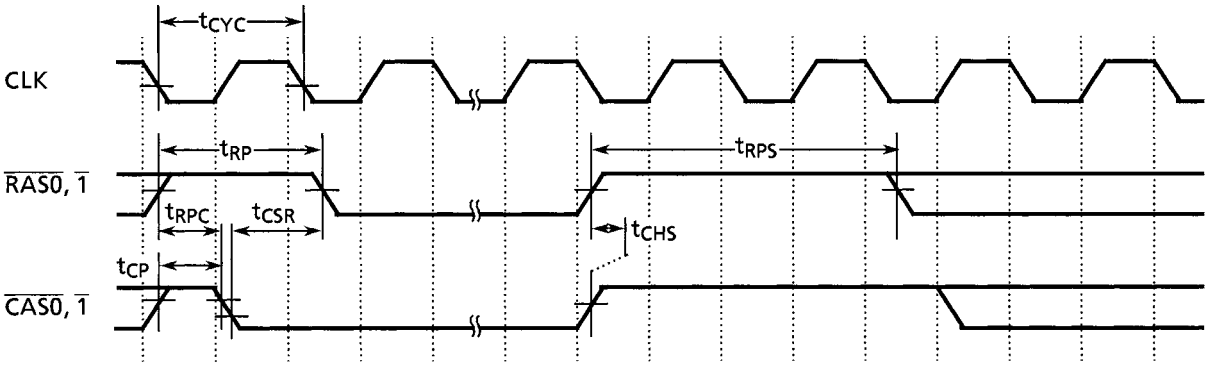
(6) DRAM page mode write cycle (3-2-2-2 mode)



(7) DRAM $\overline{CAS}$ before $\overline{RAS}$ interval refresh cycle (3 cycle mode)



(8) DRAM $\overline{CAS}$ before $\overline{RAS}$ self refresh cycle



4.4 Event Counter (TI4, TI5, TI6, TI7, TI8, TI9, TIA, TIB)

Vcc = 5 V ± 10%, TA = − 20 to 70℃ (Internal 16 to 20 MHz)

Symbol	Parameter	Variable		20 MHz		16 MHz		Unit
		Min	Max	Min	Max	Min	Max	
t_{VCK}	Clock cycle	8T + 100		500		600		ns
t_{VCKL}	Clock low-level pulse width	4T + 40		240		290		ns
t_{VCKH}	Clock high-level pulse width	4T + 40		240		290		ns

4.5 Serial Channel Timing

(1) SCLK input mode (I/O interface mode)

Vcc = 5 V ± 10%, TA = − 20 to 70℃ (Internal 16 to 20 MHz)

Symbol	Parameter	Variable		20 MHz		16 MHz		Unit
		Min	Max	Min	Max	Min	Max	
t_{SCY}	SCLK cycle	16T		0.8		1.0		μs
t_{OSS}	Output Data → Rising edge of SCLK	t_{SCY}/2 − 5T − 50		100		138		ns
t_{OHS}	SCLK rising edge → Output Data hold	5T − 100		150		213		ns
t_{HSR}	SCLK rising edge → Input Data hold	0		0		0		ns
t_{SRD}	SCLK rising edge → effective data input		t_{SCY} − 5T − 100		450		588	ns

(2) SCLK output mode (I/O interface mode)

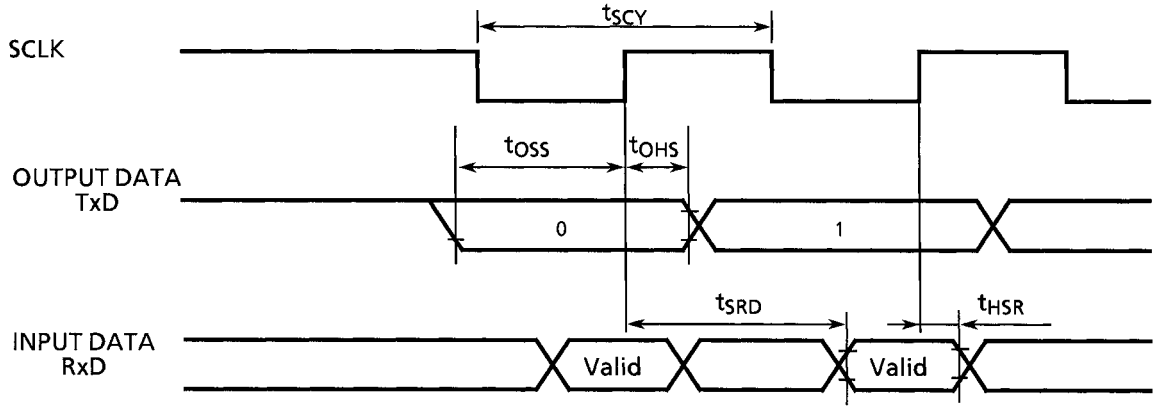
Vcc = 5 V ± 10%, TA = − 20 to 70℃ (Internal 16 to 20 MHz)

Symbol	Parameter	Variable		20 MHz		16 MHz		Unit
		Min	Max	Min	Max	Min	Max	
t_{SCY}	SCLK cycle (programmable)	16T	8192T	0.8	409.6	1.0	512	μs
t_{OSS}	Output Data → SCLK rising edge	t_{SCY} − 2T − 150		550		725		ns
t_{OHS}	SCLK rising edge → Output Data hold	2T − 80		20		45		ns
t_{HSR}	SCLK rising edge → Input Data hold	0		0		0		ns
t_{SRD}	SCLK rising edge → effective data input		t_{SCY} − 2T − 150		550		725	ns

(3) SCLK input mode (UART mode)

Vcc = 5 V ± 10%, TA = − 20 to 70℃ (Internal 16 to 20 MHz)

Symbol	Parameter	Variable		20 MHz		16 MHz		Unit
		Min	Max	Min	Max	Min	Max	
t_{SCY}	SCLK cycle	4T + 20		220		270		ns
t_{SCYL}	SCLK Low level Pulse width	2T + 5		105		130		ns
t_{SCYH}	SCLK High level Pulse width	2T + 5		105		130		ns



4.6 10-Bit AD Conversion Characteristics

Vcc = 5 V ± 10%, TA = – 20 to 70℃ (Internal 16 to 20 MHz)

Symbol	Parameter		Min	Typ	Max	Unit
VREFH	Analog reference voltage (High)		V_{CC}-0.2 V	V_{CC}	V_{CC}	V
VREFL	Analog reference voltage (Low)		V_{SS}	V_{SS}	V_{SS} + 0.2 V	
VAIN	Analog input voltage range		VREFL		VREFH	
I_{REF} (VREFL = 0 V)	Analog current for analog reference voltage					
	V_{CC} = 5V ± 10% <VREFON> = 1			0.5	1.5	mA
	V_{CC} = 5V ± 10% <VREFON> = 0			0.02	5.0	μA
Error (Quantize error of ± 0.5 LSB not included)	V_{CC} = 5V ± 10%	Total error		± 3.0	± 6	LSB

Note 1: 1LSB = (VREFH − VREFL)/1024 [V]

Note 2: Power supply current ICC from the digital power supply includes the power supply from the AVCC pin.

4.7 8-Bit DA Conversion Characteristics

Vcc = 5 V ± 10%, TA = –20 to 70°C (Internal 16 to 20 MHz)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
DAREFH	Analog reference voltage (+)		4.0		V_{CC}	V
DAREFL	Analog reference voltage (–)		V_{SS}		V_{SS}	
	Total error	RL = 2.4 KΩ		2.0	4.0	LSB
	Output voltage range	RL = 2.4 KΩ	V_{SS} + 0.5		V_{SS} – 0.5	V
	Settling time	RL = 2.4 KΩ, CL = 100 pF			5	μs
DAC output mode	Output impedance				5	Ω
	Resistive load	V_{SS} + 0.5 ≤ DAOUT ≤ V_{CC} – 0.5	2.4			kΩ

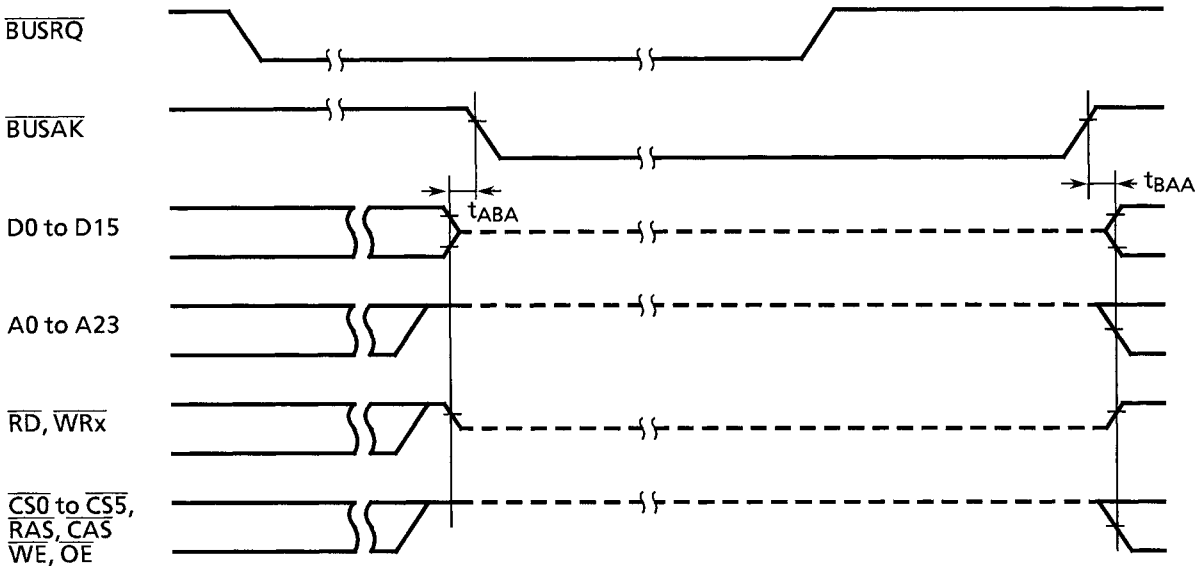
Note: RL is the resistance load of the DA converter output in.

4.8 Interrupt Operation

Vcc = 5 V ± 10%, TA = – 20 to 70℃ (Internal 16 to 20 MHz)

Symbol	Parameter	Variable		20 MHz		16 MHz		Unit
		Min	Max	Min	Max	Min	Max	
t_{INTAL}	$\overline{NMI}$, INT0 Low level Pulse width	4T		200		250		ns
t_{INTAH}	$\overline{NMI}$, INT0 High level Pulse width	4T		200		250		ns
t_{INTBL}	INT4 toINTB Low level Pulse width	8T + 100		500		600		ns
t_{INTBH}	INT4 to INTB High level Pulse width	8T + 100		500		600		ns

4.9 Bus Request/Bus Acknowledge Timing



Vcc = 5 V ± 10%, TA = – 20 to 70℃ (Internal 16 to 20 MHz)

Symbol	Parameter	Variable		20 MHz		16 MHz		Unit
		Min	Max	Min	Max	Min	Max	
t_{ABA}	Floating time to $\overline{BUSAK}$ fall	0	80	0	80	0	80	ns
t_{BAA}	Floating time to $\overline{BUSAK}$ rise	0	80	0	80	0	80	ns

Note: The bus will be released after the WAIT request is inactive, when the $\overline{BUSRQ}$ is set to “Low” during “wait” cycle.