PL-2507 Hi-Speed USB 2.0 to IDE Bridge Controller

Preliminary Datasheet

Document Revision: 0.9
Document Release: August, 2002

Prolific Technology Inc.

7F, No. 48, Sec. 3, Nan Kang Rd.

Nan Kang, Taipei 115, Taiwan, R.O.C.

Tel: 886-2-2654-6363 / Fax: 886-2-2654-6161

Email: sales@prolific.com.tw

URL: http://www.prolific.com.tw

Revision History

Revision	Description	Date
0.9	Preliminary Release – PL2507 Hi-Speed USB 2.0 to IDE Bridge Controller	August 2002

Table of Contents

1.0 Features

- Universal Serial Bus Specification 2.0 Compliant
- USB Mass Storage Class Bulk-Only Transport Specification Compliant
- AT Attachment with Packet Interface Extension (ATA/ATAPI-6) Compliant
- ATA interface support PIO mode 0 ~ 4, Multiword DMA mode 0 ~ 2, and Ultra-DMA mode 0 ~ 4 to work with ATA/ATAPI devices
- Integrated the full speed and high speed transceiver
- 5 V tolerant inputs, 3.3 V output drive
- Sufficient 4K bytes data buffer for both the downstream and upstream data transfer in optimized performance
- Support external serial EEPROM to customize vender/product related information
- Support multiple LUN (optional)
- Addition General Purpose IO pins for further customization
- On-chip 3.3v to 2.5v regulator to supply the power of 0.25 process core circuit
- Inexpensive LQ100 and LQ64 packaging available

2.0 Product Overview

The PL-2507 is a single chip USB2.0-IDE bridge controller, which is designed to perform a seamless protocol transfer between the USB and ATA interface.

It will work with full function at full speed or high speed USB transfer mode. The operating speed mode is determined by the capability of the host/hub it connected to. The PIO mode 0 to mode 5, Multi Word DMA mode 0 to mode 2, and Ultra DMA mode 0 to mode 4 are implemented to support difference IDE devices. The chip will negotiate with connected device to select the proper mode to obtain the best performance.

The chip is implemented according to the USB Bulk-Only Mass Storage Class specification ver 1.0. While the driver is default supported by most the OS so that no additional driver is needed for the bridge function.

3.0 Block Diagram

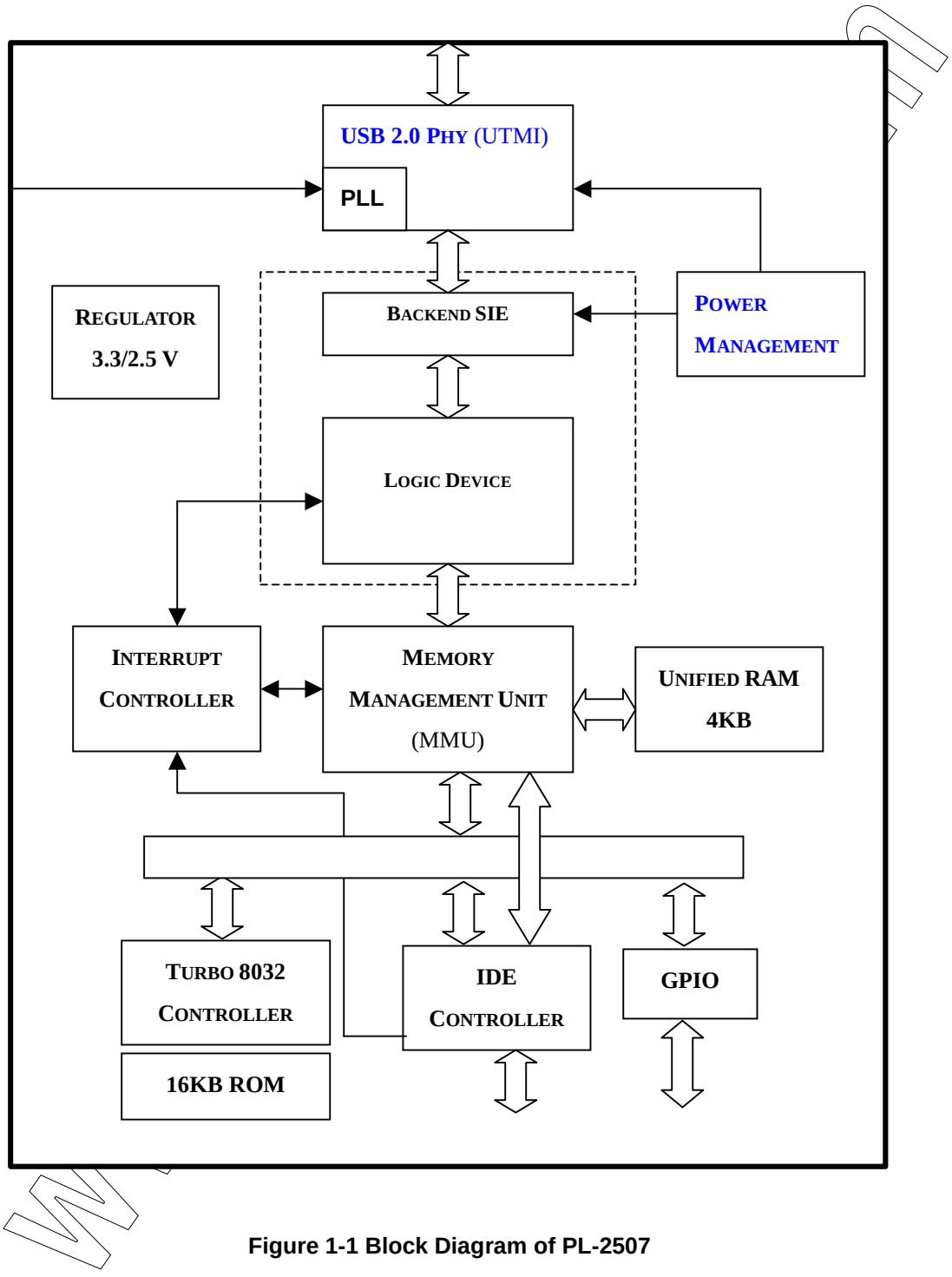

Figure 1-1 Block Diagram of PL-2507

4.0 PIN Assignment & Description

4.1 Pin Assignment for LQ 100 Package

4.1.1 USB2.0 PHY Related Pins

Table 4-1 USB2.0 PHY Related Pins

Symbol	Type	Pin No	Description
XSCI	I	69	Clock in or CMOS oscillator input.
XSCO	B	70	CMOS oscillator output.
RREF	A	73	PLL Reference level
DP	B	75	High speed DPLUS signal
DM	B	74	High speed DMINUS signal
RPU	A	77	1.5 Kohm Pull-up resistor
DPRS	B	79	Full speed DPLUS signal
DMRS	B	78	Full speed DMINUS signal
VCCK	P	67	Digital Power 2.5v
GNDK	P	68	Digital Ground
AVCC1, AVCC2, AVCC3	P	71, 80, 82	Analog Power 3.3v for on-chip PHY
AGND1, AGND2, AGND3	P	72 76 81	Analog Ground for on-chip USB PHY.

4.1.2 Internal 8032 Related Pins

Table 4-2 Internal 8032 Related Pins

Symbol	Type	Pin No	Description
P1[7:0]	B	8,10, 13,31, 34,37, 39,42	Port 1 of 8032. Can be used as firmware controlled GPIO
P3[1:0]	B	49,46	Port 3 (TXD and RXD) of 8032. Can be used as firmware controllable GPIO pins

4.1.3 IDE Interface Related Pins

Table 4-3 IDE Interface Related Pins

Symbol	Type	Pin No	Description
DD[15:0]	B	26,29, 32,35, 40,44, 47,51, 52,48, 45,41, 36,33, 30,27	16 pins Data bus of IDE interface
DA[2:0]	T	7,9,11	DA, Data Address pins of IDE interface. Will be in high impedance state until USB connection.
CSJ[1:0]	T	3,5	CS_, Chip Select pins of IDE interface. Will be in high-impedance state until USB connection.
USB_PWR	I	95	Power signal from USB connection.
ATA_RSTJ	T	24	Hardware reset pin of IDE interface. Will be in high impedance state until USB connection.
DIOWJ	T	22	ATA control. Will be in high impedance state until USB connection.
DIORJ	T	21	ATA control. Will be in high impedance state until USB connection.
DMACKJ	T	19	ATA control. Will be in high impedance state until USB connection.
IORDY	I	17	ATA control.
INTRQ	I	15	ATA control.
DMARQ	I	12	ATA control.

4.1.4 SGPIO

Table 4-4 SGPIO

Symbol	Type	Pin No	Description
SGPIO[7:0]	B	89,91, 94,97, 99,100, 4,6	Special GPIO. Can be configured pin by pin. Each pin can be configured as remote wakeup trigger to the system or interrupt trigger to the internal controller.

4.1.5 System Pins

Table 4-5 System Pins

Symbol	Type	Pin No	Description
REGPWR	P	86	3.3v Power pin for on-chip 3.3v/2.5v regulator
REGGND	P	85	Ground pin for on-chip 3.3v/2.5v regulator
REGVO	P	87	2.5v power output of 3.3v/2.5v regulator
RESETJ	I	58	External reset pin. Low active.
SCL	O	56	Clock pin of two wire serial EEPROM interface
SDA	B	55	Data pin of two wire serial EEPROM interface
TEST	I	59	Chip Test mode enable. It shall be NC or tie to Ground
SYS_TEST0	I	60	System test pin. Must leave it as NC or tie to Ground
SYS_TEST1	I	12	System test pin. Must tie to Ground
SYS_CFG	I	92	System configuration pin. Must tie to Ground during normal operation. If set to high, the chip is capable to program the serial EEPROM online.
EX_SIG0	I	96	External signal input pin. Must tie to Ground if not used
EX_SIG1	I	1	External signal input pin. Must tie to Ground if not used
IDEBLK_EN	I	88	IDE block enable. If low, the ATA control and Data Bus will all in high impedance state. It shall be set to high for proper function.
VCC	P	18,50,98	3.3v Power pins
VCCK	P	16,38,93	2.5v Power pins
GND	P	25,53,90	Digital ground pins
NC		2,20,23, 28,43,54, 57,61,62, 63,64,65, 66,83,84	No connection.

4.2 Pin Assignment for LQ64 Package

4.2.1 USB2.0 PHY Related Pins

Table 4-2-1 USB2.0 PHY Related Pins

Symbol	Type	Pin No	Description
XSCI	I	42	Clock in or CMOS oscillator input.
XSCO	B	43	CMOS oscillator output.
RREF	A	46	PLL Reference level
DP	B	48	High speed DPLUS signal
DM	B	47	High speed DMINUS signal
RPU	A	50	1.5 Kohm Pull-up resistor
DPRS	B	52	Full speed DPLUS signal
DMRS	B	51	Full speed DMINUS signal
VCCK	P	40	Digital Power 2.5v
GNDK	P	41	Digital Ground
AVCC1, AVCC2, AVCC3	P	44, 53, 55	Analog Power 3.3v for on-chip PHY
AGND1, AGND2, AGND3	P	45, 49, 54	Analog Ground for on-chip USB PHY.

4.2.2 IDE Interface Related Pins

Table 4-2-2 IDE Interface Related Pins

Symbol	Type	Pin No	Description
DD[15:0]	B	17,19, 21,23, 26,28, 30,33, 34,31, 29,27, 24,22, 20,18	16 pins Data bus of IDE interface
DA[2:0]	T	4,5,6	DA, Data Address pins of IDE interface. Will be in high impedance state until USB connection.
CSJ[1:0]	T	2,3	CS_, Chip Select pins of IDE interface. Will be in high-impedance state until USB connection.
USB_PWR	I	62	Power signal from USB connection.
ATA_RSTJ	T	15	Hardware reset pin of IDE interface. Will be in high impedance state until USB connection.

4.2.2 IDE Interface Related Pins

Table 4-2-2 IDE Interface Related Pins

Symbol	Type	Pin No	Description
DIOWJ	T	14	ATA control. Will be in high impedance state until USB connection.
DIORJ	T	13	ATA control. Will be in high impedance state until USB connection.
DMACKJ	T	12	ATA control. Will be in high impedance state until USB connection.
IORDY	I	10	ATA control.
INTRQ	I	9	ATA control.
DMARQ	I	8	ATA control.

4.2.3 System Pins

Table 4-2-3 System Pins

Symbol	Type	Pin No	Description
REGPWR	P	57	3.3v Power pin for on-chip 3.3v/2.5v regulator
REGGND	P	56	Ground pin for on-chip 3.3v/2.5v regulator
REGVO	P	58	2.5v power output of 3.3v/2.5v regulator
RESETJ	I	38	External reset pin. Low active.
SCL	O	37	Clock pin of two wire serial EEPROM interface
SDA	B	36	Data pin of two wire serial EEPROM interface
TEST	I	39	Chip Test mode enable. It shall be NC or tie to Ground
SYS_CFG	I	61	System configuration pin. Must tie to Ground during normal operation. If set to high, the chip is capable to program the serial EEPROM online.
EX_SIG0	I	63	External signal input pin. Must tie to Ground if not used
EX_SIG1	I	1	External signal input pin. Must tie to Ground if not used
SYS_TEST1	I	7	System test pin. Must tie to Ground
IDEBLK_EN	I	59	IDE block enable. If low, the ATA control and Data Bus will all in high impedance state. It shall be set to high for proper function.
VCC	P	11,32, 64	3.3v Power pins
VCCK	P	25	2.5v Power pins
GND	P	16,35, 60	Digital ground pins

5.0 USB Port Descriptor for PL-2507

PL-2507 supports the following standard USB descriptors:

- Device descriptor.
- Configuration descriptor that supports one interface.
- String descriptors. Three string descriptors are implemented namely, language ID, Vender String, and Product String.

5.1 Device Descriptor

Table 5-1 Device Descriptor

Offset	Field	Size	Value	Description
0	bLength	Byte	12h	Size of this descriptor in bytes.
1	bDescriptorType	Byte	01h	DEVICE descriptor type.
2	bcdUSB	Word	0200h	USB Specification version 2.0
4	bDeviceClass	Byte	00h	Interface Specific.
5	bDeviceSubclass	Byte	00h	Interface Specific.
6	bDeviceProtocol	Byte	00h	Interface Specific.
7	wMaxPacketSize0	Byte	40h	Maximum packet size for endpoint 0 is 64.
8	idVendor	Word	067Bh	Vendor ID for Prolific Technologies.(1)
10	idProduct	Word	2507h	Product ID for PL-2507. (1)
12	bcdDevice	Word	0100h	Device Release 1.0. (1)
14	iManufacturer	Byte	01h	String index 1 describes manufacturer. (2)
15	iProduct	Byte	02h	String index 2 describes product. (3)
16	iSerialNumber	Byte	00h	No serial number string
17	bNumConfigurations	Byte	01h	One possible configuration

Notes:

(1) – These default values shown here could be modified by external EEPROM;

(2) – The default string is "Prolific Technology Inc." in UNICODE format and could be replaced by the contents of external EEPROM;

(3) – The default string is "ATAPI-6 Bridge Controller" in UNICODE format and could be replaced by the contents of external EEPROM.

5.2 Configuration Descriptor

Table 5-2 Configuration Descriptor

Offset	Field	Size	Value	Description
0	bLength	Byte	09h	Size of this descriptor in bytes.
1	bDescriptorType	Byte	02h	CONFIGURATION descriptor type.
2	bTotalLength	Word	0020h	32 bytes of all INTERFACE & ENDPOINT.
4	bNumInterfaces	Byte	01h	The PL-2307 has one interface.
5	bConfigurationValue	Byte	01h	Value to write to the Device Configuration Register (DCR) to select this configuration.
6	iConfiguration	Byte	00h	No string description for this.
7	bmAttributes	Byte	C0h	Configuration characteristics: [4] Self-Powered & No Remote Wakeup.
8	MaxPower	Byte	32h	Maximum power consumption is 100 mA.[5]

Notes:

(4) (5) – The default value could be replaced by the contents of external EEPROM.

5.3 Interface Descriptors

Table 5-3 Interface Descriptors

Offset	Field	Size	Value	Description
0	bLength	Byte	09h	Size of this descriptor in bytes.
1	bDescriptorType	Byte	04h	INTERFACE descriptor type.
2	bInterfaceNumber	Byte	00h	Interface 0.
3	bAlternateSetting	Byte	00h	Alternate 0.
4	bNumEndpoints	Byte	02h	Supports endpoint 0, 1, and 2.
5	bInterfaceClass	Byte	08h	MASS STORAGE class.
6	iInterfaceSubClass	Byte	06h	SCSI transparent commend set
7	bInterfaceProtocol	Byte	50h	Bulk-Only Transport protocol.
8	iInterface	Byte	00h	No String descriptor for this interface.

5.4 Endpoint Descriptors

5.4.1 In High speed mode

Table 5-4-1a Bulk Out Endpoint Descriptor (Endpoint 1)

Offset	Field	Size	Value	Description
0	bLength	Byte	07h	Size of this descriptor in bytes.
1	bDescriptorType	Byte	05h	ENDPOINT descriptor type.
2	bEndpointAddress	Byte	01h	Out Endpoint 1.
3	bmAttributes	Byte	02h	BULK Endpoint.
4	wMaxPacketSize	Word	0200h	Maximum packet size is 512.
6	bInterval	Byte	00h	N/A

Table 5-4-1b Bulk In Endpoint Descriptor (Endpoint 2)

Offset	Field	Size	Value	Description
0	bLength	Byte	07h	Size of this descriptor in bytes.
1	bDescriptorType	Byte	05h	ENDPOINT descriptor type.
2	bEndpointAddress	Byte	82h	In Endpoint 2.
3	bmAttributes	Byte	02h	BULK Endpoint
4	wMaxPacketSize	Word	0200h	Maximum packet size is512.
6	bInterval	Byte	00h	N/A

5.4.2 In Full speed mode

Table 5-4-2a Bulk Out Endpoint Descriptor (Endpoint 1)

Offset	Field	Size	Value	Description
0	bLength	Byte	07h	Size of this descriptor in bytes.
1	bDescriptorType	Byte	05h	ENDPOINT descriptor type.
2	bEndpointAddress	Byte	01h	Out Endpoint 1.
3	bmAttributes	Byte	02h	BULK Endpoint.
4	wMaxPacketSize	Word	0040h	Maximum packet size is 512.
6	bInterval	Byte	00h	N/A

Table 5-4-1b Bulk In Endpoint Descriptor (Endpoint 2)

Offset	Field	Size	Value	Description
0	bLength	Byte	07h	Size of this descriptor in bytes.
1	bDescriptorType	Byte	05h	ENDPOINT descriptor type.
2	bEndpointAddress	Byte	82h	In Endpoint 2.
3	bmAttributes	Byte	02h	BULK Endpoint
4	wMaxPacketSize	Word	0040h	Maximum packet size is512.
6	bInterval	Byte	00h	N/A

5.5 Device_Qualifier Descriptors

Table 5-5 Device Qualifier Descriptors

Offset	Field	Size	Value	Description
0	bLength	Byte	0Ah	Size of this descriptor in bytes.
1	bDescriptorType	Byte	06h	DEVICE Qualifier descriptor type.
2	bcdUSB	Word	0200h	USB Specification version 2.0
4	bDeviceClass	Byte	00h	Interface Specific.
5	bDeviceSubclass	Byte	00h	Interface Specific.
6	bDeviceProtocol	Byte	00h	Interface Specific.
7	wMaxPacketSize0	Byte	40h	Maximum packet size for endpoint 0 is 64.
8	bNumConfigurations	Byte	01h	Number of other-speed configurations.
9	bReserved	Byte	00h	Reserved for future use, must be zero

5.6 Other_Speed_Configuration Descriptors

Table 5-6 Other Speed Configuration Descriptors

Offset	Field	Size	Value	Description
0	bLength	Byte	09h	Size of this descriptor in bytes.
1	bDescriptorType	Byte	07h	CONFIGURATION descriptor type.
2	bTotalLength	Word	0020h	32 bytes of all INTERFACE & ENDPOINT.
4	bNumInterfaces	Byte	01h	Number of interface supported, one interface.
5	bConfigurationValue	Byte	01h	Value to write to the Device Configuration Register (DCR) to select this configuration.
6	iConfiguration	Byte	00h	No string description for this.
7	bmAttributes	Byte	C0h	Configuration characteristics: Self-Powered & No Remote Wakeup.
8	MaxPower	Byte	32h	Maximum power consumption is 100 mA

6.0 Device Control Requests

PL-2507 supports three types of requests:

- Standard USB device request set, which perform general functions for supporting the bus and bus related functions.
- Mass Storage class request set, which is an USB class defined to implement storage device over USB protocol.
- Vender specific requests, which are implemented to provide additional control and verification method upon the optional external serial EEPROM.

6.1 Standard Device Control Requests

- SET_FEATURE/CLEAR_FEATURE: Supports DEVICE_REMOTE_WAKEUP and ENDPOINT_STALL for all endpoints. Requests with incorrect bmRequestType or endpoint number will be stalled.
- SET_CONFIGURATION/GET_CONFIGURATION
- GET_INTERFACE/SET_INTERFACE
- SET_ADDRESS
- GET_STATUS
- GET_DESCRIPTOR

SET_DESCRIPTOR and SYNCH_FRAME are not supported by the PL-2507.

6.2 Class Specific Requests

Command	bmType	bRequest	wValue	wIndex	wLength	Data	Note
Bulk-Only Mass Storage Reset	0x21	0xFF	0	interface	0	None	
Get Max LUN	0xA1	0xFE	0	interface	1	1 byte	

6.2.1 Bulk-Only Mass Storage Reset

This request is used to reset the mass storage device and its associated interface. This class-specific request shall ready the device for the next CBW from the host. The host shall send this request via the default pipe to the device. The device shall preserve the value of its bulk data toggle bits and endpoint STALL conditions despite the Bulk-Only Mass Storage Reset. The device shall NAK the status stage of the device request until the Bulk-Only Mass Storage Reset is complete.

6.2.2 Get Max LUN

The device may implement several logical units that share common device characteristics. The host uses bCBWLUN (see 5.1 Command Block Wrapper (CBW)) to designate which logical unit of the device is the destination of the CBW. The Get Max LUN device request is used to determine the number of logical units supported by the device. Logical Unit Numbers on the device shall be numbered contiguously starting from LUN 0 to a maximum LUN of 15 (Fh).

6.3 Vender Specific Requests

Command	bmType	bRequest	wValue	wIndex	wLength	Data	Note
SET_EEPROM_STR	0x41	0x05	0	0	BL	Data String	
GET_EEPROM_STR	0xC1	0x06	0	0	BL	Data String	

Note: *The BL shall not exceed 255, the requests will be stalled otherwise.*

6.3.1 SET_EEPROM_STRING Request

The PL-2507 supports the option to store the Vendor ID, Product ID, and Device Release Number in device descriptor, Attributes and Max Power setting in configuration descriptor, and Strings of String Descriptor in an external Serial EEPROM. The PL-2507 will detect the existence of the EEPROM automatically after reset. If the first word retrieved from the EEPROM matches the predefined check byte, 0x067B, it would use the data from this external EEPROM instead of the data from internal ROM.

The vendor specific SET_EEPROM_STRING request is used to change the contents of the EEPROM. The data part of this request is written to the EEPROM from address 0 all the way up to address 255. Therefore, it is necessary for the software to prepare the whole table first and then write it to the EEPROM in one single SET_EEPROM_STRING request.

6.3.2 GET_EEPROM_STRING Request

This request allows driver on host side retrieve the whole data table resides in the external serial EEPROM. The returned data is retrieved starting from address 0 to the end of data table from EEPROM. It is mostly used as a verification method to check the data integrity of the previous write.

6.3.3 Data Structure of EEPROM Content

The EEPROM is organized as following:

Address	Content	Note
1:0	Check Word – 0x067B (Predefined constant)	
3:2	Vendor ID (idVendor field of Device Descriptor)	
5:4	Product ID (idProduct field of Device Descriptor)	
7:6	Device Release Number (bdcDevice field of Device Descriptor)	
8	Attributes (bmAttributes field of Configuration Descriptor)	
9	Max Power (MaxPower field of Configuration Descriptor)	
15:10	Reserved for future use. Must be “0”	
255:16	String Descriptor Table	

The String Descriptor table is a linked data structure that holds all string descriptors recognized by this chip in the order of its index. The first entry, String 0, represents the Language ID, as defined by the USB specification. The second entry, String 1, is the Manufacturer Descriptor, as defined by the Device Descriptor of PL-2507. The third and forth entries, String 2 and 3, are the Product Descriptor and Serial Number, respective, also defined by the Device Descriptor. The user has the option to define String 4, 5, and 6 for their own private use. Each of the these String Descriptor Entries is of the following data structure:

Offset	Field	Size	Value	Note
0	bLength	1	Length of the string plus 2, i.e. (N + 2).	
1	bDescriptorType	1	03h – STRING Descriptor type.	
2	bString	N	UNICODE encoded string.	

The last entry of this table must have bLength of 0 to indicate the end of this table. If the host tries to access to the string descriptor beyond the last one, a zero-length data will be returned. The following table shows one example of valid EEPROM contents.

Offset	Content	Note
0:1	Check Word – 0x067B	Constant
2:3	Vendor ID – 0x067B	
4:5	Product ID – 0x2507	
6:7	Device Release Number – 0x0100	
8		
9		
15:10		

Offset	Content	Note
16	0x04	String Index 0 (4 Bytes)
17	0x03	
19:18	0x0409	Language ID for English (United States).
20	0x32	String Index 1 (50 Bytes)
21	0x03	
69:22	‘P’, 0x00, ‘r’, 0x00, ‘o’, 0x00, ‘l’, 0x00, ‘i’, 0x00, ‘f’, 0x00, ‘i’, 0x00, ‘c’, 0x00, ‘ ‘, 0x00, ‘T’, 0x00, ‘e’, 0x00, ‘c’, 0x00, ‘h’, 0x00, ‘n’, 0x00, ‘o’, 0x00, ‘l’, 0x00, ‘o’, 0x00, ‘g’, 0x00, ‘y’, 0x00, ‘ ‘, 0x00, ‘I’, 0x00, ‘n’, 0x00, ‘c’, 0x00, ‘.’ , 0x00	“Prolific Technology Inc.” – manufacturer description. 0x00 is padded for UNICODE.
70	0x34	String Index 2 (52 Bytes)
71	0x03	
121:72	‘A’, 0x00, ‘T’, 0x00, ‘A’, 0x00, ‘P’, 0x00, ‘I‘, 0x00, ‘-’, 0x00, ‘6’, 0x00, ‘ ’, 0x00, ‘B’, 0x00, ‘r‘, 0x00, ‘i’, 0x00, ‘d’, 0x00, ‘g’, 0x00, ‘e’, 0x00, ‘ ’, 0x00, ‘C’, 0x00, ‘o’, 0x00, ‘n’, 0x00, ‘t’, 0x00, ‘r’ , 0x00, ‘o’, 0x00, ‘l’, 0x00, ‘l’, 0x00, ‘e’, 0x00, ‘r’, 0x00	“ATAPI-6 Bridge Controller” – device description. 0x00 is padded for UNICODE.
122	0x0A	String Index 3 (10 bytes)
123	0x03	
131:124	‘0’, 0x00, ‘1’, 0x00, ‘2’, 0x00, ‘3’, 0x00	“3210” – serial number,
132	0x00	End of String Descriptor Table.

The user could also define other strings, 4 to 6, to hold useful information for the drivers and/or applications, such as software authorization codes, public key for password encryption, symbolic names, just to name a few. However, the total length of this table must not exceed 256 bytes, the supported maximum size of external EEPROM.

7.0 DC Characteristics

{ no data available at this moment }

8.0 Outline Diagram

8.1 LQ100 Package

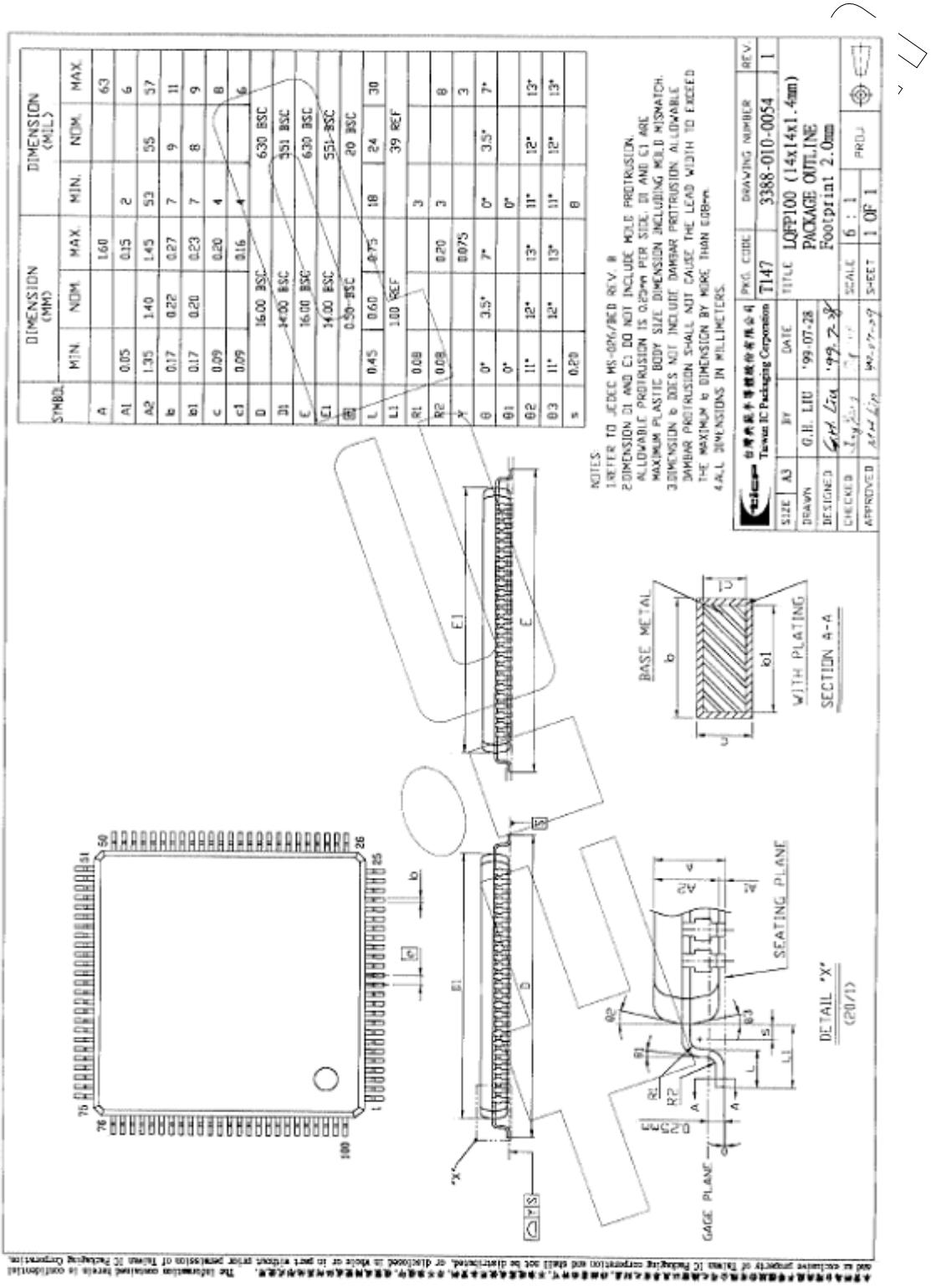

Figure 1-2 Outline Diagram of PL-2507 LQFP100

8.2 LQ64 Package

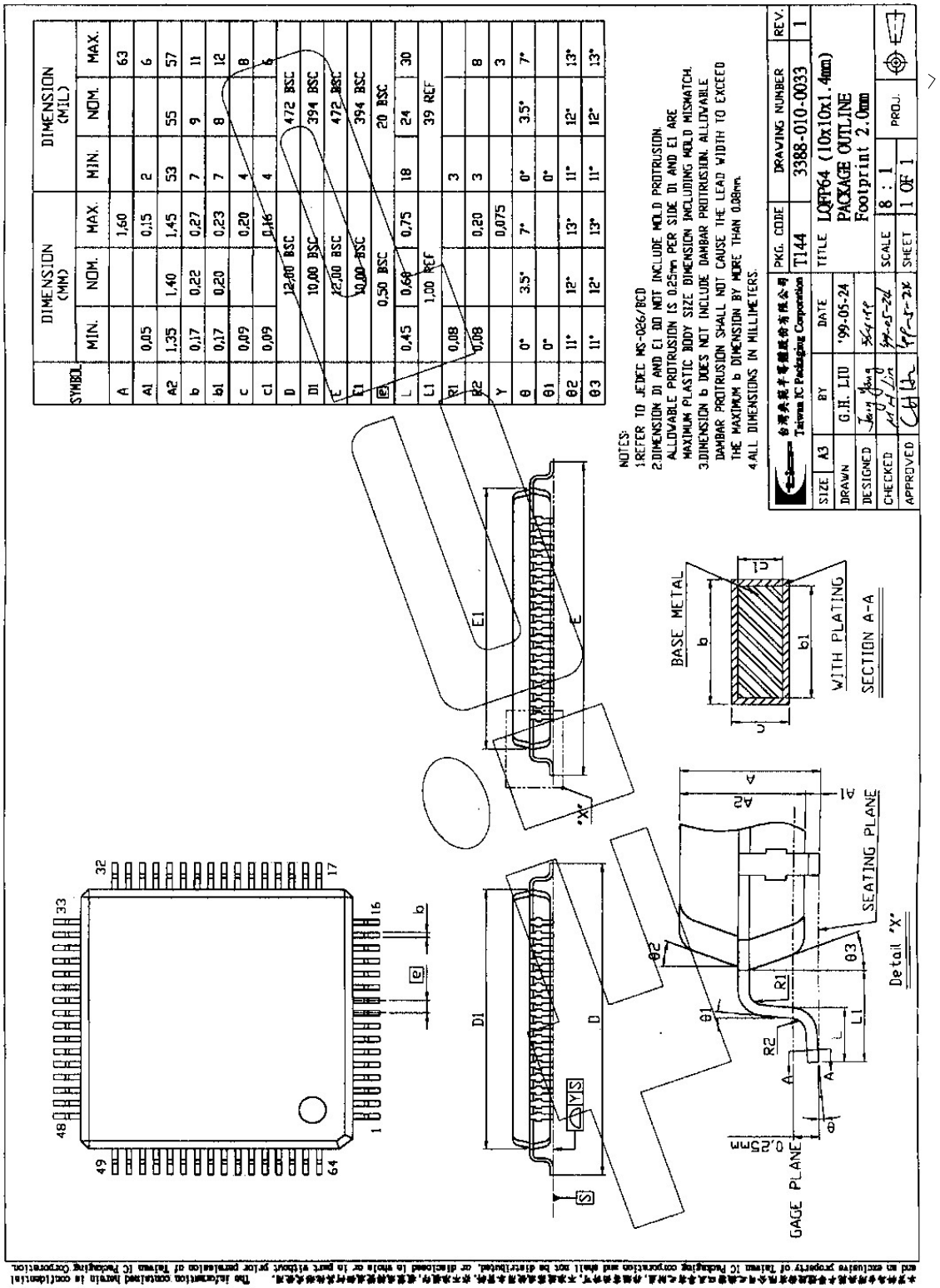

Figure 1-3 Outline Diagram of PL-2507 LQFP64