PL-2315 Portable USB Flash Disk
Product Datasheet

Document Revision: 2.0.0
Document Release: July, 2002

Prolific Technology Inc.

Revision History

Revision	Description	Date
2.0	For Chip Version B (date code 02281B) – Initial Release Note: for PL-2315 Rev A – refer to document rev. 1.0.	July 2002

Features

- Full compliance with Universal Serial Bus Specification v1.1
- On chip USB transceiver and Serial Interface Engine (SIE)
- On chip 5V-3.3V 100mA regulator for USB interface and internal circuit
- High performance write over 870Kbyte/s and read over 1030Kbyte/s
- Support up to eight state-of-the-art NAND flash memories
- Embedded USB hub function
- Write protection switch is provided
- Security device included to secure the privacy of the data (optional)
- Support booting from USB Flash Disk
- User Configurable Disk Partition
- Mass Storage Class compatible – no drivers needed in MAC OS, Windows ME/2000/XP or above
- Also supports Windows 98 with drivers supplied
- Advanced power management mechanism.
- Package type: LQFP48pin (4 NAND Flash memories)
  LQFP64pin (8 NAND Flash memories)

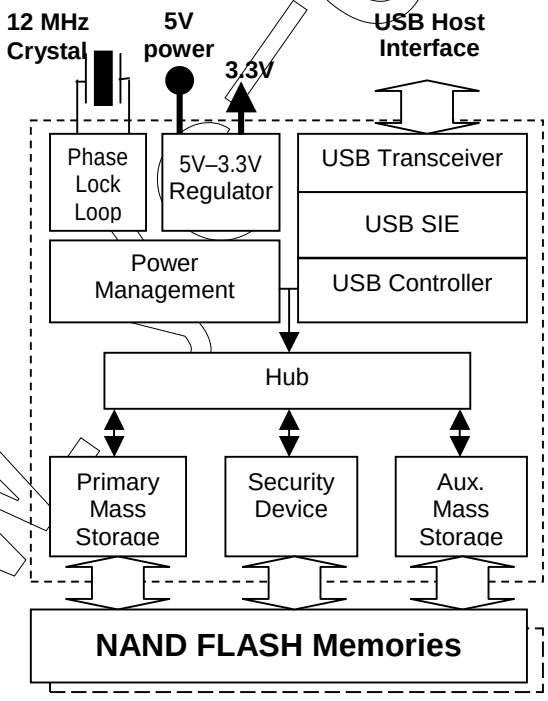

Figure 1-1 Block Diagram of PL-2315

1.0 Overview

The PL-2315 (Rev B) integrated circuit is a full-speed Portable USB Flash Disk Controller. This single chip consists of a hub, one or two mass-storage-class devices, and an optional “security device”. The PL-2315 allows interface of up to eight state-of-the-art NAND flash memories as its storage media. The required USB hub function is embedded to achieve the most cost-effective goal for multi-device solution.

The available NAND flash memories on board can generally be used as a normal single disk or partitioned into a standard mass storage device and a secured mass storage device. The sizes of the partitions can be easily configured and adjusted using the software utility program. Customers can pre-load the software driver and the application program of the “security device” or any other handy utilities into the standard storage disk to save an extra CD-ROM or floppy in order to reduce the cost and enhance users convenience.

To take advantage of Plug and Play, the mass storage device is implemented according to the USB mass storage device class. Since the default driver is embedded within most of the current OS, no extra driver is needed for Windows ME, 2000, XP and above.

The PL-2315 also provides options to customize the chip to show users’ identity. Users could modify the Vendor ID, Product ID, Language ID, manufacturer string, product string, and serial number strings of the final product.

1.1 Chip Configuration

The PL-2315 supports one Embedded hub, one or two USB mass-storage-class devices, and one optional “Security device.” Users can configure the chip by changing the setting of S_SQ_INJ pin, and by using the application program of the Security device. With the program, users can adjust the size (in MB unit) of the Standard and the Secured Disks. Users can also set and check the password of the Secured Disk. Another function of the program is to let the PL-2315 change the subclass code to support different command blocks defined by the USB mass storage class specification. Table 1.1 shows all possible chip configurations setting by S_SQ_INJ pin and the program.

Table 1.1 Chip Configurations

Security Switch [OFF] or Security Device Disabled:					
S_SQ_INJ setting	**Standard Disk**	**Secured Disk**	**Password**	**USB Devices Detected by the OS**	**Hub port number**
3.3V	√	No Partition	Don’t Care	Hub + Accessory Disk	1
3.3V	No Partition	√	None	Hub + Main Disk (Secured)	1
3.3V	No Partition	√	Yes	Hub	1
3.3V	√	√	None	Hub + Accessory Disk + Main Disk (Secured)	2
3.3V	√	√	Yes	Hub + Accessory Disk	2
Security Switch [ON] or Security Device Enabled:					
S_SQ_INJ setting	**Standard Disk**	**Secured Disk**	**Password**	**USB Devices Detected by the OS**	**Hub port number**
0V	√	No Partition	Don’t Care	Hub + Security device + Accessory Disk	2
0V	No Partition	√	None	Hub + Security device + Main Disk (Secured)	2
0V	No Partition	√	Yes	Hub + Security device + Main Disk (Secured) (after password check ok)	2
0V	√	√	None	Hub + Security device + Accessory Disk + Main Disk (Secured)	3
0V	√	√	Yes	Hub + Security device + Accessory Disk + Main Disk (Secured) (after password check ok)	3

2.0 Pin Assignment and Description

2.1 Pin Assignment and Description of PL-2315 LQFP64

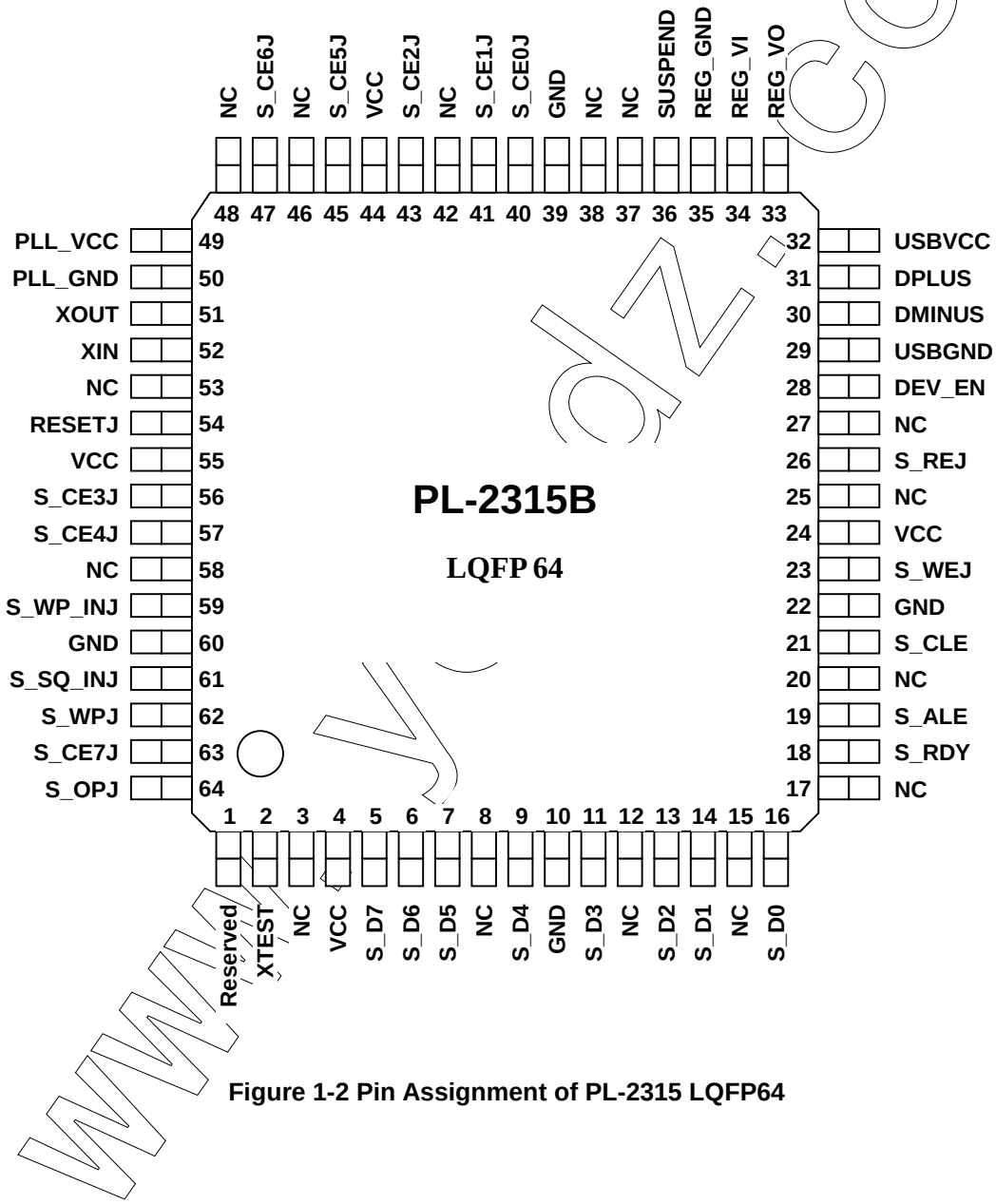

Figure 1-2 Pin Assignment of PL-2315 LQFP64

Table 2.1 Pin Descriptions of PL-2315 LQFP64

Pin	Symbol	Type	Description
1	Reserved	–	Reserved, must be tied to ground.
2	XTEST	I	Core test pin must be tied to ground for normal operation.
3	NC	–	No connection.
4	VCC	P	3.3V Power Supply.
5	S_D7	I/O	NAND flash memory data bus bit 7.
6	S_D6	I/O	NAND flash memory data bus bit 6.
7	S_D5	I/O	NAND flash memory data bus bit 5.
8	NC	–	No connection.
9	S_D4	I/O	NAND flash memory data bus bit 4.
10	GND	P	Ground.
11	S_D3	I/O	NAND flash memory data bus bit 3.
12	NC	–	No connection.
13	S_D2	I/O	NAND flash memory data bus bit 2.
14	S_D1	I/O	NAND flash memory data bus bit 1.
15	NC	–	No connection.
16	S_D0	I/O	NAND flash memory data bus bit 0.
17	NC	–	No connection.
18	S_RDY	I	NAND flash memory ready signal.
19	S_ALE	O	NAND flash memory address latch signal.
20	NC	–	No connection.
21	S_CLE	O	NAND flash memory command latch signal.
22	GND	P	Ground.
23	S_WEJ	O	NAND flash memory write enable signal, active low.
24	VCC	P	3.3V Power Supply.
25	NC	–	No connection.
26	S_REJ	O	NAND flash memory read enable signal, active low.
27	NC	–	No connection.
28	DEV_EN	O	USB Attach Enable.
29	USBGND	P	Ground for on-chip USB transceiver.
30	DMINUS	I/O	USB D- signal.
31	DPLUS	I/O	USB D+ signal.
32	USBVCC	P	3.3V Power Supply for on-chip USB transceiver.
33	REG_VO	P	3.3V output from on-chip 5V-to-3.3V regulator.
34	REG_VI	P	5V Power Supply for on-chip 5V-to-3.3V regulator.
35	REG_GND	P	Ground for on-chip 5V-to-3.3V regulator.
36	XSUSPEND	O	Suspend indication
37	NC	–	No connection.
38	NC	–	No connection.
39	GND	P	Ground.
40	S_CE0J	O	NAND flash memory 0 chip enable signal, active low.
41	S_CE1J	O	NAND flash memory 1 chip enable signal, active low.
42	NC	–	No connection.

Table 2.1 Pin Descriptions of PL-2315 LQFP64 (cont…)

Pin	Symbol	Type	Description
43	S_CE2J	O	NAND flash memory 2 chip enable signal, active low.
44	VCC	P	3.3V Power Supply.
45	S_CE5J	O	NAND flash memory 5 chip enable signal, active low.
46	NC	–	No connection.
47	S_CE6J	O	NAND flash memory 6 chip enable signal, active low.
48	NC	–	No connection.
49	PLLVCC	P	3.3V Analog Power Supply for on-chip PLL.
50	PLLGND	P	Analog Ground for on-chip PLL.
51	XOUT	O	Crystal out or no connection.
52	XIN	I	Crystal in or CMOS oscillator input.
53	NC	–	No connection.
54	RESETJ	I	Optional external Power-On-Reset signal, active low.
55	VCC	P	3.3V Power Supply.
56	S_CE3J	O	NAND flash memory 3 chip enable signal, active low.
57	S_CE4J	O	NAND flash memory 4 chip enable signal, active low.
58	NC	–	No connection.
59	S_WP_INJ	I	Write protect input, active low.
60	GND	P	Ground.
61	S_SQ_INJ	I	Security enable input, active low.
62	S_WPJ	I	NAND flash memory write protect signal, active low.
63	S_CE7J	O	NAND flash memory 7 chip enable signal, active low.
64	S_OPJ	O	Operation indication signal, active low.

2.2 Pin Assignment and Description of PL-2315 LQFP48

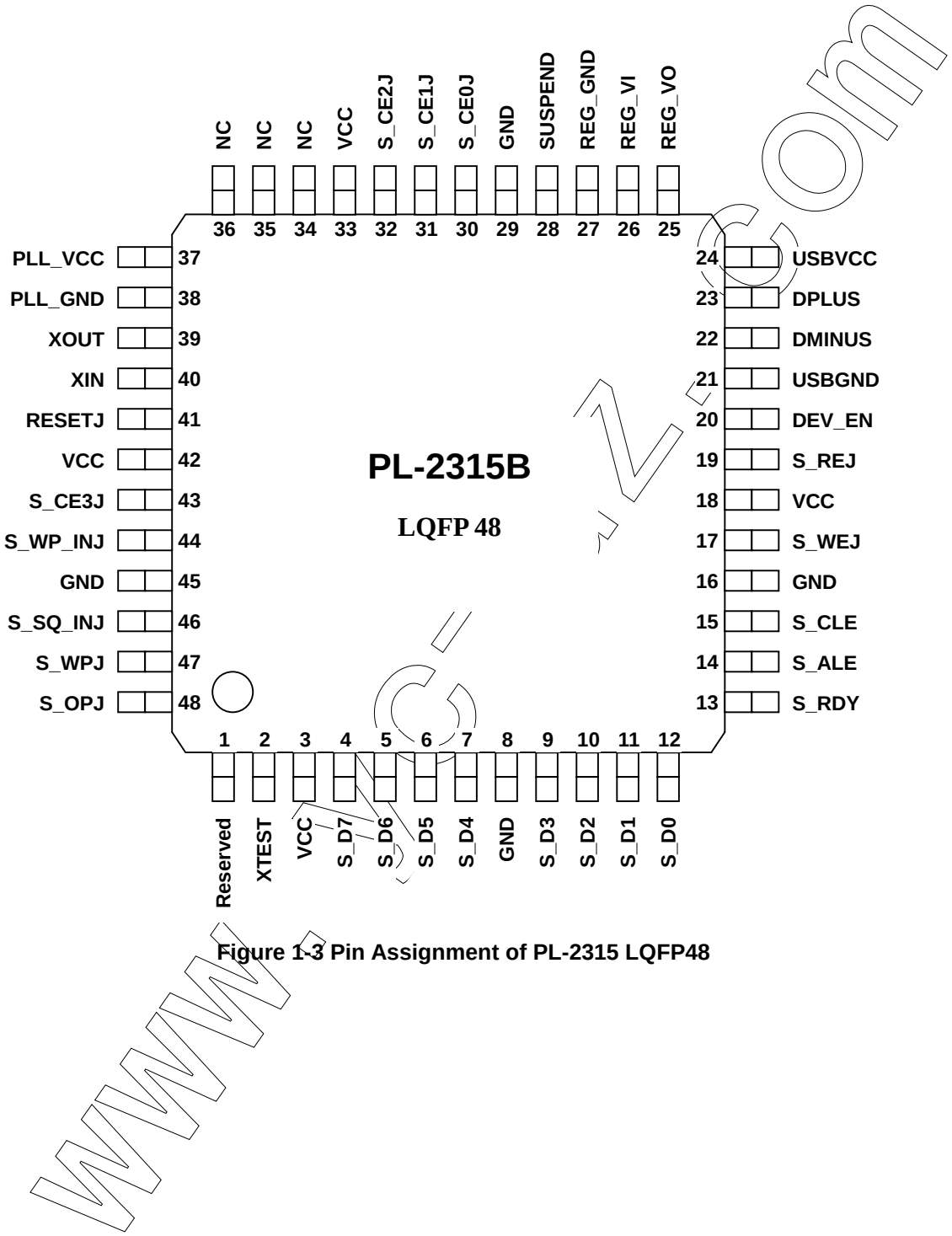

Figure 1-3 Pin Assignment of PL-2315 LQFP48

Table 2.2 Pin Descriptions of PL-2315 LQFP48

Pin	Symbol	Type	Description
1	Reserved	–	Reserved, must be tied to ground.
2	XTEST	I	Core test pin must be tied to ground for normal operation.
3	VCC	P	3.3V Power Supply.
4	S_D7	I/O	NAND flash memory data bus bit 7.
5	S_D6	I/O	NAND flash memory data bus bit 6.
6	S_D5	I/O	NAND flash memory data bus bit 5.
7	S_D4	I/O	NAND flash memory data bus bit 4.
8	GND	P	Ground.
9	S_D3	I/O	NAND flash memory data bus bit 3.
10	S_D2	I/O	NAND flash memory data bus bit 2.
11	S_D1	I/O	NAND flash memory data bus bit 1.
12	S_D0	I/O	NAND flash memory data bus bit 0.
13	S_RDY	I	NAND flash memory ready signal.
14	S_ALE	O	NAND flash memory address latch signal.
15	S_CLE	O	NAND flash memory command latch signal.
16	GND	P	Ground.
17	S_WEJ	O	NAND flash memory write enable signal, active low.
18	VCC	P	3.3V Power Supply.
19	S_REJ	O	NAND flash memory read enable signal, active low.
20	DEV_EN	O	USB Attach Enable.
21	USBGND	P	Ground for on-chip USB transceiver.
22	DMINUS	I/O	USB D- signal.
23	DPLUS	I/O	USB D+ signal.
24	USBVCC	P	3.3V Power Supply for on-chip USB transceiver.
25	REG_VO	P	3.3V output from on-chip 5V-to-3.3V regulator.
26	REG_VI	P	5V Power Supply for on-chip 5V-to-3.3V regulator.
27	REG_GND	P	Ground for on-chip 5V-to-3.3V regulator.
28	XSUSPEND	O	Suspend indication
29	GND	P	Ground.
30	S_CE0J	O	NAND flash memory 0 chip enable signal, active low.
31	S_CE1J	O	NAND flash memory 1 chip enable signal, active low.
32	S_CE2J	O	NAND flash memory 2 chip enable signal, active low.
33	VCC	P	3.3V Power Supply.
34	NC	–	No connection.
35	NC	–	No connection.
36	NC	–	No connection.
37	PLLVCC	P	3.3V Analog Power Supply for on-chip PLL.
38	PLLGND	P	Analog Ground for on-chip PLL.
39	XOUT	O	Crystal out or no connection.
40	XIN	I	Crystal in or CMOS oscillator input.

Table 2.2 Pin Descriptions of PL-2315 LQFP48 (cont…)

Pin	Symbol	Type	Description
41	RESETJ	I	Optional external Power-On-Reset signal, active low.
42	VCC	P	3.3V Power Supply.
43	S_CE3J	O	NAND flash memory 3 chip enable signal, active low.
44	S_WP_INJ	I	Write protect input, active low.
45	GND	P	Ground.
46	S_SQ_INJ	I	Security Enable input, active low.
47	S_WPJ	I	NAND flash memory write protect signal, active low.
48	S_OPJ	O	Operation indication signal, active low.

3.0 DC Characteristics

3.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	RATING	UNITS
Vcc	Power Supply	-0.3 to 3.6	V
Vin	Input Voltage	-0.3 to Vcc+0.3	V
Vout	Output Voltage	-0.3 to Vcc+0.3	V
Tstg	Storage Temperature	-55 to 150 (TBD)	C

3.2 Recommended Operation Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
Vcc	Commercial Power Supply	3.0	3.3	3.6	V
Vin	Input Voltage	0	-	Vcc	V
Tj	Commercial Junction Operation Temperature	0	25	115	C

3.3 General DC Characteristics:

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Iil	Input leakage current	No pull-up or pull-down	-1		1	uA
Ioz	Tri-state leakage current		-1		1	uA
Cin	Input capacitance			2.8		pF
Cout	Output capacitance		2.7		4.9	pF
Cbid3	Bi-directional buffer capacitance		2.7		4.9	pF

Note: The capacitance listed above does not include PAD capacitance and package capacitance.

3.4 DC Electrical Characteristics for 3.3 V Operation

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Vil	Input low voltage	CMOS			0.3*Vcc	V
Vih	Input high voltage	CMOS	0.7*Vcc			V
Vt-	Schmitt trigger negative going threshold voltage	CMOS		1.20		V
Vt+	Schmitt trigger positive going threshold voltage	CMOS		2.10		V
Vol	Output low voltage	I_{OL}= 2, 4, 8, 12, 16, 24 mA			0.4	V
Voh	Output high voltage	I_{OL}= 2, 4, 8, 12, 16, 24 mA	2.4			V
Ri	Input pull-up/pull-down resistance	V_{IL}= 0v or V_{IH}= Vcc		75		KΩ

4.0 Outline Diagram

4.1 LQFP48pin Outline Diagram:

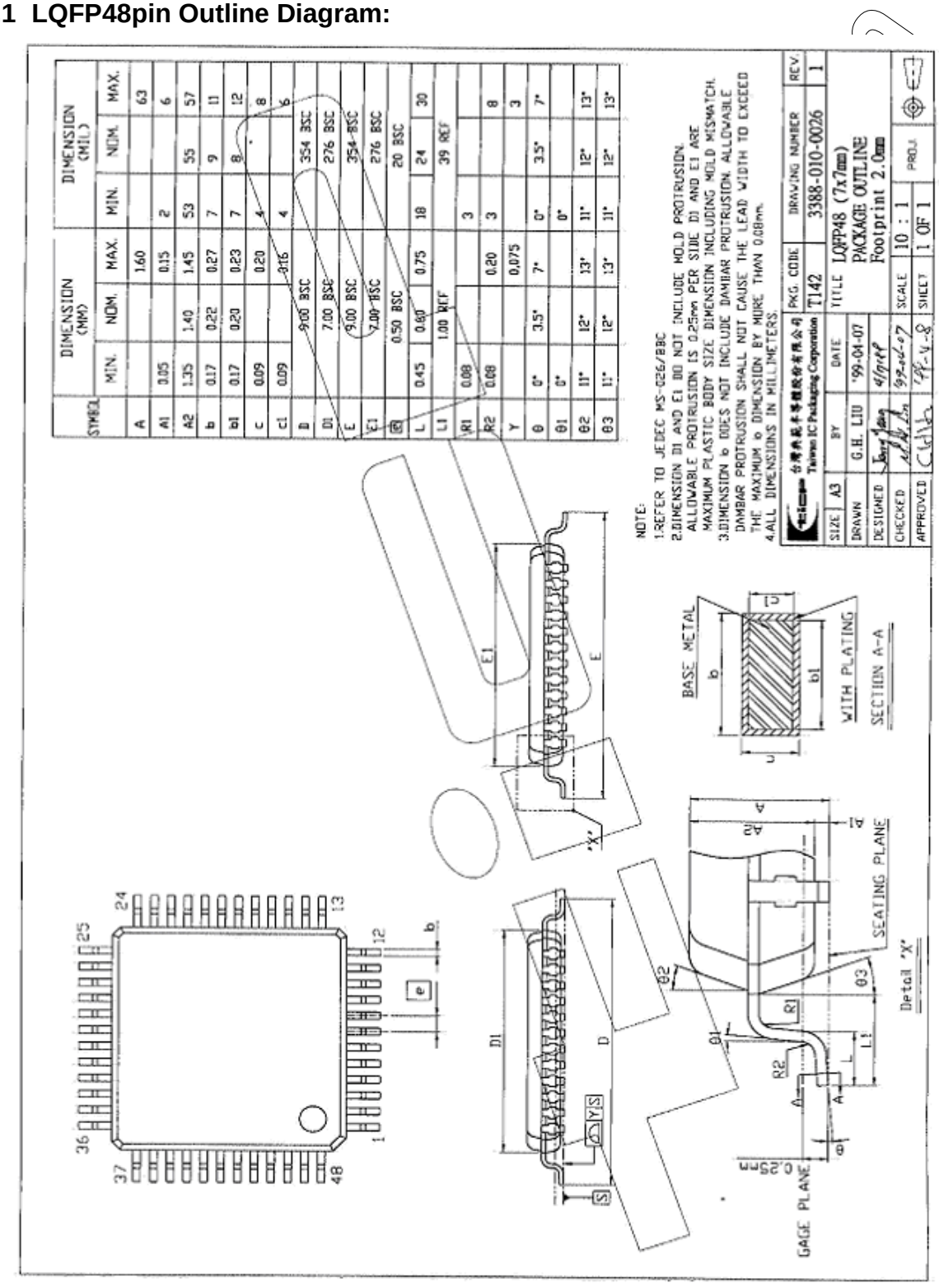

Figure 1-4 Outline Diagram of PL-2315 LQFP48

4.2 LQFP64pin Outline Diagram:

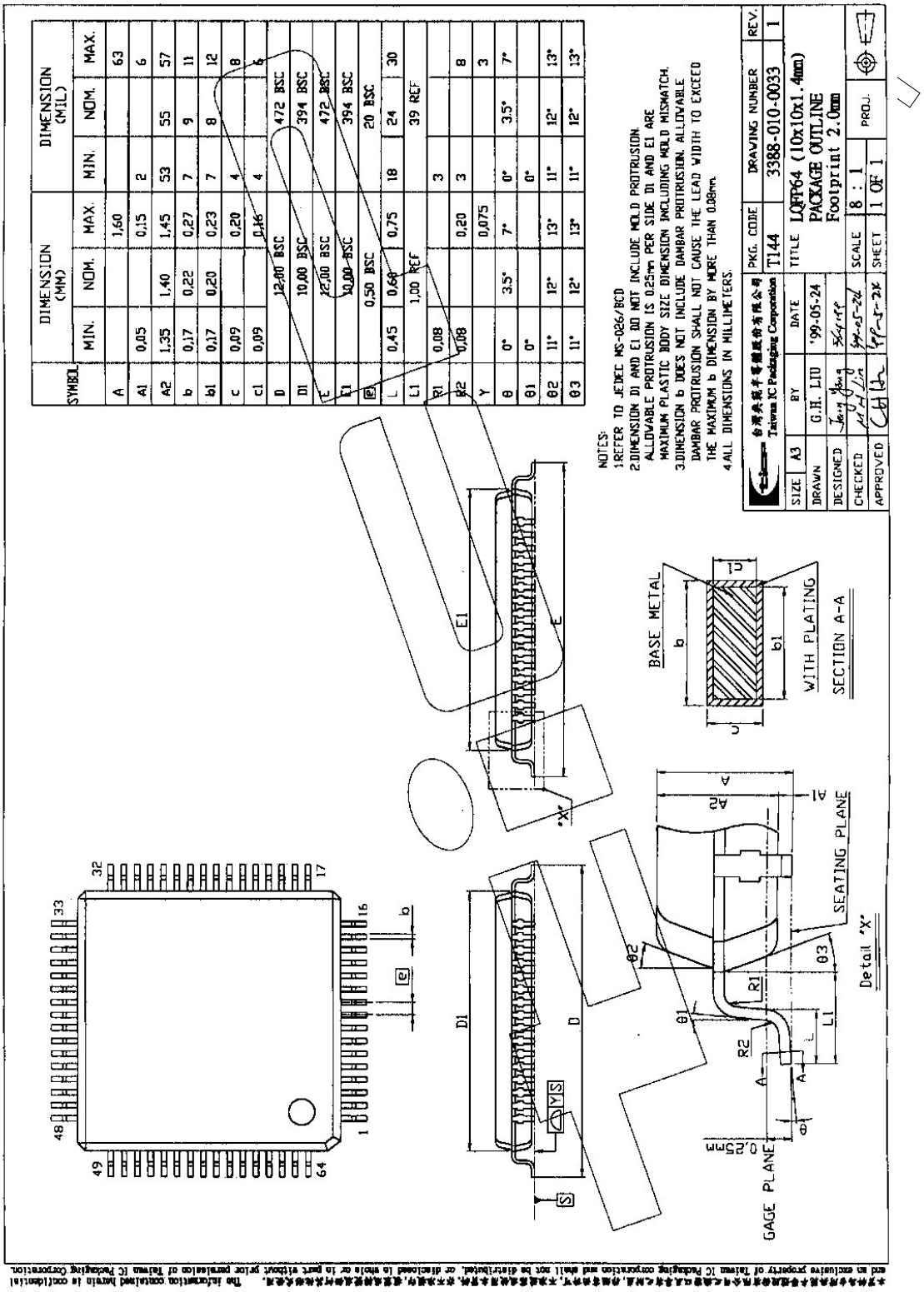

Figure 1-5 Outline Diagram of PL-2315 LQFP64