AU9331
USB Secure Digital Card Reader
Technical Reference Manual

Revision 1.2

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1.0 Introduction

1.1 Description

The AU9331 is an integrated USB Secure Digital (SD) card reader controller. It supports Secure Digital (SD) and Multimedia Card (MMC) with automatic card type detection capability. It can be used as a removable storage disk in enormous data exchange applications between PC and PC or PC and various consumer electronic devices.

The AU9331 can read Secure Digital card's contents created by handheld consumer electronic devices such as digital camera, MP3 player, PDA and mobile phone.., etc. It provides a faster and convenient way of data transfer scheme to meet the emerging need of a data exchange center between PC and various consumer devices. With AU9331, users' experience will be further enhanced by the Plug-and-Play nature built into latest operation systems such as Windows XP and MacOS X.

Because of the multiple sectors transfer up to 4G bytes and the single chip integration, AU9331 is the most powerful and cost efficient SD reader controller solution in the market.

1.2 Features

- Fully compliant with USB v1.1 specification and USB Device Class Definition for Mass Storage, Bulk-Transport v1.0
- Fully compliant with Secure Digital (SD) v1.0 Specification.
- Work with default driver from Windows ME, Windows 2000, Windows XP, Mac OS 9.1, Mac OS X; Linux, Windows 98 and WinCE 3.0 are supported by vendor driver from Alcor.
- Ping-pong FIFO implementation for concurrent bus operation to increase bandwidth
- Support multiple sectors transfer up to 4G bytes to optimize performance
- Support optional external EEPROM for USB VID, PID and string customization
- LED for bus activity monitoring
- Runs at 12MHz
- Built-in 3.3V regulator
- 28-pin SSOP package

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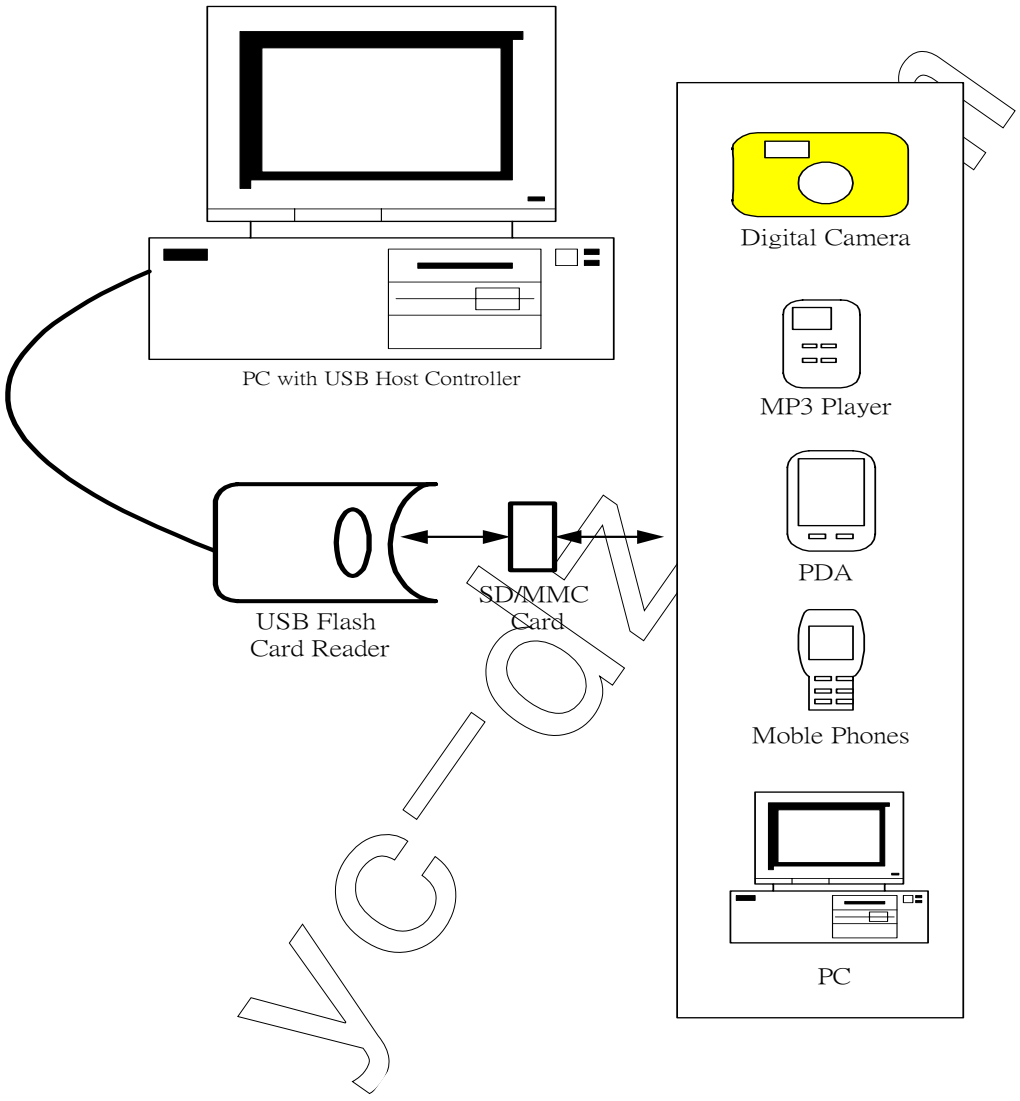
2.0 Application Block Diagram

Following is the application diagram of a typical flash memory card reader using AU9330. By connecting the reader to a PC through USB port, the AU9331 is acting as a bridge between the flash memory card from digital camera, MP3 player, PDA or mobile phone and PC.



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3.0 Pin Assignment

The AU9331 is packed in 28-SSOP form factor. The following figure shows signal name for each pin and the table in the following page describes each pin in detail.

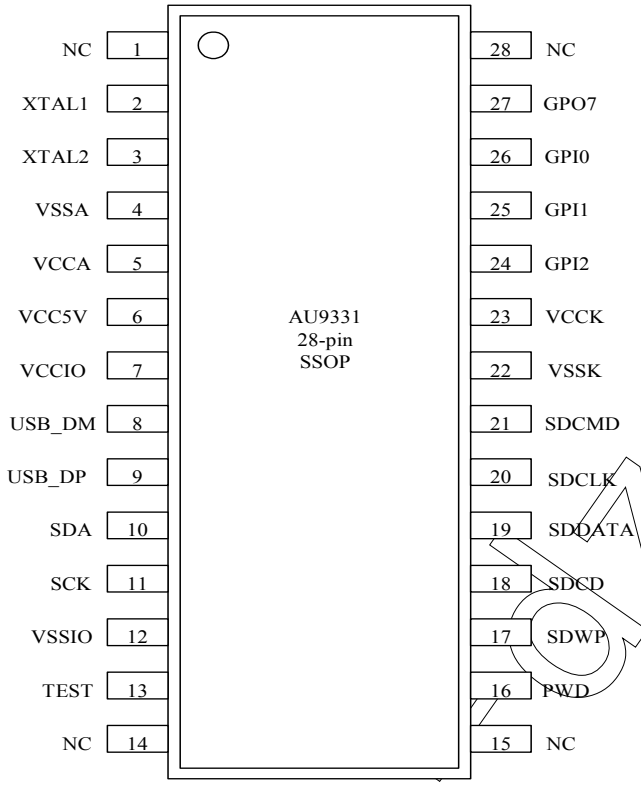
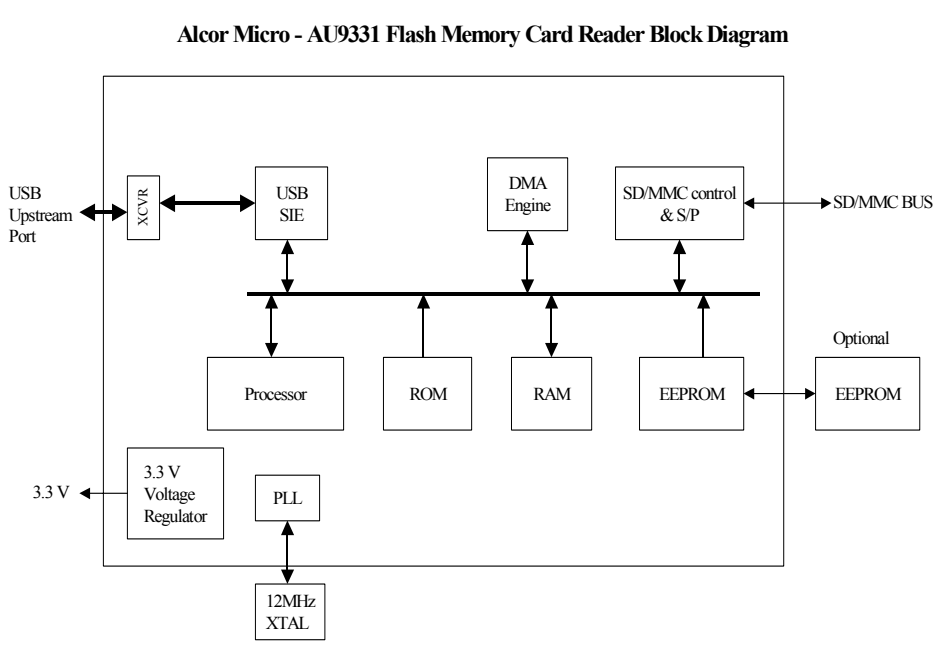


Table 3-1. Pin Descriptions

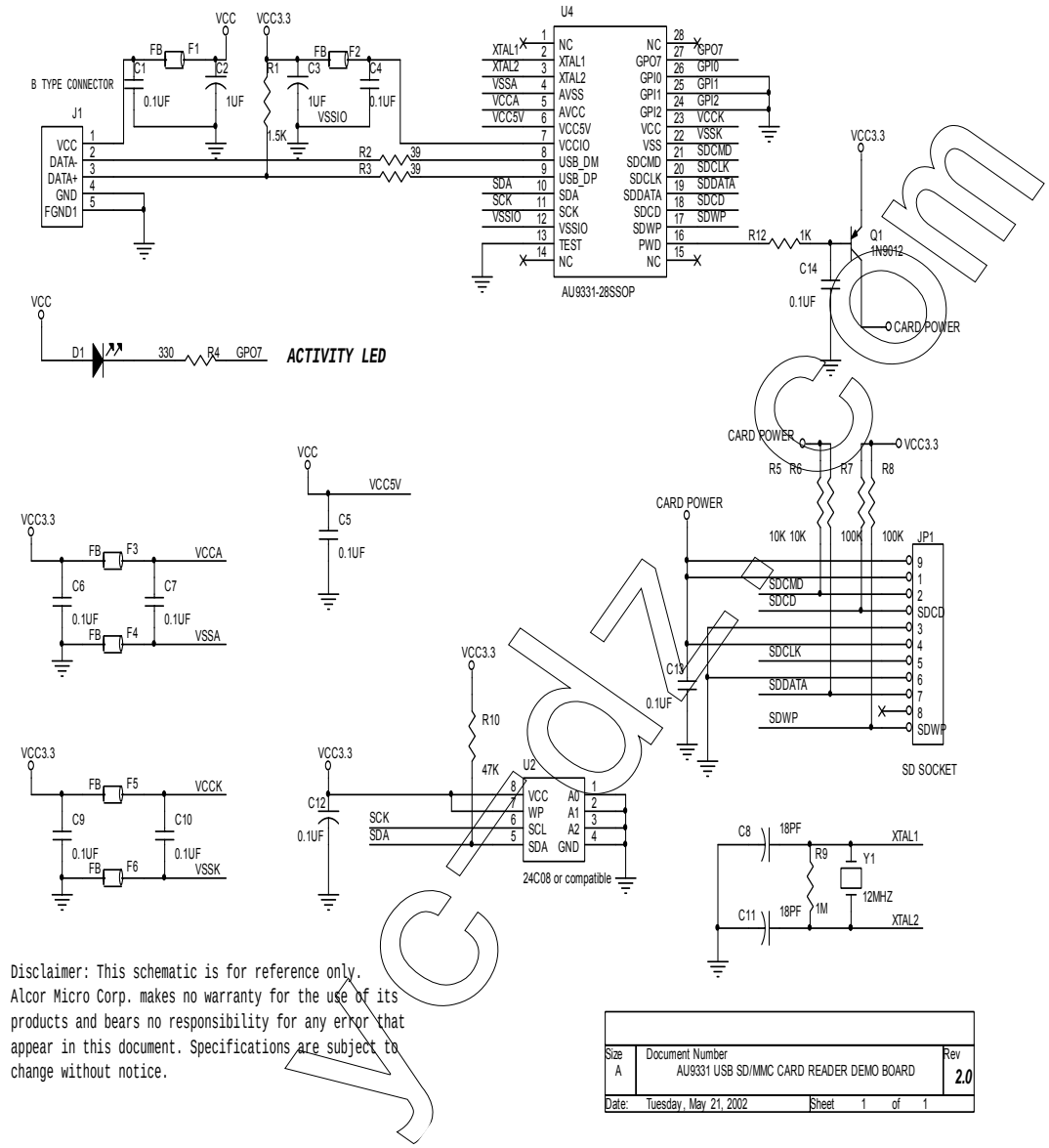
pin	Name	IO Type	Description
1	NC		
2	XTAL1	I	Crystal Oscillator Input (12MHz)
3	XTAL2	O	Crystal Oscillator Output (12MHz)
4	VSSA	Ground	Analog Ground
5	VCCA	PWR	Analog power supply
6	VCC5V	PWR	5V power supply
7	VCCIO	PWR	Regular 3.3V output/ IO 3.3V input
8	USB_DM	I/O	USB D-
9	USB_DP	I/O	USB D+
10	SDA	I/O	EEPROM data inout
11	SCK	O	EEPROM clcok
12	VSSIO	PWR	Ground
13	Test	I	Should connect to Vss
14	NC		
15	NC		
16	PWD	O	0 Power on; 1 Power down
17	SDWP	I	SD Write Protect
18	SDCD	I	SD Card Detect
19	SDDATA	I/O	SD Card Data
20	SDCLK	O	SD Card Clock
21	SDCMD	I/O	SD Card Command
22	VSSK	PWR	Ground
23	VCCK	PWR	Core 3.3V Input
24	GPI2	I	Should connect to Vss
25	GPI1	I	Should connect to Vss
26	GPI0	I	Should connect to Vss
27	GPO7	O	General Purpose Output pin, used as activity LED
28	NC		

4.0 System Architecture and Reference Design

4.1 AU9331 Block Diagram



4.2 Sample Schematics



Disclaimer: This schematic is for reference only. Alcor Micro Corp. makes no warranty for the use of its products and bears no responsibility for any error that appear in this document. Specifications are subject to change without notice.

Size	Document Number	Rev
A	AU9331 USB SD/MMC CARD READER DEMO BOARD	2.0
Date: Tuesday, May 21, 2002	Sheet 1 of 1	

5.0 Electrical Characteristics

5.1 Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
V_{CC}	Power Supply	4.75	5	5.25	V
V_{IN}	Input Voltage	0		V_{CC}	V
T_{OPR}	Operating Temperature	0		85	^{O}C
T_{STG}	Storage Temperature	-40		125	^{O}C

5.2 General DC Characteristics

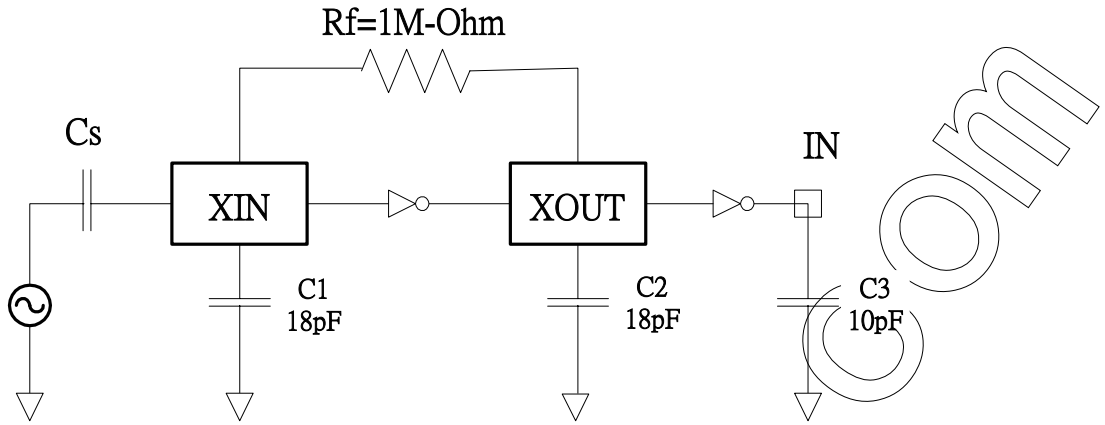
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{IL}	Input low current	no pull-up or pull-down	-1		1	µA
I_{IH}	Input high current	no pull-up or pull-down	-1		1	µA
I_{OZ}	Tri-state leakage current		-10		10	µA
C_{IN}	Input capacitance			5		ρF
C_{OUT}	Output capacitance			5		ρF
C_{BID}	Bi-directional buffer capacitance			5		ρF

5.3 DC Electrical Characteristics for 3.3 volts operation

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IL}	Input Low Voltage	CMOS			0.9	V
V_{IH}	Input Hight Voltage	CMOS	2.3			V
V_{OL}	Output low voltage	I_{OL}=4mA, 16mA			0.4	V
V_{OH}	Output high voltage	I_{OH}=4mA,16mA	2.4			V
R_I	Input Pull-up/down resistance	Vil=0_V or Vih=V_{CC}		10k/200k		KΩ

5.4 Crystal Oscillator Circuit Setup for Characterization

The following setup was used to measure the open loop voltage gain for crystal oscillator circuits. The feedback resistor serves to bias the circuit at its quiescent operating point and the AC coupling capacitor, Cs, is much larger than C1 and C2.



5.5 ESD Test Results

Test Description : ESD Testing was performed on a Zapmaster system using the Human-Body –Model (HBM) and Machine-Model (MM), according to MIL_STD 883 and EIAJ IC_121 respectively.

- Human-Body-Model stress devices by sudden application of a high voltage supplied by a 100 PF capacitor through 1.5 Kohm resistance.
- Machine-Model stresses devices by sudden application of a high voltage supplied by a 200 PF capacitor through very low (0 ohm) resistance

Test circuit & condition

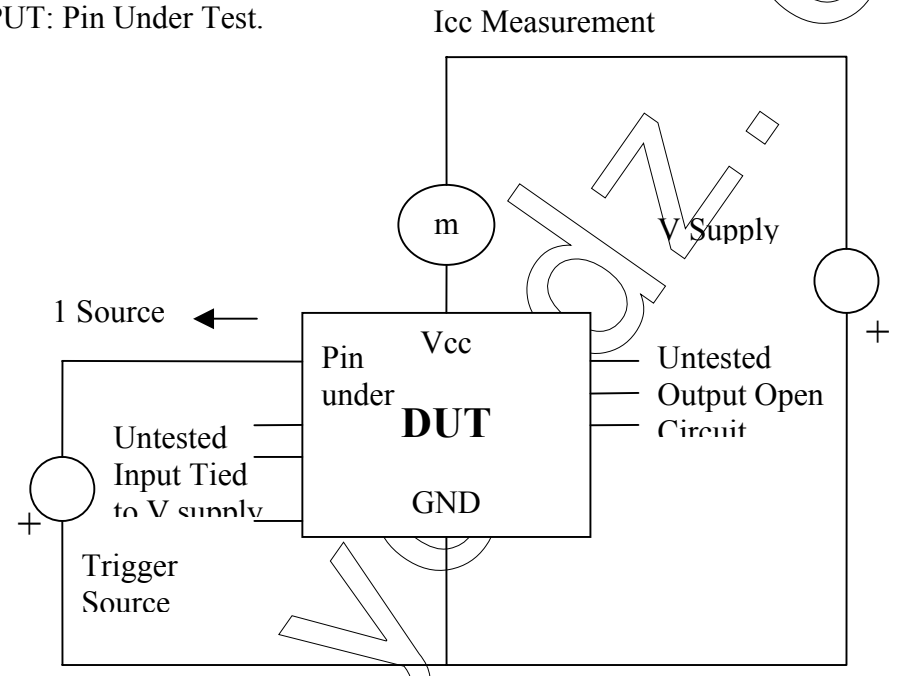
- Zap Interval : 1 second
- Number of Zaps : 3 positive and 3 negative at room temperature
- Critera : I-V Curve Tracing

Model	Model	S/S	TARGET	Results
HBM	Vdd, Vss, I/C	15	4000V	Pass
MM	Vdd, Vss, I/C	15	200V	Pass

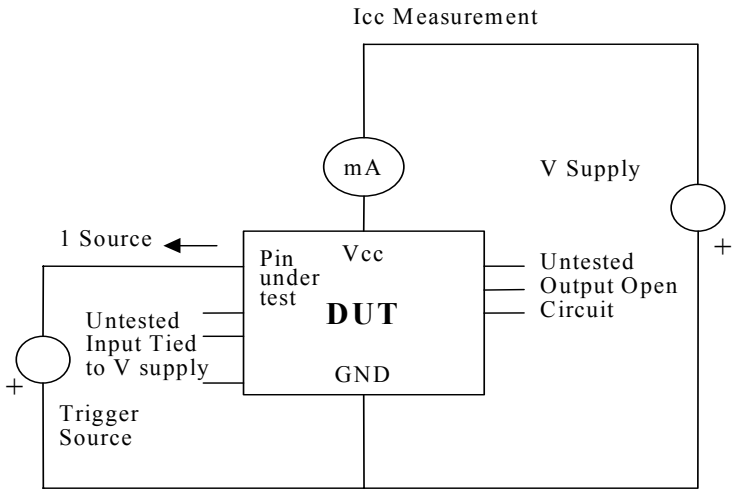
5.6 Latch-Up Test Results

Test Description: Latch-Up testing was performed at room ambient using an IMCS-4600 system which applies a stepped voltage to one pin per device with all other pins open except Vdd and Vss which were biased to 5 Volts and ground respectively.
Testing was started at 5.0 V (Positive) or 0 V(Negative), and the DUT was biased for 0.5 seconds.
If neither the PUT current supply nor the device current supply reached the predefined limit (DUT=0 mA , Icc=100 mA), then the voltage was increased by 0.1 Volts and the pin was tested again.
This procedure was recommended by the JEDEC JC-40.2 CMOS Logic standardization committee.

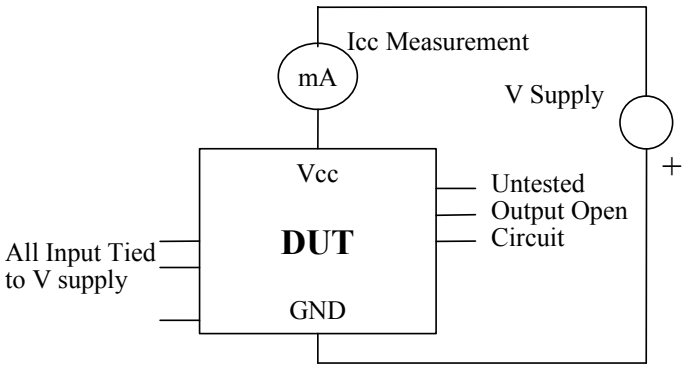
Notes:
1. DUT: Device Under Test.
2. PUT: Pin Under Test.



Test Circuit : Positive Input/ output Overvoltage /Overcurrent



Test Circuit : Negative Input/ Output Overvoltage /Overcurrent



Supply Voltage test

Latch–Up Data

Model	Model	Voltage (v)/ Current (mA)	S/S	Results
Voltage	+	11.0	5	Pass
	-	11.0		
Current	+	200	5	
	-	200		
Vdd-Vxx		9.0	5	Pass

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6.0 Mechanical Information