AU9350
USB SmartMediaCard Reader Controller Chip TRM

Revision 1.0

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1.0 Introduction

1.1 Description

The AU9350 is a single chip integrated USB SmartMediaCard (SMC) reader controller. It can be used as a removable storage disk in enormous data exchange applications between PC and PC or PC and various consumer electronic appliances.

The AU9350 reads digital data saved on SmartMediaCard while users manipulating electronic devices such as digital cameras, MP3 players, PDAs and mobile phones… etc. By the AU9350, users can transfer information such as data, graphics, texts or digital images from one electronic device to another quickly and easily. With AU9350, users' experience will be further enhanced by the USB Plug-and-Play nature built into latest operation systems such as Windows 2000/XP and Mac OS X.

By integrating of various analog components, the AU9350 is the most powerful and most effective solution for smar mediacard reader.

1.2 Features

- Fully compliant with USB v1.1 specification and USB Device Class Definition for Mass Storage, Bulk-Transport v1.0
- Fully compliant with SmartMediaCard (SMC) Standard 2000 Specification.
- Work with default driver from Windows ME, Windows 2000, Windows XP, Mac OS 9.1, and Mac OS X. Windows 98 is supported by vendor driver from Alcor.
- Ping-pong FIFO implementation for concurrent bus operation
- Support multiple sectors transfer to 4GB to optimize performance
- Support Mask ROM Card capacity from 2MB to 64MB.
- Support Flash Card capacity from 4MB to 125 MB.
- Support optional external EEPROM for USB VID, PID and string customization
- Capable of handling 8 sets of built-in PID, VID and strings to minimize inventory control and improve lead production lead time
- LED for bus activity indication.
- Integrated power switch and power management circuit to meet USB 500uA power consumption during suspend with SMC card in the slot.
- Runs at 12MHz, built-in 48 MHz PLL
- Built-in 3.3V regulator
- 48-pin LQFP package

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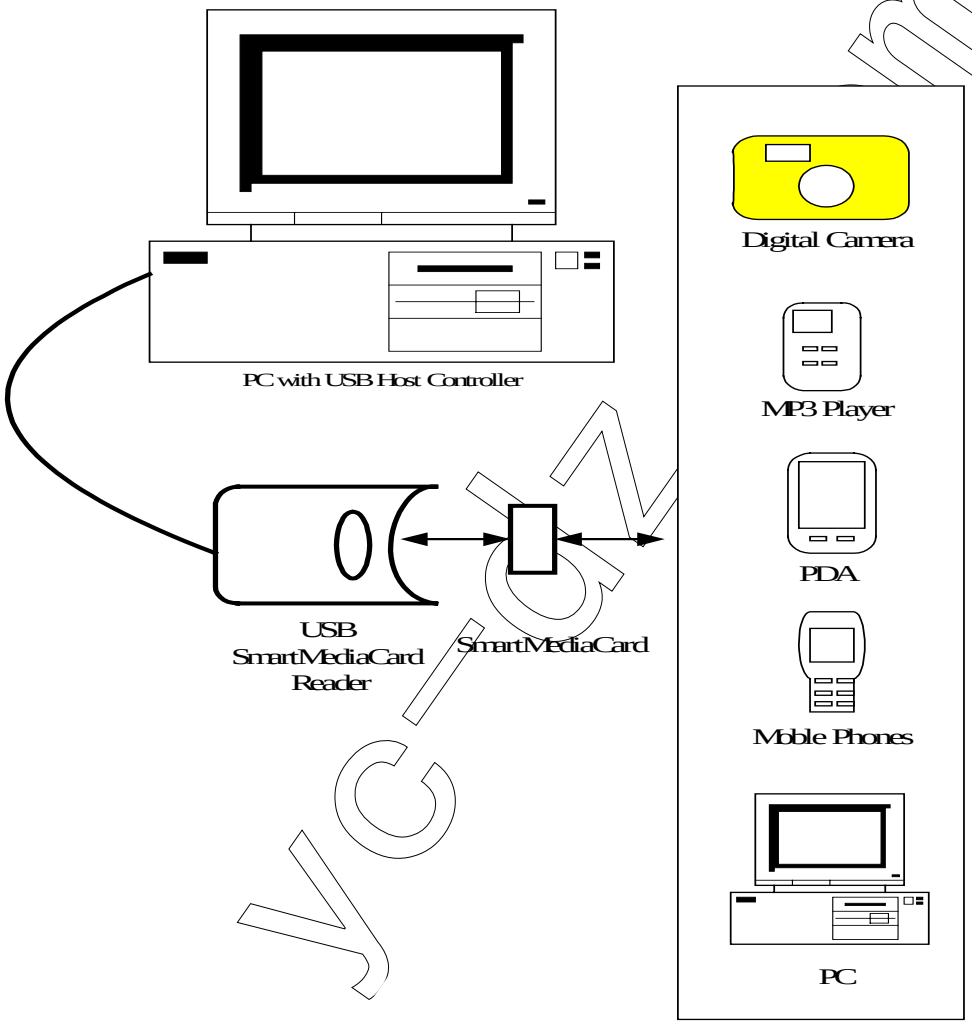
2.0 Application Block Diagram

Following is the application diagram of a typical flash memory card reader using AU9350. By connecting the reader to a PC through USB bus, the AU9350 is acting as a bridge between the flash memory card from digital camera, MP3 player, PDA or mobile phone and PC.



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3.0Pin Assignment

The AU9350 is packed in 48-LQFP form factor. The following figure shows signal name for each pin and the table in the following page describes each pin in detail.

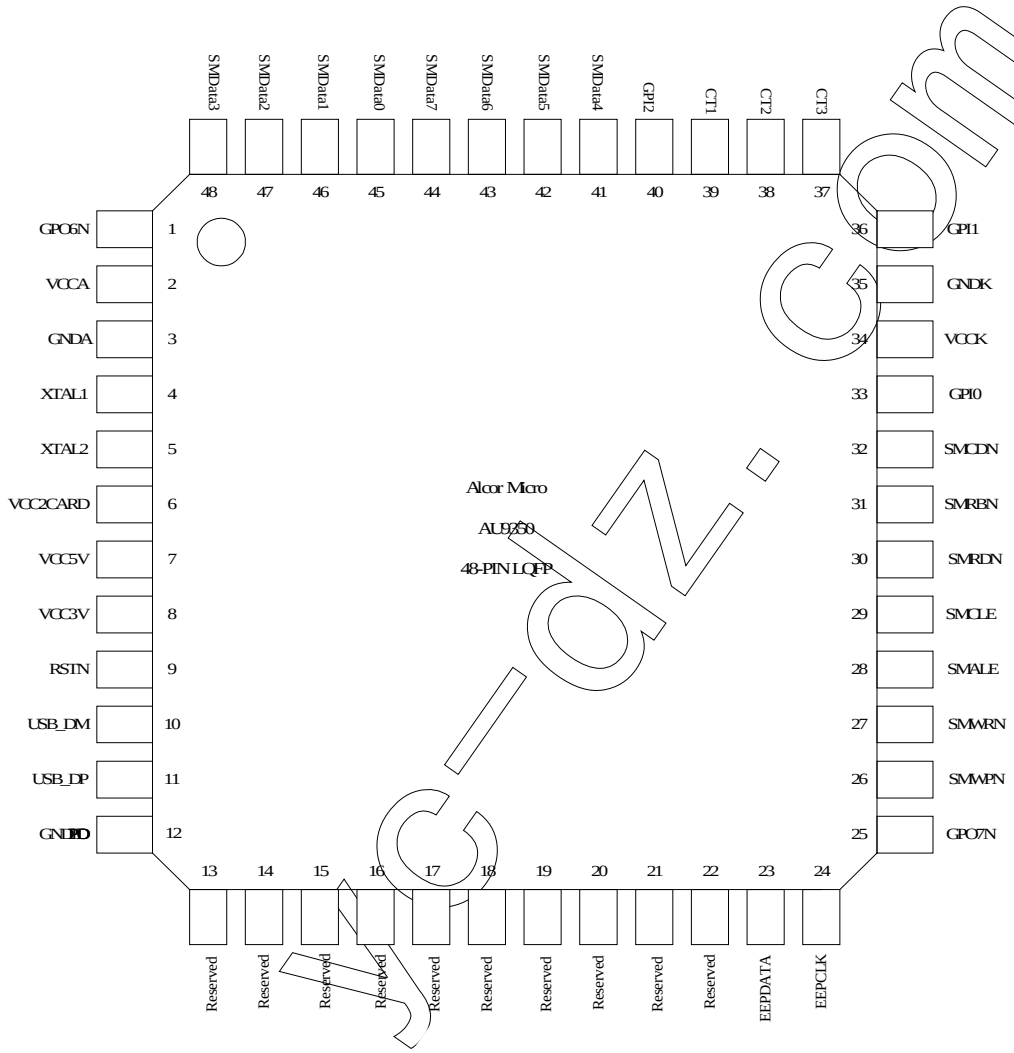


Table 3-1. Pin Descriptions

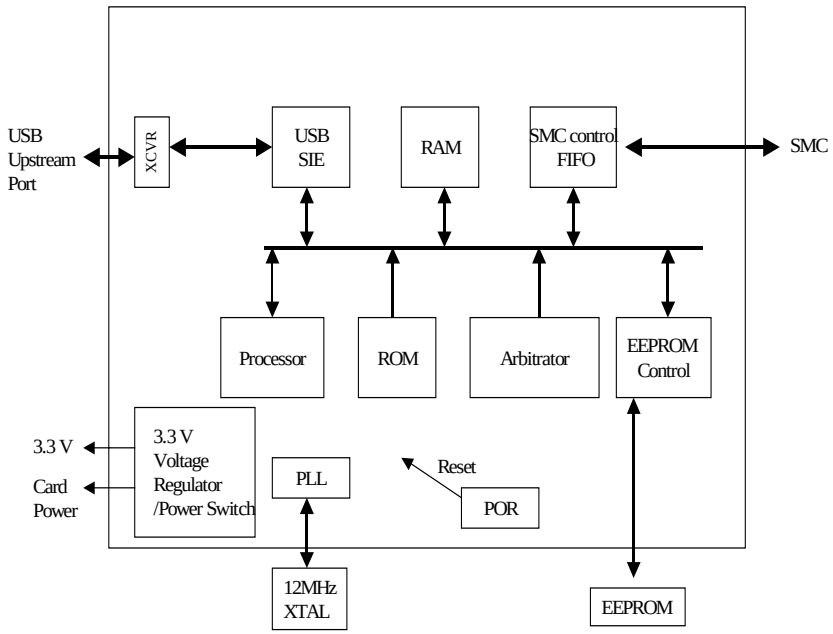
Pin	Name	I/O Type	Description
1	GPO6N	O	General Purpose Output pin, used as activity LED
2	VCCA	PWR	Analog 3.3V input
3	GNDA	PWR	Ground
4	XTAL1	I	Crystal Oscillator Input (12MHz)
5	XTAL2	O	Crystal Oscillator Output (12MHz)
6	VCC2CARD	O	Connect to SmartMedia Card Vcc
7	VCC5V	PWR	5V power supply
8	VCC3V	PWR	Regular 3.3V output/ IO 3.3V input
9	RSTN	I	Hardware reset (Active Low)
10	USB_DM	I/O	USB D-
11	USB_DP	I/O	USB D+
12	GNDIO	PWR	Ground
13	RFU		Reserved for future use
14	RFU		Reserved for future use
15	RFU		Reserved for future use
16	RFU		Reserved for future use
17	RFU		Reserved for future use
18	RFU		Reserved for future use
19	RFU		Reserved for future use
20	RFU		Reserved for future use
21	RFU		Reserved for future use
22	RFU		Reserved for future use
23	EEPDATA	I/O	Connect to I2C Serial Data

24	EEPCLK	O	Connect to I2C Serial Clock Input
25	GPO7N	O	General Purpose Output pin, used as activity LED
26	SMWPN	I	Connect to SmartMedia Card Write Protect
27	SMWRN	O	Connect to SmartMedia Card Write Enable
28	SMALE	O	Connect to SmartMedia Card Address Latch Enable
29	SMCLE	O	Connect to SmartMedia Card Command Latch Enable
30	SMRDN	O	Connect to SmartMedia Card Read Enable
31	SMRBN	I	Connect to SmartMedia Card Ready/Busy Output
32	SMCDN	I	Connect to SmartMedia Card Card Detect
33	GPI0	I	Selection VID/PID
34	VCCK	PWR	Core 3.3V Input
35	GNDK	PWR	Ground
36	GPI1	I	Selection VID/PID
37	CT3	I	ECC Selection ('0'=Disable, '1'=Enable)
38	CT2	I	ROM Selection ('0' = ASIC ROM, '1'=External ROM)
39	CT1	I	PLL Selection ('0'= ASIC PLL, '1'= External PLL)
40	GPI2	I	Selection VID/PID
41	SMDATA4	I/O	Connect to SmartMedia Card Data IO4
42	SMDATA5	I/O	Connect to SmartMedia Card Data IO5
43	SMDATA6	I/O	Connect to SmartMedia Card Data IO6
44	SMDATA7	I/O	Connect to SmartMedia Card Data IO7
45	SMDATA0	I/O	Connect to SmartMedia Card Data IO0
46	SMDATA1	I/O	Connect to SmartMedia Card Data IO1
47	SMDATA2	I/O	Connect to SmartMedia Card Data IO2
48	SMDATA3	I/O	Connect to SmartMedia Card Data IO3

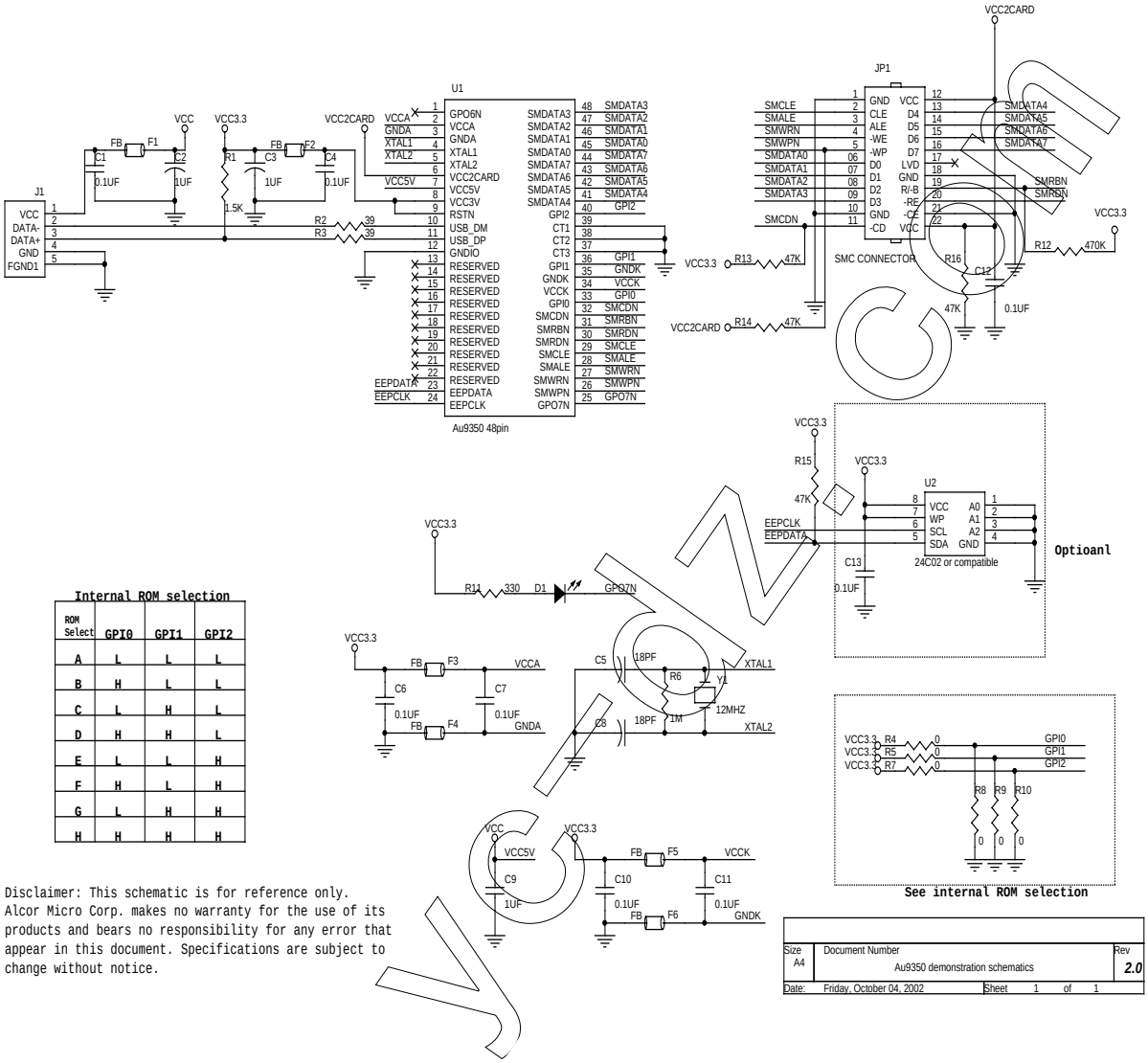
4.0 System Architecture and Reference Design

4.1 AU9350 Block Diagram

Alcor Micro - AU9350 Flash Memory Card Reader Controller Chip Block Diagram



4.2 Sample Schematics



Internal ROM selection

ROM Select	GPI0	GPI1	GPI2
A	L	L	L
B	H	L	L
C	L	H	L
D	H	H	L
E	L	L	H
F	H	L	H
G	L	H	H
H	H	H	H

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Size	Document Number	Rev
A4	Au9350 demonstration schematics	2.0
Date:	Friday, October 04, 2002	Sheet 1 of 1

5.0 Electrical Characteristics

5.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Power Supply	-0.3 to 6.0	V
V_{IN}	Input Voltage	-0.3 to VCC+0.3	V
V_{OUT}	Output Voltage	-0.3 to VCC+0.3	V
T_{STG}	Storage Temperature	-40 to 125	C

5.2 Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
V_{CC}	Power Supply	4.5	5.0	5.5	V
V_{IN}	Input Voltage	0		V_{CC}	V
T_{OPR}	Operating Temperature	-5		85	^{O}C

5.3 General DC Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{IL}	Input low current	no pull-up or pull-down	-1		1	µA
I_{IH}	Input high current	no pull-up or pull-down	-1		1	µA
I_{OZ}	Tri-state leakage current		-10		10	µA
C_{IN}	Input capacitance			4		ρF
C_{OUT}	Output capacitance			4		ρF
C_{BID}	Bi-directional buffer capacitance			4		ρF

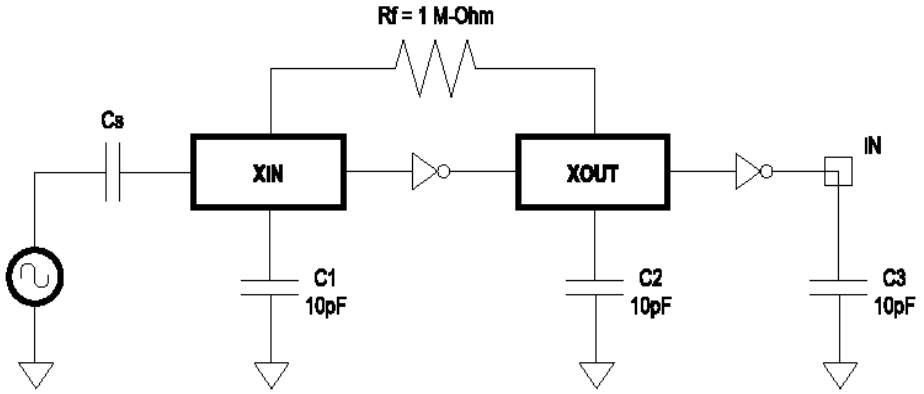
5.4 DC Electrical Characteristics for 5 volts operation

(Under Recommended Operating Conditions and V_{CC}=4.5v ~ 5.5v , Tj= -40°C to + 85°C)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IL}	Input Low Voltage	TTL			0.8	V
V_{IL}	Input Low Voltage	CMOS			$0.3*V_{CC}$	V
V_{IL}	Schmitt input Low Voltage	TTL		1.10		V
V_{IL}	Schmitt input Low Voltage	CMOS		1.84		V
V_{IH}	Input High Voltage	TTL	2.2			V
V_{IH}	Input Hight Voltage	CMOS	$0.7*V_{CC}$			V
V_{IH}	Schmitt input High Voltage	TTL		1.87		V
V_{IH}	Schmitt input High Voltage	CMOS		3.22		V
V_{OL}	Output low voltage	I_{OL}=2, 4, 8, 12, 16, 24 mA			0.4	V
V_{OH}	Output high voltage	I_{OH}=2, 4, 8, 12, 16, 24 mA	3.5			V
R_I	Input Pull-up/down resistance	$Vil=0_V$ or $Vih=V_{CC}$		50		KΩ

5.5 Crystal Oscillator Circuit Setup for Characterization

The following setup was used to measure the open loop voltage gain for crystal oscillator circuits. The feedback resistor serves to bias the circuit at its quiescent operating point and the AC coupling capacitor, Cs, is much larger than C1 and C2.



5.6 USB Transceiver Characteristics

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage		3.0	3.6	V
V_I	DC input voltage range		0	5.5	V
$V_{I/O}$	DC input range for I/Os		0	V_{CC}	V
V_O	DC output voltage range		0	V_{CC}	V
T_{AMB}	Operating ambient temperature range in free air	See DC and AC characteristics for individual device	0	70	°C

ABSOLUTE MAXIMUM RATINGS (Notes 1 and 2)

In accordance with the Absolute Maximum Rating System, Voltages are referenced to GND (Ground=0v)

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage		-0.5	+6.5	V
I_{IK}	DC input diode current	Vi<0		-50	mA
V_I	DC input voltage	Note 3	-0.5	+5.5	V
$V_{I/O}$	DC input voltage range for I/Os		-0.5	Vcc +0.5	V
I_{OK}	DC output diode current	Vo> Vcc or Vo<0		+/-50	mA
V_O	DC output voltage	Note 3	-0.5	Vcc +0.5	V
I_O	DC output source sink current for VP/VM and RCV pins	Vo=0 to Vcc		+/-15	mA
I_O	DC output source or sink current for D+/D- pins	Vo= 0 to Vcc		+/-50	mA
I_{CC}, I_{GND}	DC Vcc or GND current			+/-100	mA
T_{STO}	Storage temperature range		-60	+150	°C
P_{TOT}	Power dissipation per package				mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2. The performance capability of a high performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output clamp current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (Ground=0V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS -40°C to +85°C			UNIT
			MIN	TYP	MAX	
VHYS	Hysteresis on inputs	Vcc=3.0V to 3.6V (Note 3)	0.3	0.4	0.5	V
VIH	HIGH level input	Vcc=3.0V to 3.6V (Note 3)		1.5	2.0	V
VIL	LOW level input	Vcc=3.0V to 3.6V (Note 3)	0.8	1.1		V
RoH	Output impedance (HIGH state)	Note 2	28	34	43	ohm
RoL	Output impedance (LOW state)	Note 2	28	35	43	ohm
VOH	HIGH level output (Note 3)	Vcc=3.0V Io=6mA Vcc=3.0V Io=4mA Vcc=3.0V Io=100µA	2.2 2.4 2.8	2.7		V
VOL	LOW level output (Note 3)	Vcc=3.0V Io=6mA Vcc=3.0V Io=4mA Vcc=3.0V Io=100µA		0.3	0.7 0.4 0.2	V
IQ	Quiescent supply current	Vcc=3.6V V=Vcc or GND Io=0		330	600	µA
Isup	Supply current in suspend	Vcc=3.6V V=Vcc or GND Io=0			70	µA
IFS	Active supply current (Full Speed)	Vcc=3.3V		9	14	mA
ILS	Active supply current (Low Speed)	Vcc=3.3V		2		mA
ILeak	Input leakage current	Vcc=3.6V V=5.5V or GND, not for I/O Pins		+/-0.1	+/-0.5	µA
IOFF	3-state output OFF-state current	Vi=Vih or Vil; Vo=Vcc or GND			+/-10	µA

NOTES:

1. All typical values are at Vcc=3.3V and Tamb=25°C.
2. This value includes an external resistor of 24 ohm +/-1%. See "Load D+ and D-" diagram for testing details.
3. All signals except D+ and D-.

AC ELECTRICAL CHARACTERISTICS

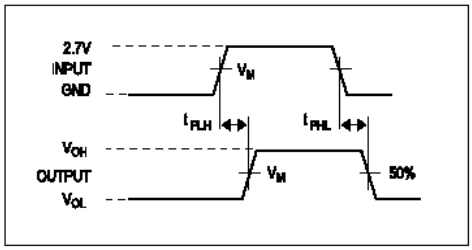
GND=0V, $t_R = t_F$ =3.0 ns; C_L =50 pF; RL=500 Ohms

SYMBOL	PARAMETER	WAVEFORM	LIMITS (T_{A})					UNIT
			0°C to +25°C			0°C to +70°C		
			MIN	TYP	MAX	MIN	MAX	
tpLH tpHL	VMO VPO to D+/D- Full Speed	1	0 0		12 12	0 0	14 14	ns
trise tfall	Rise and Fall Times Full Speed	2	4 4	9 9	20 20	4 4	20 20	ns
tRFM	Rise and Fall Time Matching Full Speed		90		110	90	110	%
tpLH tpHL	VMO VPO to D+/D- Low Speed	1		120 120	300 300		300 300	ns
trise tfall	Rise and Fall Times Low Speed	2	75 75		300 200	75 75	300 200	ns
tRFM	Rise and Fall Time Matching Low Speed		70		130	70	130	%
tpLH tpHL	D+/D- to RCV	3		9 9	16 16		16 16	ns
tpLH tpHL	D+/D- to VP/VM	1		4 4	8 8		8 8	ns
tpHZ tpZH tpLZ tpZL	OE# to D+/D- RL = 500ohm	4			12 12 10 10		12 12 10 10	ns
tsu	Setup for SPEED	5	0					ns
Vcr	Crossover point[1]	3	1.3		2.0	1.3	2.0	V

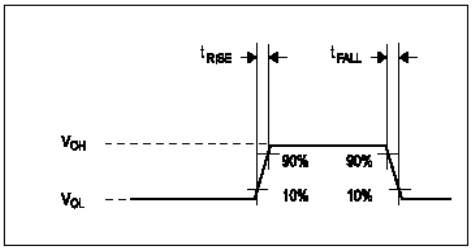
NOTES:

1. The crossover point is in the range of 1.3V to 2.5V for the low speed mode with a 50 pF capacitance.

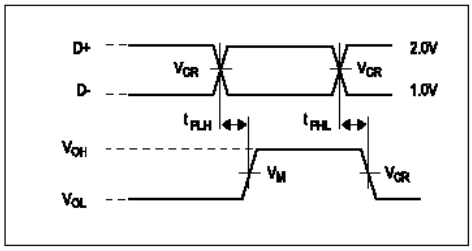
AC WAVEFORM 1.
D+/D- TO VP/VM OR VPO/VMO TO D+/D-



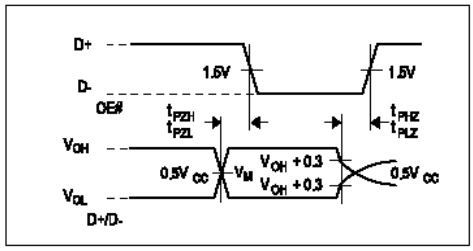
AC WAVEFORM 2.
RISE AND FALL TIMES



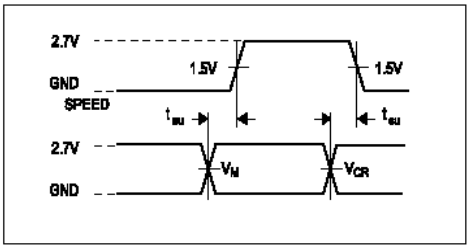
AC WAVEFORM 3.
D+/D- TO RCV



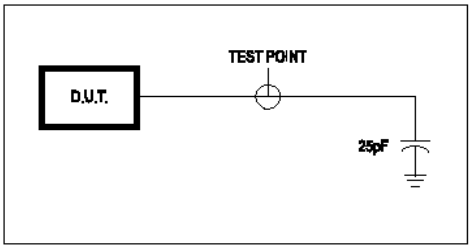
AC WAVEFORM 4.
OE# TO D/+/D-



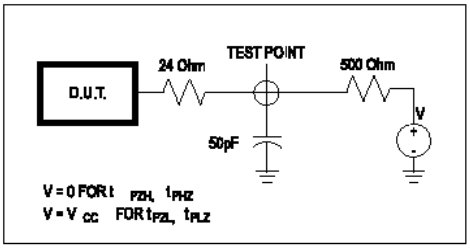
AC WAVEFORM 5.
SETUP FOR SPEED



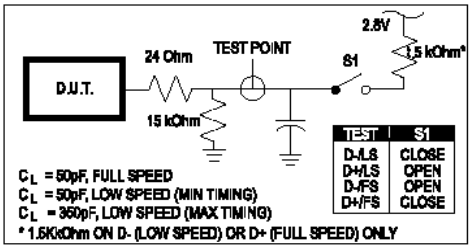
TEST CIRCUIT 1.
LOAD FOR VM/VP AND RCV



TEST CIRCUIT 2.
LOAD FOR ENABLE AND DISABLE TIMES



TEST CIRCUIT 3.
LOAD FOR D+/D-



5.7 ESD Test Results

Test Description: ESD Testing was performed on a Zapmaster system using the Human-Body-Model (HBM) and Machine-Model (MM), according to MIL-STD 883 and EIAJ IC-121 respectively.

- Human-Body-Model stresses devices by sudden application of a high voltage supplied by a 100pF capacitor through 1.5k-ohm resistance.
- Machine-Model stresses devices by sudden application of a high voltage supplied by a 200pF capacitor through very low (0 ohm) resistance.

Test Circuit & Condition

- Zap Interval: 1 second
- Number of Zaps: 3 positive and 3 negative at room temperature
- Criteria: I-V Curve Tracing

ESD Data

Model	Mode	S/S	Target	Results
HBM	Vdd, Vss, I/O	15	6000V	PASS
MM	Vdd, Vss, I/O	15	200V	PASS

5.8 Latch-Up Test Results

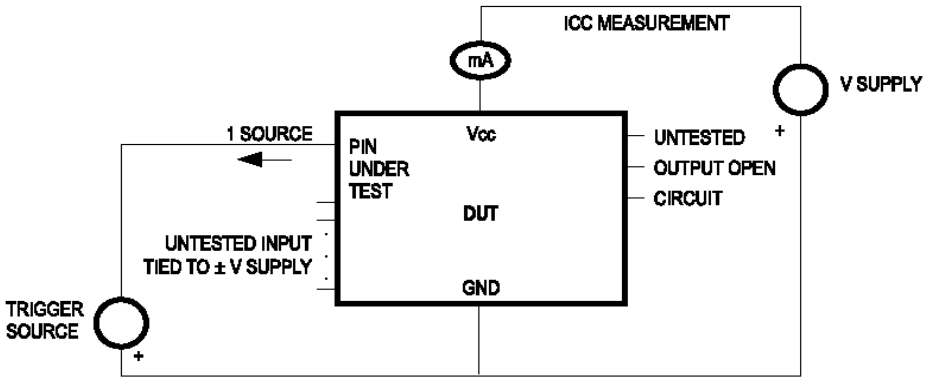
Test Description: Latch-Up testing was performed at room ambient using an IMCS-4600 system which applies a stepped voltage to one pin per device with all other pins open except Vdd and Vss which were biased to 5Volts and ground respectively.

Testing was started at 5.0V (Positive) or 0V (Negative), and the DUT was biased for 0.5 seconds.

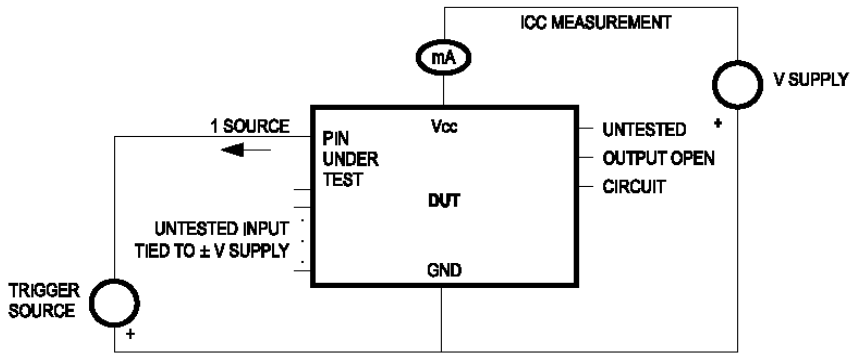
If neither the PUT current supply nor the device current supply reached the predefined limit (DUT=00mA, Icc=100mA), then the voltage was increased by 0.1Volts and the pin was tested again.

This procedure was recommended by the JEDEC JC-40.2 CMOS Logic standardization committee.

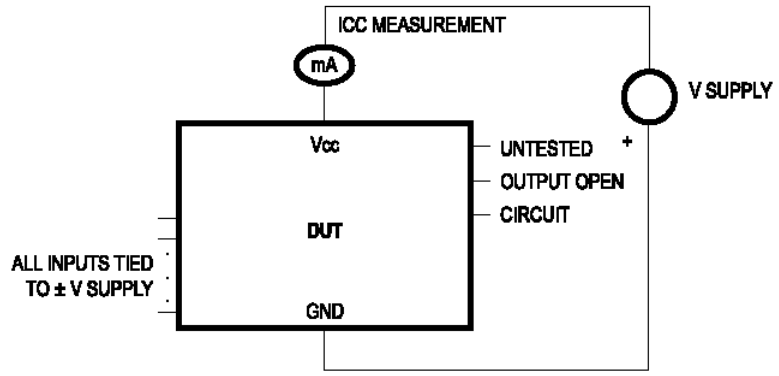
Notes:
1. DUT: The device under test.
2. PUT: The pin under test.



Test Circuit: Positive Input/Output Overvoltage/Overcurrent



Test Circuit: Negative Input/Output Overvoltage/Overcurrent

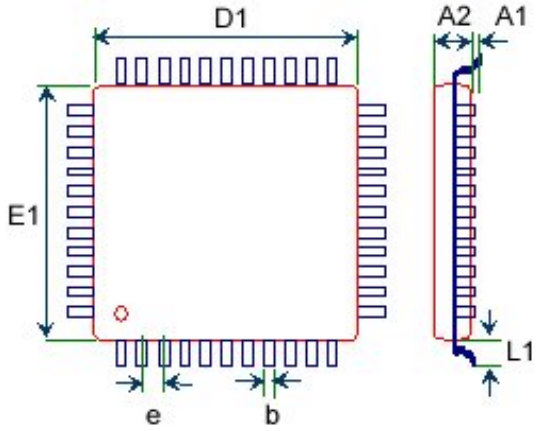


Supply Overvoltage Test

Latch-Up Data

Mode		Voltage (V)	Current (mA)	S/S	Results
Voltage	+	11.0		5	Pass
	-	11.0		5	Pass
Current	+		200	5	Pass
	-		200	5	Pass
Vdd - Vxx		9.0		5	Pass

6.0Mechanical Information



body size		lead	A1	A2	L1	b	c	e
D1	E1	count						
7	7	48	0.1	1.4	1	0.2	0.127	0.5

A1	stand-off
A2	body thickness
L1	lead length
b	lead width
c	lead thickness
e	lead pitch