Si2456/Si2433/Si2414

V.90, V.34, V.32bis ISOmodem™ Chipset with Integrated Global DAA

Features

- Data modem formats
  - ITU-T, Bell
  - 300 bps up to 56 kbps
  - V.42, V.42bis, MNP2-5
  - Automatic rate negotiation
- Caller ID decode
- 3.3 V power
- No external ROM or RAM required
- UART with flow control
- AT command set support
- Integrated DAA
  - Over 5000 V capacitive isolation
  - Parallel phone detect
  - Globally-compliant line interface
  - Overcurrent detection
- Fast connect
- Parallel interface
- Call progress support
- Firmware upgradeable

Applications

- Set-top boxes
- E-mail terminals
- Point-of-sale terminals
- Digital video recorders
- Security systems
- Remote monitoring

Description

The Si2456 is a complete, ITU-V.90-compliant, 56 kbps modem chipset with integrated direct access arrangement (DAA) that provides a programmable line interface to meet global telephone line requirements with a single design. Available in two small packages, it eliminates the need for a separate DSP data pump, external RAM and ROM, modem controller, codec, isolation transformer, relays, opto-isolators, and 2- to 4-wire hybrid. The ISOmodem™ chipset is ideal for embedded modem applications due to its small board space, low power consumption, and global compliance. The Si2433 and Si2414 products offer all the same features as the Si2456 with connect rates of up to 33.6 kbps and 14.4 kbps, respectively.

Functional Block Diagram

Ordering Information

This data sheet is valid only for those chipset combinations listed on page 66.

Pin Assignments

<table>
<thead>
<tr>
<th>Pin</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1-24</td>
<td>Si2456/33/14</td>
</tr>
<tr>
<td>2-23</td>
<td>Si2456/33/14</td>
</tr>
<tr>
<td>3-22</td>
<td>Si2456/33/14</td>
</tr>
<tr>
<td>4-21</td>
<td>Si2456/33/14</td>
</tr>
<tr>
<td>5-20</td>
<td>Si2456/33/14</td>
</tr>
<tr>
<td>6-19</td>
<td>Si2456/33/14</td>
</tr>
<tr>
<td>7-18</td>
<td>Si2456/33/14</td>
</tr>
<tr>
<td>8-17</td>
<td>Si2456/33/14</td>
</tr>
<tr>
<td>9-16</td>
<td>Si2456/33/14</td>
</tr>
<tr>
<td>10-15</td>
<td>Si2456/33/14</td>
</tr>
<tr>
<td>11-14</td>
<td>Si2456/33/14</td>
</tr>
<tr>
<td>12-13</td>
<td>Si2456/33/14</td>
</tr>
</tbody>
</table>

Patents pending
## TABLE OF CONTENTS

<table>
<thead>
<tr>
<th>Section</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>Electrical Specifications</td>
<td>4</td>
</tr>
<tr>
<td>Typical Application Schematic</td>
<td>11</td>
</tr>
<tr>
<td>Bill of Materials: Si2456/33/14 Chipset</td>
<td>12</td>
</tr>
<tr>
<td>Functional Description</td>
<td>17</td>
</tr>
<tr>
<td>Digital Interface</td>
<td>17</td>
</tr>
<tr>
<td>Serial Interface</td>
<td>17</td>
</tr>
<tr>
<td>Parallel Interface</td>
<td>17</td>
</tr>
<tr>
<td>Command Mode</td>
<td>18</td>
</tr>
<tr>
<td>Data Mode</td>
<td>18</td>
</tr>
<tr>
<td>Fast Connect</td>
<td>18</td>
</tr>
<tr>
<td>V.29 Fast Connect</td>
<td>18</td>
</tr>
<tr>
<td>Clocking/Low Power Modes</td>
<td>18</td>
</tr>
<tr>
<td>Data Compression</td>
<td>19</td>
</tr>
<tr>
<td>Error Correction</td>
<td>19</td>
</tr>
<tr>
<td>Wire Mode</td>
<td>19</td>
</tr>
<tr>
<td>Caller ID Operation</td>
<td>19</td>
</tr>
<tr>
<td>Parallel Phone Detection</td>
<td>19</td>
</tr>
<tr>
<td>Overcurrent Detection</td>
<td>21</td>
</tr>
<tr>
<td>Global Operation</td>
<td>21</td>
</tr>
<tr>
<td>Firmware Upgrades</td>
<td>21</td>
</tr>
<tr>
<td>EEPROM Interface</td>
<td>21</td>
</tr>
<tr>
<td>AT Commands</td>
<td>21</td>
</tr>
<tr>
<td>Extended AT Commands</td>
<td>26</td>
</tr>
<tr>
<td>S-Registers</td>
<td>36</td>
</tr>
<tr>
<td>User-Access Registers (U-Registers)</td>
<td>39</td>
</tr>
<tr>
<td>Bit-Mapped U-Register Detail (defaults in bold)</td>
<td>44</td>
</tr>
<tr>
<td>Parallel Interface Registers</td>
<td>60</td>
</tr>
<tr>
<td>Pin Descriptions: Si2456/33/14</td>
<td>62</td>
</tr>
<tr>
<td>Pin Descriptions: Si3015</td>
<td>64</td>
</tr>
<tr>
<td>Ordering Guide</td>
<td>66</td>
</tr>
<tr>
<td>Package Outline: 24-Pin TSSOP</td>
<td>67</td>
</tr>
<tr>
<td>Package Outline: 16-Pin SOIC</td>
<td>68</td>
</tr>
<tr>
<td>Document Change List</td>
<td>69</td>
</tr>
<tr>
<td>Contact Information</td>
<td>70</td>
</tr>
</tbody>
</table>
# Electrical Specifications

**Table 1. Recommended Operating Conditions**

<table>
<thead>
<tr>
<th>Parameter1</th>
<th>Symbol</th>
<th>Test Condition</th>
<th>Min2</th>
<th>Typ</th>
<th>Max2</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ambient Temperature</td>
<td>( T_A )</td>
<td>K-Grade, F-Grade</td>
<td>0</td>
<td>25</td>
<td>70</td>
<td>°C</td>
</tr>
<tr>
<td>Ambient Temperature</td>
<td>( T_A )</td>
<td>B-Grade</td>
<td>–40</td>
<td>25</td>
<td>85</td>
<td>°C</td>
</tr>
<tr>
<td>Si2456/33/14 Supply Voltage, Digital3</td>
<td>( V_D )</td>
<td>3.0</td>
<td>3.3</td>
<td>3.6</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

**Notes:**

1. The Si2456/33/14 specifications are guaranteed when the typical application circuit (including component tolerance) and any Si2456/33/14 and any Si3015 are used. See "Typical Application Schematic" on page 11.
2. All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise stated.
3. The digital supply, \( V_D \), operates from 3.0 to 3.6 V. The Si2456/33/14 interface supports 5 V logic (CLKIN/XTALI supports 3.3 V logic only).
### Table 2. DAA Loop Characteristics

(V_D = 3.0 to 3.6 V, T_A = 0 to 70 °C for K-Grade)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC Termination Voltage</td>
<td>V_TR</td>
<td>I_L = 20 mA, ACT^1 = 1 DCT = 11 (CTR21)</td>
<td>—</td>
<td>—</td>
<td>7.5</td>
<td>V</td>
</tr>
<tr>
<td>DC Termination Voltage</td>
<td>V_TR</td>
<td>I_L = 42 mA, ACT = 1 DCT = 11 (CTR21)</td>
<td>—</td>
<td>—</td>
<td>14.5</td>
<td>V</td>
</tr>
<tr>
<td>DC Termination Voltage</td>
<td>V_TR</td>
<td>I_L = 50 mA, ACT = 1 DCT = 11 (CTR21)</td>
<td>—</td>
<td>—</td>
<td>40</td>
<td>V</td>
</tr>
<tr>
<td>DC Termination Voltage</td>
<td>V_TR</td>
<td>I_L = 60 mA, ACT = 1 DCT = 11 (CTR21)</td>
<td>40</td>
<td>—</td>
<td>—</td>
<td>V</td>
</tr>
<tr>
<td>DC Termination Voltage</td>
<td>V_TR</td>
<td>I_L = 20 mA, ACT = 0 DCT = 01 (Japan)</td>
<td>—</td>
<td>—</td>
<td>6.0</td>
<td>V</td>
</tr>
<tr>
<td>DC Termination Voltage</td>
<td>V_TR</td>
<td>I_L = 100 mA, ACT = 0 DCT = 01 (Japan)</td>
<td>9</td>
<td>—</td>
<td>—</td>
<td>V</td>
</tr>
<tr>
<td>DC Termination Voltage</td>
<td>V_TR</td>
<td>I_L = 20 mA, ACT = 0 DCT = 10 (FCC)</td>
<td>—</td>
<td>—</td>
<td>7.5</td>
<td>V</td>
</tr>
<tr>
<td>DC Termination Voltage</td>
<td>V_TR</td>
<td>I_L = 100 mA, ACT = 0 DCT = 10 (FCC)</td>
<td>9</td>
<td>—</td>
<td>—</td>
<td>V</td>
</tr>
<tr>
<td>On-Hook Leakage Current</td>
<td>I_LK</td>
<td>V_TR = -48 V</td>
<td>—</td>
<td>—</td>
<td>7</td>
<td>µA</td>
</tr>
<tr>
<td>Operating Loop Current</td>
<td>I_LP</td>
<td>FCC/Japan Modes</td>
<td>13</td>
<td>—</td>
<td>120</td>
<td>mA</td>
</tr>
<tr>
<td>Operating Loop Current</td>
<td>I_LP</td>
<td>CTR21</td>
<td>13</td>
<td>—</td>
<td>60</td>
<td>mA</td>
</tr>
<tr>
<td>DC Ring Current^2</td>
<td></td>
<td>DC flowing through ring detection circuitry</td>
<td>—</td>
<td>—</td>
<td>7</td>
<td>µA</td>
</tr>
<tr>
<td>Ring Detect Voltage^3</td>
<td>V_RD</td>
<td>RT = 0</td>
<td>11</td>
<td>—</td>
<td>22</td>
<td>V_{rms}</td>
</tr>
<tr>
<td>Ring Detect Voltage^3</td>
<td>V_RD</td>
<td>RT = 1</td>
<td>17</td>
<td>—</td>
<td>33</td>
<td>V_{rms}</td>
</tr>
<tr>
<td>Ring Frequency</td>
<td>F_R</td>
<td></td>
<td>15</td>
<td>—</td>
<td>68</td>
<td>Hz</td>
</tr>
<tr>
<td>Ringer Equivalence Number^4</td>
<td>REN</td>
<td></td>
<td>—</td>
<td>—</td>
<td>0.2</td>
<td></td>
</tr>
</tbody>
</table>

**Notes:**
1. ACT = U67, bit 5; DCT = U67, bits 3:2; RT = U67, bit 0; RZ = U67, bit 1.
2. R25 and R26 installed.
3. The ring signal is guaranteed to not be detected below the minimum. The ring signal is guaranteed to be detected above the maximum.
4. C15, R14, Z2, and Z3 not installed. RZ = 0.
Figure 1. Test Circuit for Loop Characteristics

Table 3. DC Characteristics, $V_D = 3.3$ V
($V_D = 3.0$ to 3.6 V, $T_A = 0$ to 70 °C for K-Grade)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>High Level Input Voltage</td>
<td>$V_{IH}$</td>
<td></td>
<td>2.0</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Low Level Input Voltage</td>
<td>$V_{IL}$</td>
<td></td>
<td></td>
<td></td>
<td>0.8</td>
<td>V</td>
</tr>
<tr>
<td>High Level Output Voltage</td>
<td>$V_{OH}$</td>
<td>$I_O = -2$ mA</td>
<td>2.4</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Low Level Output Voltage</td>
<td>$V_{OL}$</td>
<td>$I_O = 2$ mA</td>
<td></td>
<td></td>
<td>0.35</td>
<td>V</td>
</tr>
<tr>
<td>Input Leakage Current</td>
<td>$I_L$</td>
<td></td>
<td>-10</td>
<td></td>
<td>10</td>
<td>µA</td>
</tr>
<tr>
<td>Pullup Resistance Pins 3,4,9,11,13,14,16,23,24</td>
<td>$R_{PU}$</td>
<td></td>
<td>50</td>
<td>100</td>
<td>200</td>
<td>kΩ</td>
</tr>
<tr>
<td>Total Supply Current$^*$</td>
<td>$I_D$</td>
<td>$V_{D33}$ pin</td>
<td></td>
<td>26</td>
<td>35</td>
<td>mA</td>
</tr>
<tr>
<td>Total Supply Current, Powerdown$^*$</td>
<td>$I_D$</td>
<td>PDN = 1</td>
<td></td>
<td>35</td>
<td>100</td>
<td>µA</td>
</tr>
</tbody>
</table>

*Note: All inputs at 0 or $V_D$. All inputs held static except clock, and all outputs unloaded (Static $I_{OUT} = 0$ mA).
## Table 4. DAA AC Characteristics

\(^{(V_D = 3.0 \text{ to } 3.6 \text{ V}, T_A = 0 \text{ to } 70 ^\circ \text{C for K-Grade)}}\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sample Rate</td>
<td>Fs</td>
<td></td>
<td>—</td>
<td>9.6</td>
<td>—</td>
<td>kHz</td>
</tr>
<tr>
<td>Crystal Oscillator Frequency</td>
<td>F_{XTL}</td>
<td></td>
<td>—</td>
<td>4.9152</td>
<td>—</td>
<td>MHz</td>
</tr>
<tr>
<td>Transmit Frequency Response</td>
<td></td>
<td>Low –3 dBFS Corner</td>
<td>—</td>
<td>5</td>
<td>—</td>
<td>Hz</td>
</tr>
<tr>
<td>Receive Frequency Response</td>
<td></td>
<td>Low –3 dBFS Corner</td>
<td>—</td>
<td>5</td>
<td>—</td>
<td>Hz</td>
</tr>
<tr>
<td>Transmit Full Scale Level(^1)</td>
<td>V_{FS}</td>
<td></td>
<td>—</td>
<td>1</td>
<td>—</td>
<td>V_{PEAK}</td>
</tr>
<tr>
<td>Receive Full Scale Level(^1)</td>
<td>V_{FS}</td>
<td></td>
<td>—</td>
<td>1</td>
<td>—</td>
<td>V_{PEAK}</td>
</tr>
<tr>
<td>Dynamic Range(^2,3,4)</td>
<td>DR</td>
<td>ACT(^5) = 0, DCT(^5) = 10 (FCC) IL = 100 mA</td>
<td>82</td>
<td>—</td>
<td>—</td>
<td>dB</td>
</tr>
<tr>
<td>Dynamic Range(^2,3,6)</td>
<td>DR</td>
<td>ACT = 0, DCT = 01 (Japan) IL = 20 mA</td>
<td>83</td>
<td>—</td>
<td>—</td>
<td>dB</td>
</tr>
<tr>
<td>Dynamic Range(^2,3,4)</td>
<td>DR</td>
<td>ACT = 1, DCT = 11 (CTR21) IL = 60 mA</td>
<td>84</td>
<td>—</td>
<td>—</td>
<td>dB</td>
</tr>
<tr>
<td>Transmit Total Harmonic Distortion(^4,7)</td>
<td>THD</td>
<td>ACT = 0, DCT = 10 (FCC) IL = 100 mA</td>
<td>—</td>
<td>—85</td>
<td>—</td>
<td>dB</td>
</tr>
<tr>
<td>Transmit Total Harmonic Distortion(^5,7)</td>
<td>THD</td>
<td>ACT = 0, DCT = 01 (Japan) IL = 20 mA</td>
<td>—</td>
<td>—76</td>
<td>—</td>
<td>dB</td>
</tr>
<tr>
<td>Receive Total Harmonic Distortion(^6,7)</td>
<td>THD</td>
<td>ACT = 0, DCT = 01 (Japan) IL = 20 mA</td>
<td>—</td>
<td>—74</td>
<td>—</td>
<td>dB</td>
</tr>
<tr>
<td>Receive Total Harmonic Distortion(^4,7)</td>
<td>THD</td>
<td>ACT = 1, DCT = 11 (CTR21) IL = 60 mA</td>
<td>—</td>
<td>—82</td>
<td>—</td>
<td>dB</td>
</tr>
<tr>
<td>AOOUT Dynamic Range</td>
<td>VIN = 1 kHz</td>
<td></td>
<td>—</td>
<td>40</td>
<td>—</td>
<td>dB</td>
</tr>
<tr>
<td>AOOUT THD</td>
<td>VIN = 1 kHz</td>
<td></td>
<td>—</td>
<td>40</td>
<td>—</td>
<td>dB</td>
</tr>
<tr>
<td>AOOUT Full-Scale Level</td>
<td></td>
<td></td>
<td>—</td>
<td>0.7V_{DD}</td>
<td>—</td>
<td>V_{PP}</td>
</tr>
<tr>
<td>AOOUT Mute Level</td>
<td></td>
<td></td>
<td>—</td>
<td>60</td>
<td>—</td>
<td>dB</td>
</tr>
</tbody>
</table>

**Notes:**

1. Measured at TIP and RING with 600 Ω termination at 1 kHz.
2. DR = 20 x log |Vin| + 20 x log (RMS signal/RMS noise).
3. Measurement is 300 to 3400 Hz. Applies to transmit and receive paths.
4. Vin = 1 kHz, –3 dBFS, Fs = 10300 Hz.
5. ACT = U67, bit 5; DCT = U67, bits 3:2.
6. Vin = 1 kHz, –6 dBFS, Fs = 10300 Hz.
7. THD = 20 x log (RMS distortion/RMS signal).
### Table 5. Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC Supply Voltage</td>
<td>V_D</td>
<td>4.1</td>
<td>V</td>
</tr>
<tr>
<td>Input Current, Si2456/33/14 Digital Input Pins</td>
<td>I_IN</td>
<td>±10</td>
<td>µA</td>
</tr>
<tr>
<td>Digital Input Voltage</td>
<td>V_IND</td>
<td>-0.3 to 5.3</td>
<td>V</td>
</tr>
<tr>
<td>CLKIN/XTALI Input Voltage</td>
<td>V_XIND</td>
<td>-0.3 to (V_D + 0.3)</td>
<td>V</td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td>T_A</td>
<td>-10 to 100</td>
<td>°C</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>T_STG</td>
<td>-40 to 150</td>
<td>°C</td>
</tr>
</tbody>
</table>

**Note:** Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### Table 6. Switching Characteristics

(V_D = 3.0 to 3.6 V, T_A = 0 to 70 °C for K-Grade)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLKOUT Output Clock Frequency</td>
<td>t_BD</td>
<td>2.4576</td>
<td>—</td>
<td>39.3216</td>
<td>MHz</td>
</tr>
<tr>
<td>Baud Rate Accuracy</td>
<td>t_BR</td>
<td>-1</td>
<td>—</td>
<td>1</td>
<td>%</td>
</tr>
<tr>
<td>Start Bit ↓ to RTS ↓</td>
<td>t_RTH</td>
<td>—</td>
<td>1/(2 x Baud Rate)</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>CTS or RTS ↑ High to Start Bit↓</td>
<td>t_RTS</td>
<td>10</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>RESET ↓ to RESET ↑</td>
<td>t_RS</td>
<td>5.0</td>
<td>—</td>
<td>—</td>
<td>ms</td>
</tr>
<tr>
<td>RESET ↑ to 1st AT Command</td>
<td>t_AT</td>
<td>300</td>
<td>—</td>
<td>—</td>
<td>ms</td>
</tr>
<tr>
<td>Address Setup</td>
<td>t_AS</td>
<td>15</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>Address Hold</td>
<td>t_AH</td>
<td>0</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>WR Low Pulse Width</td>
<td>t_WL</td>
<td>50</td>
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<tr>
<td>Write Data Setup Time</td>
<td>t_WDSU</td>
<td>20</td>
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<tr>
<td>Write Cycle Time</td>
<td>t_GC</td>
<td>120</td>
<td>—</td>
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<td>ns</td>
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<tr>
<td>Chip Select Setup</td>
<td>t_CSS</td>
<td>10</td>
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<tr>
<td>Chip Select Hold</td>
<td>t_CSH</td>
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<tr>
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<td>t_RL</td>
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<td>ns</td>
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<tr>
<td>RD Low to Data Driven Time</td>
<td>t_RLDD</td>
<td>—</td>
<td>—</td>
<td>20</td>
<td>ns</td>
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<tr>
<td>Data Hold</td>
<td>t_DH</td>
<td>10</td>
<td>—</td>
<td>—</td>
<td>ns</td>
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<tr>
<td>RD High to Hi-Z Time</td>
<td>t_DZ</td>
<td>—</td>
<td>—</td>
<td>30</td>
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<tr>
<td>Read Cycle Time</td>
<td>t_RC</td>
<td>120</td>
<td>—</td>
<td>—</td>
<td>ns</td>
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</table>

**Note:** All timing is referenced to the 50% level of the waveform. Input test levels are V_{IH} = V_D – 0.4 V, V_{IL} = 0.4 V
UART Time for Modem Receive Path (8N1 Mode)

UART Timing for Modem Transmit Path (9N1 Mode with 9th Bit Escape)

Figure 2. Asynchronous UART Serial Interface Timing Diagram
Figure 3. Parallel Interface Read Timing

Figure 4. Parallel Interface Write Timing
## Bill of Materials: Si2456/33/14 Chipset

<table>
<thead>
<tr>
<th>Component</th>
<th>Value</th>
<th>Supplier(s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1,C4(^1)</td>
<td>150 pF, 3 kV, X7R, ±20%</td>
<td>Novacap, Venkel, Johanson, Murata, Panasonic</td>
</tr>
<tr>
<td>C3,C13,C35,C36</td>
<td>0.22 µF, 16 V, X7R, ±20%</td>
<td>Novacap, Venkel, Johanson, Murata, Panasonic</td>
</tr>
<tr>
<td>C5(^2)</td>
<td>0.1 µF, 50 V, Elec/Tant, ±20%</td>
<td>Venkel, Johanson, Murata, Panasonic</td>
</tr>
<tr>
<td>C6,C10,C16,C37</td>
<td>0.1 µF, 16 V, X7R, ±20%</td>
<td>Novacap, Venkel, Johanson, Murata</td>
</tr>
<tr>
<td>C7,C8(^3)</td>
<td>560 pF, 250 V, X7R, ±20%</td>
<td>Novacap, Venkel, Johanson, Murata, Panasonic</td>
</tr>
<tr>
<td>C9</td>
<td>22 nF, 250 V, X7R, ±20%</td>
<td>Novacap, Venkel, Johanson, Murata, Panasonic</td>
</tr>
<tr>
<td>C12</td>
<td>1.0 µF, 16 V, Tant, ±20%</td>
<td>Venkel, Panasonic</td>
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<tr>
<td>C14(^4)</td>
<td>0.68 µF, 16 V, X7R/Elec/Tant, ±20%</td>
<td>Novacap, Venkel, AUX, Murata, Panasonic</td>
</tr>
<tr>
<td>C18,C19(^3)</td>
<td>3.9 nF, 16 V, X7R, ±20%</td>
<td>Novacap, Venkel, Johanson, Murata</td>
</tr>
<tr>
<td>C20</td>
<td>0.01 µF, 16 V, X7R, ±20%</td>
<td>Novacap, Venkel, Johanson, Murata</td>
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<tr>
<td>C22(^4)</td>
<td>1800 pF, 50 V, X7R, ±20%</td>
<td>Not installed</td>
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<tr>
<td>C24,C25(^1)</td>
<td>1000 pF, 3 kV, X7R, ±10%</td>
<td>Novacap, Venkel, Johanson, Murata, Panasonic</td>
</tr>
<tr>
<td>C26,C27</td>
<td>33 pF, 16 V, NPO, ±5%</td>
<td>Novacap, Venkel, Johanson, Murata</td>
</tr>
<tr>
<td>C30(^4)</td>
<td>10 pF, 16 V, NPO, ±10%</td>
<td>Not Installed</td>
</tr>
<tr>
<td>C38,C39(^2,5)</td>
<td>47 pF, 16 V, X7R, ±10%</td>
<td>Venkel</td>
</tr>
<tr>
<td>D1,D2(^6)</td>
<td>Dual Diode, 300 V, 225 mA</td>
<td>Central Semiconductor</td>
</tr>
<tr>
<td>D3,D4(^1)</td>
<td>BAV99 Dual Diode, 70 V, 350 mW</td>
<td>Diodes Inc., OnSemiconductor, Fairchild</td>
</tr>
<tr>
<td>FB1,FB2</td>
<td>Ferrite Bead, 600 Ω, ±25%, 200 mA</td>
<td>Murata</td>
</tr>
<tr>
<td>L1,L2(^2,5)</td>
<td>68 µH, 120 mA, 4 Ω max, ±10%</td>
<td>Murata, Panasonic</td>
</tr>
<tr>
<td>Q1,Q3</td>
<td>A42, NPN, 300 V</td>
<td>OnSemiconductor, Fairchild, Zetex</td>
</tr>
<tr>
<td>Q2</td>
<td>A92, PNP, 300 V</td>
<td>OnSemiconductor, Fairchild, Zetex</td>
</tr>
<tr>
<td>Q4(^7)</td>
<td>BCP56, NPN, 60 V, 1/2 W</td>
<td>OnSemiconductor, Fairchild</td>
</tr>
</tbody>
</table>

**Notes:**
1. The Si2456/33/14 design survives up to 3500 V longitudinal surges without R27, R28, D3, D4, Z4, and Z5. Adding the R27, R28, D3, D4, Z4, and Z5 enhanced lightning options increases longitudinal surge survival to greater than 6600 V. The isolation capacitors, C1, C4, C24, and C25, must also be rated to greater than the surge voltage. Y-class capacitors are recommended for highest surge survival.
2. For FCC-only designs, C14, C38, C39, R12, R13, R31, and R32 are not required (leave Si3015 pin 12 unconnected); L1 and L2 may be replaced with a short; R2 may be ±5%; with Z1 rated at 18 V, C5 may be rated at 16 V; also see Note 9.
3. If the auto answer, ring detect, and caller ID features are not used, R9, R10, C7, and C8 may be removed.
4. C22 and C30 may provide an additional improvement in emissions/immunity, depending on design and layout. Population option recommended. See “AN70: Si2456/Si2433/Si2414/Si2403 Modem Designer’s Guide” for details.
5. Compliance with EN55022 and/or CISPR-22 conductance disturbance tests requires the following: L1, L2, C38, C39, R31, and R32, D1 and D2 must be 400 V-rated, and RV2 must be populated. See also “EN55022 and CISPR-22 Compliance” in “AN70: Si2456/Si2433/Si2414/Si2403 Modem Designer’s Guide”.
6. Several diode bridge configurations are acceptable (suppliers include General Semi., Diodes Inc.)
7. Q4 may require copper on board to meet 1/2 W power requirement. (Contact manufacturer for details.)
8. RV2 can be installed to improve performance for multiple longitudinal surges.
9. The R7, R8, R15, and R16, R17, R19 resistors may each be replaced with a single resistor of 1.78 kΩ, 3/4 W, ±1%. For FCC-only designs, 1.78 kΩ, 1/16 W, ±5% resistors may be used.
10. If the parallel phone detection feature is not used, R25 and R26 may be removed.
11. To ensure compliance with ITU specifications, frequency tolerance must be less than 100 ppm including initial accuracy, 5-year aging, 0 to 70 °C, and capacitive loading. Crystals with 50 ppm initial accuracy typically satisfy this requirement.
<table>
<thead>
<tr>
<th>Component</th>
<th>Value</th>
<th>Supplier(s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>RV1</td>
<td>Sidactor, 275 V, 100 A</td>
<td>Teccor, ST Microelectronics, Microsemi, TI</td>
</tr>
<tr>
<td>RV2⁵,⁸</td>
<td>270 V, MOV</td>
<td>Not Installed</td>
</tr>
<tr>
<td>R2²</td>
<td>402 Ω, 1/16 W, ±1%</td>
<td>Venkel, Panasonic</td>
</tr>
<tr>
<td>R5</td>
<td>100 kΩ, 1/16 W, ±1%</td>
<td>Venkel, Panasonic</td>
</tr>
<tr>
<td>R6</td>
<td>120 kΩ, 1/16 W, ±5%</td>
<td>Venkel, Panasonic</td>
</tr>
<tr>
<td>R7, R8, R15, R16, R17, R19⁹</td>
<td>5.36 kΩ, 1/4 W, ±1%</td>
<td>Venkel, Panasonic</td>
</tr>
<tr>
<td>R9, R10³</td>
<td>56 kΩ, 1/10 W, ±5%</td>
<td>Venkel, Panasonic</td>
</tr>
<tr>
<td>R11</td>
<td>9.3 kΩ, 1/16 W, ±1%</td>
<td>Venkel, Panasonic</td>
</tr>
<tr>
<td>R12²</td>
<td>78.7 Ω, 1/16 W, ±1%</td>
<td>Venkel, Panasonic</td>
</tr>
<tr>
<td>R13²</td>
<td>215 Ω, 1/16 W, ±1%</td>
<td>Venkel, Panasonic</td>
</tr>
<tr>
<td>R18</td>
<td>2.2 kΩ, 1/10 W, ±5%</td>
<td>Venkel, Panasonic</td>
</tr>
<tr>
<td>R24</td>
<td>150 Ω, 1/16 W, ±5%</td>
<td>Venkel, Panasonic</td>
</tr>
<tr>
<td>R25, R26¹⁰</td>
<td>10 MΩ, 1/16 W, ±5%</td>
<td>Venkel, Panasonic</td>
</tr>
<tr>
<td>R27, R28¹</td>
<td>10 Ω, 1/10 W, ±5%</td>
<td>Venkel, Panasonic</td>
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<tr>
<td>R31, R32²,⁵</td>
<td>470 Ω, 1/16 W, ±5%</td>
<td>Venkel, Panasonic</td>
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<td>U1</td>
<td>Si2456/33/14</td>
<td>Silicon Labs</td>
</tr>
<tr>
<td>U2</td>
<td>Si3015</td>
<td>Silicon Labs</td>
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<td>Y1</td>
<td>4.9152 MHz, 20 pF, 100 ppm¹¹, 150 ESR</td>
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<tr>
<td>Z1¹</td>
<td>Zener Diode, 43 V, 1/2 W</td>
<td>Vishay, OnSemiconductor, Rohm</td>
</tr>
<tr>
<td>Z4, Z5¹</td>
<td>Zener Diode, 5.6 V, 1/2 W</td>
<td>Vishay, OnSemiconductor, Rohm</td>
</tr>
</tbody>
</table>

Notes:
1. The Si2456/33/14 design survives up to 3500 V longitudinal surges without R27, R28, D3, D4, Z4, and Z5. Adding the R27, R28, D3, D4, Z4, and Z5 enhanced lightning options increases longitudinal surge survival to greater than 6600 V. The isolation capacitors, C1, C4, C24, and C25, must also be rated to greater than the surge voltage. Y-class capacitors are recommended for highest surge survival.
2. For FCC-only designs, C14, C38, C39, R12, R13, R31, and R32 are not required (leave Si3015 pin 12 unconnected); L1 and L2 may be replaced with a short; R2 may be ±5%; with Z1 rated at 18 V, C5 may be rated at 16 V; also see Note 9.
3. If the auto answer, ring detect, and caller ID features are not used, R9, R10, C7, and C8 may be removed.
4. C22 and C30 may provide an additional improvement in emissions/immunity, depending on design and layout. Population option recommended. See “AN70: Si2456/Si2433/Si2414/Si2403 Modem Designer’s Guide” for details.
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7. Q4 may require copper on board to meet 1/2 W power requirement. (Contact manufacturer for details.)
8. RV2 can be installed to improve performance for multiple longitudinal surges.
9. The R7, R8, R15, and R16, R17, R19 resistors may each be replaced with a single resistor of 1.78 kΩ, 3/4 W, ±1%. For FCC-only designs, 1.78 kΩ, 1/16 W, ±5% resistors may be used.
10. If the parallel phone detection feature is not used, R25 and R26 may be removed.
11. To ensure compliance with ITU specifications, frequency tolerance must be less than 100 ppm including initial accuracy, 5-year aging, 0 to 70 °C, and capacitive loading. Crystals with 50 ppm initial accuracy typically satisfy this requirement.
Table 7. Protocol Characteristics

<table>
<thead>
<tr>
<th>Data Rate</th>
<th>Specification</th>
</tr>
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<tbody>
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<td>56 kbps</td>
<td>ITU-T V.90</td>
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<tr>
<td>54.666 kbps</td>
<td>ITU-T V.90</td>
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<tr>
<td>53.333 kbps</td>
<td>ITU-T V.90</td>
</tr>
<tr>
<td>52 kbps</td>
<td>ITU-T V.90</td>
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<td>50.666 kbps</td>
<td>ITU-T V.90</td>
</tr>
<tr>
<td>49.333 kbps</td>
<td>ITU-T V.90</td>
</tr>
<tr>
<td>48 kbps</td>
<td>ITU-T V.90</td>
</tr>
<tr>
<td>46.666 kbps</td>
<td>ITU-T V.90</td>
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<td>ITU-T V.90</td>
</tr>
<tr>
<td>30.666 kbps</td>
<td>ITU-T V.90</td>
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<tr>
<td>29.333 kbps</td>
<td>ITU-T V.90</td>
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<td>28 kbps</td>
<td>ITU-T V.90</td>
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<td>14.4 kbps</td>
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<td>ITU-T V.34 or V.32bis</td>
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<td>ITU-T V.34, V.32bis, or V.29</td>
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<tr>
<td>7200 bps</td>
<td>ITU-T V.34 or V.32bis</td>
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<tr>
<td>4800 bps</td>
<td>ITU-T V.34 or V.32bis</td>
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<tr>
<td>2400 bps</td>
<td>ITU-T V.34 or V.22bis</td>
</tr>
<tr>
<td>1200 bps</td>
<td>ITU-T V.22bis, V.23, or Bell 212A</td>
</tr>
<tr>
<td>300 bps</td>
<td>ITU-T V.21</td>
</tr>
<tr>
<td>300 bps</td>
<td>Bell 103</td>
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Notes:
1. Supported on Si2456 only.
2. Supported on Si2456 and Si2433 only.
<table>
<thead>
<tr>
<th>Item</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Data Format</strong></td>
<td>Selectable 8, 9, 10, or 11 bits per character</td>
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<tr>
<td>Compatibility</td>
<td>ITU-T V.90(^1), V.34(^2), V.32bis, V.32, V.23, V.22bis, V.22, V.21, Bell 212A, and Bell 103</td>
</tr>
<tr>
<td><strong>Operating Mode</strong></td>
<td>Two-wire full duplex</td>
</tr>
<tr>
<td><strong>Data Modulation</strong></td>
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</tr>
<tr>
<td>28 to 56 kbps(^1)</td>
<td>V.90 as specified by ITU-T</td>
</tr>
<tr>
<td>2.4 to 33.6 kbps(^2)</td>
<td>V.34 as specified by ITU-T</td>
</tr>
<tr>
<td>14.4 kbps</td>
<td>128-level TCM/2400 Baud ±0.01%</td>
</tr>
<tr>
<td>12.0 kbps</td>
<td>64-level TCM/2400 Baud ±0.01%</td>
</tr>
<tr>
<td>9600 bps</td>
<td>32-level TCM/2400 Baud ±0.01%</td>
</tr>
<tr>
<td>9600 bps</td>
<td>16-level QAM/2400 Baud ±0.01%</td>
</tr>
<tr>
<td>7200 bps</td>
<td>V.29 QAM as specified by ITU-T</td>
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<tr>
<td>4800 bps</td>
<td>16-level TCM/2400 Baud ±0.01%</td>
</tr>
<tr>
<td>2400 bps</td>
<td>4-level QAM/2400 Baud ±0.01%</td>
</tr>
<tr>
<td>1200 bps</td>
<td>16-level QAM/600 Baud ±0.01%</td>
</tr>
<tr>
<td>0 to 300 bps</td>
<td>4-level PSK/600 Baud ±0.01%</td>
</tr>
<tr>
<td></td>
<td>FSK 0–300 Baud ±0.01%</td>
</tr>
<tr>
<td><strong>Answer Tone</strong></td>
<td></td>
</tr>
<tr>
<td>ITU-T V.32bis, V.32, V.22bis, V.22, and V.21 modes</td>
<td>2100 Hz ±3 Hz</td>
</tr>
<tr>
<td>Bell 212A and 103 modes</td>
<td>2225 Hz ±3 Hz</td>
</tr>
<tr>
<td><strong>Transmit Carrier</strong></td>
<td></td>
</tr>
<tr>
<td>V.90(^1)</td>
<td>As specified by ITU-T</td>
</tr>
<tr>
<td>V.34(^2)</td>
<td>As specified by ITU-T</td>
</tr>
<tr>
<td>ITU-T V.32bis</td>
<td>1800 Hz ±0.01%</td>
</tr>
<tr>
<td>ITU-T V.32</td>
<td>1800 Hz ±0.01%</td>
</tr>
<tr>
<td>ITU-T V.22, V.22bis/Bell 212A</td>
<td>1200 Hz ±0.5 Hz</td>
</tr>
<tr>
<td></td>
<td>2400 Hz ±1 Hz</td>
</tr>
<tr>
<td>ITU-T V.21</td>
<td>Mark (980 Hz ±12 Hz) Space (1180 Hz ±12 Hz)</td>
</tr>
<tr>
<td></td>
<td>Mark (1650 Hz ±12 Hz) Space (1850 Hz ±12 Hz)</td>
</tr>
<tr>
<td></td>
<td>Mark (1270 Hz ±12 Hz) Space (1070 Hz ±12 Hz)</td>
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<td></td>
<td>Mark (2225 Hz ±12 Hz) Space (2025 Hz ±12 Hz)</td>
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<tr>
<td><strong>Output Level</strong></td>
<td></td>
</tr>
<tr>
<td>Permissive—Switched network</td>
<td>−9 dBm maximum</td>
</tr>
</tbody>
</table>

**Notes:**
1. Supported on Si2456 only.
2. Supported on Si2456 and Si2433 only.
## Table 7. Protocol Characteristics (Continued)

<table>
<thead>
<tr>
<th>Item</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Receive Carrier</strong>&lt;br&gt;ITU-T V.90&lt;sup&gt;1&lt;/sup&gt;&lt;br&gt;ITU-T V.34&lt;sup&gt;2&lt;/sup&gt;&lt;br&gt;ITU-T V.32bis&lt;br&gt;ITU-T V.32&lt;br&gt;ITU-T V.22, V.22bis/Bell 212A&lt;br&gt; Originate mode&lt;br&gt; Answer mode&lt;br&gt;ITU-T V.21&lt;br&gt; Originate mode&lt;br&gt; Answer mode&lt;br&gt;Bell 103&lt;br&gt; Originate mode&lt;br&gt; Answer mode</td>
<td>As specified by ITU-T&lt;br&gt;1800 Hz ±7 Hz&lt;br&gt;2400 Hz ±7 Hz&lt;br&gt;Mark (980 Hz ±12 Hz) Space (1180 Hz ±12 Hz)&lt;br&gt;Mark (1650 Hz ±12 Hz) Space (1850 Hz ±12 Hz)&lt;br&gt;Mark (2225 Hz ±12 Hz) Space (2025 Hz ±12 Hz)&lt;br&gt;Mark (1270 Hz ±12 Hz) Space (1070 Hz ±12 Hz)</td>
</tr>
<tr>
<td><strong>Carrier Detect</strong> (level for ITU-T V.22bis, V.22, V.21, 212, 103) in Switched Network</td>
<td>Acquisition (~43 dBm)&lt;br&gt;Release (~48 dBm)</td>
</tr>
<tr>
<td><strong>Hysteresis</strong></td>
<td>2 dBm minimum</td>
</tr>
</tbody>
</table>

**Note:** ITU-T V.90<sup>1</sup>, V.34<sup>2</sup>, V.32/V.32bis are echo-canceling protocols that use signal quality as criteria for maintaining connection. They also provide for self-training detection to force disconnect.

<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Line Equalization</strong></td>
<td>Automatic Adaptive</td>
</tr>
<tr>
<td><strong>Connection Options</strong></td>
<td>Loss of Carrier in ITU-T V.22bis and lower</td>
</tr>
<tr>
<td><strong>Phone Types</strong></td>
<td>500 (rotary dial), 2500 (DTMF dial)</td>
</tr>
<tr>
<td><strong>Dialing</strong></td>
<td>Pulse and Tone</td>
</tr>
<tr>
<td><strong>DTMF Output Level</strong></td>
<td>Per Part 68</td>
</tr>
<tr>
<td><strong>Pulse Dial Ratio</strong></td>
<td>Make/Break: 39/61%</td>
</tr>
<tr>
<td><strong>Ring Cadence</strong></td>
<td>On 2 seconds; Off 4 seconds</td>
</tr>
<tr>
<td><strong>Call Progress Monitor</strong></td>
<td>BUSY&lt;br&gt;CONNECT (rate)&lt;br&gt;NO ANSWER&lt;br&gt;NO CARRIER&lt;br&gt;NO DIALTONE&lt;br&gt;OK&lt;br&gt;RING&lt;br&gt;RINGING</td>
</tr>
</tbody>
</table>

**Notes:**
1. Supported on Si2456 only.
2. Supported on Si2456 and Si2433 only.
Functional Description

The ISOmodem™ chipset is a complete embedded modem chipset with integrated direct-access arrangement (DAA) that provides a programmable line interface to meet global telephone line requirements. Available in two small packages, this solution includes a DSP data pump, a modem controller, on-chip RAM and ROM, an analog front end (AFE), a DAA, and analog output.

The Si2456/33/14 accepts standard modem AT commands and provides connect rates up to 56/33.6/14.4 kbps full-duplex over the Public Switched Telephone Network (PSTN). The Si2456/33/14 features a complete set of modem protocols including all ITU-T standard formats up to 56 kbps.

The Si2456/33/14 provides numerous additional features for embedded modem applications. The modem includes full caller ID detection and decoding for global standards. Call progress is supported through echoing result codes and is also programmable to meet global settings. Because the Si2456/33/14 integrates the DAA, analog features, such as parallel phone detect, overcurrent detection, and global PTT compliance with a single design, are included.

This device is ideal for embedded modem applications due to its small board space, low power consumption, and global compliance. The Si2456/33/14 solution includes a silicon DAA using Silicon Laboratories’ proprietary ISOcap™ technology. This highly-integrated DAA can be programmed to meet worldwide PTT specifications for ac termination, dc termination, ringer impedance, and ringer threshold. In addition, the Si2456/33/14 has been designed to meet the most stringent worldwide requirements for out-of-band energy, billing-tone immunity, lightning surges, and safety requirements.

The Si2456/33/14 is designed to be rapidly incorporated into existing modem applications. The device interfaces directly through either a serial UART to a microcontroller or to a PC through a standard RS-232 transceiver. This interface allows for PC evaluation of the modem immediately upon powerup via the AT commands using standard terminal software. The Si2456/33/14 also provides an 8-bit parallel port.

The Si2456/33/14 solution requires only a few low-cost discrete components to achieve global compliance. See the “Typical Application Schematic” on page 11.

Digital Interface

The ISOmodem chipset digital I/O can be configured as either a serial UART interface with flow control or a parallel 8-bit interface.

Selection of a serial or parallel I/O interface is determined by the state of AOUT/INT (Si2456/33/14, pin 13) during the rising edge of RESET. An internal pullup resistor forces the default state to serial mode operation. An external 10 kΩ pulldown resistor can be connected to AOUT/INT to force selection of parallel mode. Additionally, when selecting parallel mode, CS should remain high until after the rising edge of RESET. Configuration of pins 3, 4, 8–11, 13–16, and 22–24 is determined by this interface selection.

Serial Interface

The ISOmodem chipset supports Data Terminal Equipment (DTE) rates up to 307.2 kbps with the standard serial UART format. Upon powerup, the UART defaults to a 19.2 kbps baud rate. If a pulldown resistor ≤ 10 kΩ is placed between D2 (Si2456/33/14, pin 16) and GND (Si2456/33/14, pin 6), the DTE rate is set by the autobaud feature after reset.

The serial interface also provides a hardware pin, DCD (data carrier detect), which remains low as long as the Si2456/33/14 is connected.

The INT interrupt pin can be programmed to alert the host of changes to the interrupts listed in I/O Control 0 (U70).

Autobaud

The ISOmodem chipset includes an automatic baud rate detection feature that allows the host to start transmitting data at any standard DTE rate from 300 bps to 307.2 kbps. This feature is enabled by placing a pulldown resistor ≤ 10 kΩ between D2 (pin 16) and GND.

Parallel Interface

The parallel interface is an 8-bit data bus with a single bit address. Figure 3 on page 10 shows the required timing for the parallel interface.

If A0 = 0, the data bus represents a read/write to the “Parallel Interface 0 (0x00)” register on page 60. If A0 = 1, the data bus represents a read/write to the “Parallel Interface 1 (0x01)” register on page 61.
Command Mode
Upon reset, the ISOmodem chipset is in Command mode and accepts “AT” commands. An outgoing modem call can be made using the “ATDT#” (tone dial) or “ATDP#” (pulse dial) command after the device is configured. If the handshake is successful, the modem responds with the response codes detailed in Table 12 on page 33 and enters data mode.

Data Mode
The ISOmodem chipset is in Data mode while it has a connection to another modem or is in the process of establishing a connection.

In Command and Data mode, the Si2456/33/14 operates in asynchronous DTE mode only. Data protocols are available to provide error correction to improve reliability (V.42 and MNP2-4) and data compression to increase throughput (V.42bis and MNP5).

Each connection between two modems in Data mode begins with a handshaking sequence. During that sequence, the modems determine the line speed, data protocol, and related parameters for the data link. Configuration through AT commands determines the range of choices available to the modem during the negotiation process.

Fast Connect
The ISOmodem chipset supports a Fast Connect mode of operation to reduce the time of a connect sequence in originate mode. The Fast Connect modes can be enabled for V.21, V.22, V.22bis, Bell103, Bell212, and V.29 modulations. In addition, the Si2456/33/14 may be set to either default asynchronous data communications equipment (DCE) mode or a transparent HDLC synchronous mode.

V.29 Fast Connect
In addition to the low modulation speed fast connect modes, the ISOmodem chipset also supports a fast connect mode based on the 9600 bps V.29 fax modulation standard. In order to provide a time-critical interface from the host to the Si2456/33/14, the Si2456/33/14 uses an interface derived from the fax class 1 AT command set. See “AN70: Si2456/Si2433/Si2414/Si2403 Modem Designer’s Guide” for more details.

Clocking/Low Power Modes
The ISOmodem chipset contains an on-chip phase-locked loop (PLL) and clock generator. Using either a single crystal or master clock input, the Si2456/33/14 can generate all the internal clocks required to support the featured modem protocols. Either a 4.9152 MHz clock (3.3 V max input—see Table 5 on page 8) on XTAL1 or a 4.9152 MHz crystal across XTAL1 and XTAL0 forms the master clock (±100 ppm max) for the Si2456/33/14. This clock source is sent to an internal PLL that generates all necessary internal system clocks including the DSP clock. Figure 5 shows a block diagram of how the DSP clock and the CLKOUT are derived.

Using the S24 S-register, the Si2456/33/14 can be set to automatically enter sleep mode after a pre-programmed time of inactivity with either the DTE or the remote modem. The sleep mode is entered after (S24) seconds have passed since the TX FIFO has been empty. The Si2456/33/14 remains in the sleep state until either a 1 to 0 transition on TXD (serial mode) or a 1 to 0 transition on CS occurs.

Additionally, the Si2456/33/14 may be placed in a complete Powerdown mode. Complete powerdown is accomplished via U65[13] (PDN). Once the PDN bit is written, the Si2456/33/14 completely powers down and can only be powered back on via the RESET pin.

A 78.6432 MHz/(R1 + 1) clock is produced on the CLKOUT pin that may be used as an external system clock. R1 may be programmed via U5E to any value between 1 and 31 (default value = 31).
The modem can achieve DTE (host-to-ISOmodem chipset) speeds greater than the maximum DCE (modem-to-modem) speed through the use of a data compression protocol. The compression protocols available are the ITU-T V.42bis and MNP5 protocols. Data compression attempts to increase throughput by compressing the data before actually sending it. The modem is, thus able to transmit more data in a given period of time.

Error Correction
The ISOmodem chipset can employ error-correction (reliable) protocols to ensure error-free delivery of asynchronous data sent between the host and the remote end. The Si2456/33/14 supports V.42 and MNP2-4 error correction protocols. V.42 (LAPM) is most commonly used and is enabled by default.

Wire Mode
Wire mode is used to communicate with standard non-error correcting modems. When optioned with ‘\N3, the ISOmodem chipset falls back to wire mode if it fails in an attempt to negotiate a V.42 or MNP link with the remote modem. Error correction and data compression are not active in wire mode.

Caller ID Operation
The ISOmodem chipset supports full type 1 caller ID detection and decode for the US Bellcore, European ETSI, UK, and Japanese caller ID protocols. Caller ID is enabled via the +VCID and +VCDT commands.

Parallel Phone Detection
The ISOmodem chipset is able to detect when another telephone, modem, or other device is using the phone line. This allows the host to avoid interrupting another phone call when the phone line is already in use and to intelligently handle an interruption when the Si2456/33/14 is using the phone line.

On-Hook Line-in-Use Detection
When the ISOmodem chipset is sharing the telephone line with other devices, it is important that it not interrupt a call in progress. To detect whether another device is using the shared telephone line, the host can use the Si2456/33/14 to monitor the TIP-RING dc voltage with the LVCS (Line Voltage and Current Sense) register (U79, bits 4:0). See Figure 6 on page 20. See also the %Vn commands for automatic line-in-use detection.

Off-Hook Intrusion Detection
When the ISOmodem chipset is off-hook, an algorithm is implemented in the Si2456/33/14 to automatically monitor the TIP-RING loop current via the LVCS register. When the Si2456/33/14 is off-hook, the LVCS register switches from representing the TIP-RING voltage to representing the TIP-RING current. (See Figure 7 on page 20.) Upon detecting an intrusion, the Si2456/33/14 alerts the host to the condition via the INT pin.
Figure 6. Loop Voltage

Figure 7. Loop Current
Overcurrent Detection
The ISOmodem chipset includes an overcurrent detection feature that measures the loop current at a programmable time after the Si2456/33/14 goes off-hook. This allows the Si2456/33/14 to detect if it is connected to an improper telephone line. The overcurrent detection feature may be enabled by setting the OCDM bit (U70, bit 11). OHT (U77, bits 8:0) sets the delay after off-hook until the loop current is measured.

In the CTR21 mode of operation, the overcurrent detection can trip unnecessarily for loop current values greater than 55 mA. Therefore, if the Si2456/33/14 is in CTR21 mode and an overcurrent condition is detected, the host should switch the Si2456/33/14 into FCC mode and check the LVCS register for a valid overcurrent value equal to 0x1F.

Global Operation
The ISOmodem chipset contains an integrated silicon direct-access arrangement (Silicon DAA) that provides a programmable line interface to meet international telephone line interface requirements. “AN70: Si2456/Si2433/Si2414/Si2403 Modem Designer’s Guide” gives the DAA register settings required to meet international PTT standards.

Additionally, the user-access registers (via the AT:U and AT:R commands) may be programmed for country-specific settings, such as dial tone, ring, ringback, and busy tone. See AN70 for complete details.

Firmware Upgrades
The ISOmodem chipset contains an on-chip program ROM that includes the firmware required for the features listed in this data sheet. In addition, the Si2456/33/14 contains on-chip program RAM to accommodate minor changes to the ROM firmware. This allows Silicon Labs to provide future firmware updates to optimize the characteristics of new modem designs and those already deployed in the field. See AN70 for further information.

EEPROM Interface
The ISOmodem chipset supports an optional serial peripheral interface (SPI) bus serial EEPROM. The EEPROM must support SPI mode 3 with a 16-bit (8 kbit – 64 kbit range) address. Upon powerup, if a pulldown resistor $\leq 10 \, k\Omega$ is placed between D6 (Si2456, pin 4) and GND, the Si2456 attempts to detect an EEPROM. An installed EEPROM may contain custom default settings, firmware upgrades, and/or user-defined AT command macros for use in custom AT commands or country codes.

AT Commands
At powerup, the Si2456/33/14 is in the AT Command mode. In Command mode, the modem monitors the input (serial or parallel) checking constantly for a valid command. (AT commands are described in Table 8.)
## Table 8. Basic AT Command Set (Command Defaults in Bold)

<table>
<thead>
<tr>
<th>Command</th>
<th>Action</th>
</tr>
</thead>
<tbody>
<tr>
<td>$</td>
<td>Display AT Command mode settings.</td>
</tr>
<tr>
<td>A</td>
<td>Answer incoming call.</td>
</tr>
<tr>
<td>A/</td>
<td>Re-execute last command. This is the only command not preceded by “AT” or followed by a &lt;CR&gt;.</td>
</tr>
</tbody>
</table>
| Dn      | Dial
The dial command, which may be followed by one or more dial command modifiers, manually dials a phone number:

<table>
<thead>
<tr>
<th>Modifier</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>! or &amp;</td>
<td>Flash hook switch for FHT (U4F) ms (default: 500 ms)</td>
</tr>
<tr>
<td>, or &lt;</td>
<td>Pause before continuing for S8 seconds (default: 2 seconds)</td>
</tr>
<tr>
<td>;</td>
<td>Return to AT Command mode after verifying dialtone and dialing any digits.</td>
</tr>
<tr>
<td>G</td>
<td>Telephone voting mode. This modifier, intended for use in Japan, enables a special dial-in voting mode that may be used with certain automated voting systems. When this modifier is placed anywhere in the dial string (e.g. ATDG), the Si2456/33/14/03 will dial the phone number and wait S7 seconds (60 by default) to detect a busy tone. When the busy tone is detected, the Si2456/33/14/03 will report whether or not a polarity reversal occurs between the time the last digit is dialed and the detection of the busy tone. The Si2456/33/14/03 will report either “POLARITY REVERSAL” or “NO POLARITY REVERSAL”. It is not possible to establish a modem connection when using this command.</td>
</tr>
<tr>
<td>P</td>
<td>Pulse (rotary) dialing—pulse digits: 0, 1, 2, 3, 4, 5, 6, 7, 8, 9</td>
</tr>
<tr>
<td>T</td>
<td>Tone (DTMF) dialing—DTMF digits: *, #, A, B, C, D, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9.</td>
</tr>
</tbody>
</table>
| W        | Wait for dial tone before continuing for S14 seconds (default: 12 seconds). Blind dialing modes X0, X1, and X3 do not affect the W command.
If the DOP bit (U7A, bit 7) is set, the “ATTW” command will cause the Si2456/33/14 to pause dialing and either report an “OK” if a dialtone is detected or “NO DIALTONE” if a dial tone is not detected. |
| En       | Local DTE echo |
| E0       | Disable |
| **E1**   | Enable |
| Hn       | Hook switch. |
| H0       | Go on-hook (hang up modem). |
| H1       | Go off-hook. |
| In       | Identification and checksum. |
### Table 8. Basic AT Command Set (Command Defaults in Bold) (Continued)

<table>
<thead>
<tr>
<th>Command</th>
<th>Action</th>
</tr>
</thead>
</table>
| I0      | Display Si2456/33/14 revision code.  
         | B: Revision B  
         | C: Revision C, etc. |
| I1      | Display Si2456/33/14 firmware revision code (numeric). |
| I3      | Display line-side revision code.  
         | 15D = Si3015 revision D |
| I6      | Display the Si2456/33/14 model number.  
         | “2414” = Si2414  
         | “2433” = Si2433  
         | “2456” = Si2456 |
| I7      | Diagnostic Results 1. See “AN70: Si2456/Si2433/Si2414/Si2403 Modem Designer’s Guide” for details. |
| I8      | Diagnostic Results 2. See AN70 for details. |
| M0      | **Speaker is always off.**  
         | M1      | Speaker is on while dialing and handshaking; off in Data mode.  
         | M2      | Speaker is always on.  
         | M3      | Speaker is off while dialing; on during handshaking and retraining.  
         | On      | Return to Data mode from Command mode operation.  
         | O0      | Return to Data mode.  
         | O1      | Return to Data mode and perform a full retrain (at any speed except 300 bps).  
         | O2      | Return to Data mode and perform rate renegotiation.  
         | Qn      | Response mode.  
         | Q0      | **Enable result codes (see Table 12 on page 33)**  
         | Q1      | Disable result codes (enable quiet mode).  
         | R       | Initiate V.23 reversal.  
         | Sn      | S-register operation (see Table 13 on page 36).  
         | S$      | List contents of all S registers.  
         | Sn?     | Display contents of S-register n.  
         | Sn=x    | Set S-register n to value x (where n and x are decimal values).  
         | Vn      | Result code type (see Table 12 on page 33).  
         | V0      | Numeric result codes.  
         | V1      | **Verbal result codes**  
         | Xn      | Call Progress Monitor (CPM)—This command controls which CPM signals are monitored and reported to the host from the Si2456/33/14. (See Table 12 on page 33.)  
         | X0      | Basic results; disable CPM—Blind dial (does not wait for dial tone). CONNECT message does not include speed.  
         | X1      | Extended results; disable CPM—Blind dial. CONNECT message includes speed.  
         | X2      | Extended results and detect dial tone only—Add dial tone detection to X1 mode. Does not blind dial.  
         | X3      | Extended results and detect busy only—Add busy tone detection to X1 mode. |
### Table 8. Basic AT Command Set (Command Defaults in Bold) (Continued)

<table>
<thead>
<tr>
<th>Command</th>
<th>Action</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>X4</strong></td>
<td>Extended results, full CPM—Full CPM enabled, CONNECT message includes speed.</td>
</tr>
<tr>
<td><strong>X5</strong></td>
<td>Extended results—Full CPM enabled including ringback detection. Adds ringback detection to X4 mode.</td>
</tr>
<tr>
<td><strong>Yn</strong></td>
<td>Long space disconnect—Modem hangs up after 1.5 seconds or more of continuous space while on-line.</td>
</tr>
<tr>
<td><strong>Y0</strong></td>
<td>Disable.</td>
</tr>
<tr>
<td><strong>Y1</strong></td>
<td>Enable.</td>
</tr>
<tr>
<td><strong>Z</strong></td>
<td>Hard Reset—This command is functionally equivalent to pulsing the RESET pin low. (See tAT in Table 6 on page 8.)</td>
</tr>
<tr>
<td><strong>:E</strong></td>
<td>Read from serial EEPROM.</td>
</tr>
<tr>
<td><strong>:I</strong></td>
<td>Interrupt Read—This command causes the Si2456/33/14 to report the lower 8 bits of the interrupt register I/O Control 0 (U70). The CID, OCD, PPD, and RI bits are also cleared, and the INT pin (INT bit in parallel mode) is deactivated on this read.</td>
</tr>
<tr>
<td><strong>:M</strong></td>
<td>Write to serial EEPROM.</td>
</tr>
<tr>
<td><strong>:P</strong></td>
<td>Program RAM Write—This command is used to upload firmware supplied by Silicon Labs to the Si2456/33/14. The format for this command is AT:Paaaa,xxxx,yyyy,.... where aaaa is the first address in hexadecimal, and xxxx,yyyy,.... is data in hexadecimal. Only one :P command is allowed per AT command line. No other commands can be concatenated in the :P command line. This command is only for use with special files provided by Silicon Laboratories. Do not attempt to use this command for any other purpose. Use &amp;T6 to display checksum for patch verification.</td>
</tr>
<tr>
<td><strong>:R</strong></td>
<td>User-Access Register Read—This command allows the user to read from the user-access registers. (See pages 39–57.) The format is “AT:Raa”, where aa = user-access address in hexadecimal. The “AT:R” command causes all the U- registers to be displayed.</td>
</tr>
<tr>
<td><strong>:U</strong></td>
<td>User-Access Register Write—This command allows the user to write to the 16-bit user-access registers. (See page 39.) The format is “AT:Uaa,xxxx,yyyy,zzzz,...” where aa = user-access address in hexadecimal. xxxx = data in hexadecimal to be written to location aa. yyyy = data in hexadecimal to be written to location (aa + 1). zzzz = data in hexadecimal to be written to location (aa + 2). etc.</td>
</tr>
<tr>
<td><strong>+VCID = X</strong></td>
<td>Caller ID Enable.</td>
</tr>
<tr>
<td>X</td>
<td>Mode</td>
</tr>
<tr>
<td>0</td>
<td>Off</td>
</tr>
<tr>
<td>1</td>
<td>On—formatted</td>
</tr>
<tr>
<td>2</td>
<td>On—raw data format</td>
</tr>
<tr>
<td><strong>+VCDT = X</strong></td>
<td>Caller ID Type.</td>
</tr>
<tr>
<td>X</td>
<td>Mode</td>
</tr>
<tr>
<td>0</td>
<td>After ring only</td>
</tr>
<tr>
<td>1</td>
<td>Always on</td>
</tr>
<tr>
<td>2</td>
<td>UK</td>
</tr>
<tr>
<td>3</td>
<td>Japan</td>
</tr>
</tbody>
</table>
Table 8. Basic AT Command Set (Command Defaults in Bold) (Continued)

<table>
<thead>
<tr>
<th>Command</th>
<th>Action</th>
</tr>
</thead>
<tbody>
<tr>
<td>+FCLASS = X</td>
<td>Class 1 Mode Enable.</td>
</tr>
<tr>
<td>X Mode</td>
<td>Enables support for Class 1 mode for use in the V.29 Fast Connect mode.</td>
</tr>
<tr>
<td>0 Off</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
</tr>
</tbody>
</table>

| +FTM = X | Class 1 Transmit Carrier. |
| X Mode | |
| 2 | Transmit V.21 (980 Hz) tone and detect (2100/2225 Hz) tone. Stop transmit 980 Hz when 2100/2225 detected. |
| 53 | Same as &T4, but transmit V.29 7200 bps. Data pattern set by S40 register. AT + FCLASS = 0 must be sent to restore the Si2456/33/14 to normal operation after test. |
| 54 | Same as &T4, but transmit V.29 9600 bps. Data pattern set by S40 register. AT + FCLASS = 0 must be sent to restore the Si2456/33/14 to normal operation after test. |
| 95 | V.29 short synchronous. |
| 96 | V.29 full synchronous. |

| +FRM = X | Class 1 Transmit Carrier. |
| X Mode | |
| 2 | Detect V.21 (980 Hz) tone for longer than 100 ms, then send answer tone (2100/2225 Hz) for 200 ms. |
| 95 | V.29 short synchronous. |
| 96 | V.29 full synchronous. |

| +GCI = X | Country settings - Automatically configure all registers for a particular country. |
| X Country | |
| 0 Japan | |
| B4 United Kingdom | |
| B5 United States | |

**Note:** U-registers will be configured to Silicon Laboratories’ recommended values. Changes may be made by writing individual registers after sending the AT+GCI command. Several countries use the same configurations as the United Kingdom and the United States. Refer to “AN70: Si2456/Si2433/ Si2414/Si2403 Modem Designer’s Guide” for details.

| +GCI? | List current country code setting (response is: + GCI:<setting>) |
| +GCI = ? | List all possible country code settings. |
Extended AT Commands

The extended AT commands are supported by the Si2456/33/14 and are described in Tables 9 through 11.

### Table 9. Extended AT& Command Set (Command Defaults in Bold)

<table>
<thead>
<tr>
<th>Command</th>
<th>Action</th>
</tr>
</thead>
<tbody>
<tr>
<td>&amp;$</td>
<td>Display AT&amp; current settings.</td>
</tr>
<tr>
<td>&amp;D0</td>
<td>ESC (pin 22) is not used.</td>
</tr>
<tr>
<td>&amp;D1</td>
<td>ESC (pin 22) escapes to command mode from data mode if also enabled by HES U70, bit 15.</td>
</tr>
<tr>
<td>&amp;D2</td>
<td>ESC (pin 22) assertion during a modem connection causes the modem to go on-hook and return to command mode.</td>
</tr>
<tr>
<td>&amp;D3</td>
<td>ESC (pin 22) assertion causes ATZ command (reset and return OK result code).</td>
</tr>
<tr>
<td>&amp;Gn</td>
<td>Line connection rate limit—This command sets an upper limit on the line speed that the Si2456/33/14 can connect. Note that the &amp;Hn commands may limit the line speed as well (&amp;Gn not used for &amp;H0 or &amp;H1). Not all modulations support rates given by &amp;G. Any improper setting will be ignored.</td>
</tr>
<tr>
<td>&amp;G3</td>
<td>1200 bps max</td>
</tr>
<tr>
<td>&amp;G4</td>
<td>2400 bps max</td>
</tr>
<tr>
<td>&amp;G5</td>
<td>4.8 kbps max</td>
</tr>
<tr>
<td>&amp;G6</td>
<td>7.2 kbps max</td>
</tr>
<tr>
<td>&amp;G7</td>
<td>9.6 kbps max</td>
</tr>
<tr>
<td>&amp;G8</td>
<td>12 kbps max</td>
</tr>
<tr>
<td>&amp;G9</td>
<td>14.4 kbps max (default for Si2414)</td>
</tr>
<tr>
<td>&amp;G10</td>
<td>16.8 kbps max</td>
</tr>
<tr>
<td>&amp;G11</td>
<td>19.2 kbps max</td>
</tr>
<tr>
<td>&amp;G12</td>
<td>21.6 kbps max</td>
</tr>
<tr>
<td>&amp;G13</td>
<td>24 kbps max</td>
</tr>
<tr>
<td>&amp;G14</td>
<td>26.4 kbps max</td>
</tr>
<tr>
<td>&amp;G15</td>
<td>28.8 kbps max</td>
</tr>
<tr>
<td>&amp;G16</td>
<td>31.2 kbps max</td>
</tr>
<tr>
<td>&amp;G17</td>
<td>33.6 kbps max (default for Si2456 and Si2433)</td>
</tr>
<tr>
<td>&amp;Hn</td>
<td>Switched network handsháke mode—&amp;Hn commands must be on a separate command line from ATD, ATA, or ATO commands.</td>
</tr>
<tr>
<td>&amp;H0</td>
<td>V.90 with automatic fallback (56 kbps to 300 bps) (default for Si2456)</td>
</tr>
<tr>
<td>&amp;H1</td>
<td>V.90 only (56 kbps to 28 kbps)</td>
</tr>
<tr>
<td>&amp;H2</td>
<td>V.34 with automatic fallback (33.6 kbps to 300 bps) (default for Si2433)</td>
</tr>
<tr>
<td>&amp;H3</td>
<td>V.34 only (33.6 kbps to 2400 bps)</td>
</tr>
<tr>
<td>&amp;H4</td>
<td>ITU-T V.32bis with automatic fallback (14.4 kbps to 300 bps) (default for Si2414)</td>
</tr>
<tr>
<td>&amp;H5</td>
<td>ITU-T V.32bis only (14.4 kbps to 4800 bps)</td>
</tr>
<tr>
<td>&amp;H6</td>
<td>ITU-T V.22bis only (2400 bps or 1200 bps)</td>
</tr>
<tr>
<td>&amp;H7</td>
<td>ITU-T V.22 only (1200 bps)</td>
</tr>
</tbody>
</table>
### Table 9. Extended AT& Command Set (Command Defaults in Bold) (Continued)

<table>
<thead>
<tr>
<th>Command</th>
<th>Action</th>
</tr>
</thead>
<tbody>
<tr>
<td>&amp;H8</td>
<td>Bell 212 only (1200 bps)</td>
</tr>
<tr>
<td>&amp;H9</td>
<td>Bell 103 only (300 bps)</td>
</tr>
<tr>
<td>&amp;H10</td>
<td>ITU-T V.21 only (300 bps)</td>
</tr>
<tr>
<td>&amp;H11</td>
<td>V.23 (1200/75 bps)</td>
</tr>
<tr>
<td>&amp;Pn</td>
<td>Japan pulse dialing</td>
</tr>
<tr>
<td>&amp;P0</td>
<td>Configure Si2456/33/14 for 10 pulse-per-second pulse dialing. For Japan.</td>
</tr>
<tr>
<td>&amp;P1</td>
<td>Configure Si2456/33/14 for 20 pulse-per-second pulse dialing. For Japan.</td>
</tr>
<tr>
<td>&amp;Tn</td>
<td>Test Mode</td>
</tr>
<tr>
<td>&amp;T0</td>
<td>Cancel Test Mode (Escape to Command mode to issue AT&amp;T0). This command will also report the number of bit errors encountered on the previous &amp;T4 test.</td>
</tr>
<tr>
<td>&amp;T2</td>
<td>Initiate ITU-T V.54 (ANALOOP) test. Modulation set by &amp;H AT command. Test loop is through the DSP (Si2456/33/14 device) only. The Si2456/33/14 echoes data from TX pin (Register 0 in parallel mode) back to RX pin (Register 0 in parallel mode).</td>
</tr>
<tr>
<td>&amp;T3</td>
<td>Initiate ITU-T V.54 (ANALOOP) test. Modulation set by &amp;H AT command. Test loop is through the DSP (Si2456/33/14), DAA interface section (Si2456/33/14), ISOcap interface (Si3015), and analog hybrid circuit (Si3015). Si2456/33/14 echoes data from TX pin (Register 0 in parallel mode) back to RX pin (Register 0 in parallel mode). Phone line termination required as in Figure 1. To test only the ISOcap link operation, the hybrid and AFE codec can be removed from the test loop by setting the DL bit (U62, bit 1).</td>
</tr>
<tr>
<td>&amp;T4</td>
<td>Initiate transmit as originating modem with automatic data generation. Modulation, data rate, and symbol rate are set by &amp;H, &amp;G, and S41. Data pattern is set by the S40 register. Continues until the ATH command is sent after an escape into command mode. Data is also demodulated as in ANALOOP, and any bit errors are counted to be displayed after the test using &amp;T0.</td>
</tr>
<tr>
<td>&amp;T5</td>
<td>Initiate transmit as answering modem with automatic data generation. Modulation, data rate, and symbol rate are set by &amp;H, &amp;G, and S41. Data pattern is set by the S40 register. Continues until the ATH command is sent after an escape into command mode. Data is also demodulated as in ANALOOP, and any bit errors are counted to be displayed after the test using &amp;T0.</td>
</tr>
<tr>
<td>&amp;T6</td>
<td>Compute checksum for firmware-upgradeable section of program memory. If no firmware upgrade is installed, &amp;T6 returns 0xDE5C.</td>
</tr>
<tr>
<td>&amp;Xn</td>
<td>Automatic determination of telephone line type.</td>
</tr>
<tr>
<td>&amp;X0</td>
<td>Abort &amp;x1 or &amp;x2 command.</td>
</tr>
<tr>
<td>&amp;X1</td>
<td>Automatic determination of telephone line type. Result code: WXYZn.</td>
</tr>
<tr>
<td>W:</td>
<td>0 = line supports DTMF dialing.</td>
</tr>
<tr>
<td></td>
<td>1 = line is pulse dial only.</td>
</tr>
<tr>
<td>X:</td>
<td>0 = line supports 20 pps dialing.</td>
</tr>
<tr>
<td></td>
<td>1 = line supports 10 pps dialing only.</td>
</tr>
<tr>
<td>Y:</td>
<td>0 = extension network present (PBX).</td>
</tr>
<tr>
<td></td>
<td>1 = outside line (PSTN) connected directly.</td>
</tr>
<tr>
<td>Z:</td>
<td>0 = continuous dialtone.</td>
</tr>
<tr>
<td></td>
<td>1 = make-break dialtone.</td>
</tr>
<tr>
<td>n:</td>
<td>0–9 (number required for outside line if Y = 0).</td>
</tr>
</tbody>
</table>
Table 9. Extended AT& Command Set (Command Defaults in Bold)  (Continued)

<table>
<thead>
<tr>
<th>Command</th>
<th>Action</th>
</tr>
</thead>
<tbody>
<tr>
<td>&amp;X2</td>
<td>Same as &amp;X1, but Y result (PBX) is not tested.</td>
</tr>
<tr>
<td>*Y2A</td>
<td>Produce a constant answer tone (ITU-T) and return to command mode. The answer tone continues until the ATH command is received or the S7 timer expires.</td>
</tr>
</tbody>
</table>

Table 10. Extended AT% Command Set (Command Defaults in Bold)

<table>
<thead>
<tr>
<th>Command</th>
<th>Action</th>
</tr>
</thead>
<tbody>
<tr>
<td>%$</td>
<td>Display AT% command settings.</td>
</tr>
<tr>
<td>%B</td>
<td>Report blacklist. See also S42 register.</td>
</tr>
<tr>
<td>%Cn</td>
<td>Data compression</td>
</tr>
<tr>
<td>%C0</td>
<td>Disable V.42bis and MNP5 data compression</td>
</tr>
<tr>
<td>%C1</td>
<td>Enable V.42bis in transmit and receive paths. If MNP is selected \N2 or \N3, then %C1 enables MNP5 in transmit and receive paths.</td>
</tr>
<tr>
<td>%C2</td>
<td>Enable V.42bis in transmit path only</td>
</tr>
<tr>
<td>%C3</td>
<td>Enable V.42bis in receive path only</td>
</tr>
<tr>
<td>%On</td>
<td>Answer mode</td>
</tr>
<tr>
<td>%O1</td>
<td>Si2456/33/14 will auto-answer a call in answer mode</td>
</tr>
<tr>
<td>%O2</td>
<td>Si2456/33/14 will auto-answer a call in originate mode</td>
</tr>
<tr>
<td>%Vn</td>
<td>Automatic Line Status Detection. After the %V1 and %V2 commands are issued, the Si2456/33/14 will automatically check the telephone connection for whether or not a line is present. If a line is present, the Si2456/33/14 will automatically check if the line is already in use. Finally, the Si2456/33/14 will check line status both before going off-hook and again before dialing. %V1 uses the fixed method and %V2 uses the adaptive method. %V0 (default) disables this feature.</td>
</tr>
<tr>
<td>%V0</td>
<td>Disable automatic line-in-use detection.</td>
</tr>
</tbody>
</table>
Table 10. Extended AT% Command Set (Command Defaults in Bold) (Continued)

<table>
<thead>
<tr>
<th>Command</th>
<th>Action</th>
</tr>
</thead>
</table>
| %V1     | Automatic Line Status Detection - Fixed Method. **Description:** Before going off-hook with the ATD, ATO, or ATA commands, the Si2456/33/14 compares the line voltage (via LVCS) to registers NOLN (U83) and LIUS (U84):  
  **Loop Voltage** | **Action** |
  0 ≤ LVCS ≤ NOLN | Report “NO LINE” and remain on-hook.  
  NOLN ≤ LVCS ≤ LIUS | Report “LINE IN USE” and remain on-hook.  
  LIUS ≤ LCVS | Go off-hook and establish a modem connection.  

Once the call has begun, the off-hook intrusion algorithm (described in “Off-Hook Intrusion Detection” on page 19) operates normally. In addition, the Si2456/33/14 will report “NO LINE” if the telephone line is completely disconnected. If the HOI bit (U77, bit 11) is set, “LINE IN USE” is reported upon intrusion.

| %V2     | Automatic Line Status Detection - Adaptive Method. **Description:** Before going off-hook with the ATD, ATO, or ATA commands, the Si2456/33/14 compares the line voltage (via LVCS) to the NLIU (U85) register:  
  **Loop Voltage** | **Action** |
  0 ≤ LVCS ≤ (0.0625 x NLIU) | Report “NO LINE” and remain on-hook.  
  (0.0625 x NLIU) < LVCS ≤ (0.85 x NLIU) | Report “LINE IN USE” and remain on-hook.  
  (0.85 x NLIU) < LCVS | Go off-hook and establish a modem connection.  

The NLIU register is updated every 1 ms with the minimum non-zero value of LVCS in the last 30 ms. This allows the Si2456/33/14 to eliminate errors due to 50/60 Hz interference and also adapt to relatively slow change in the on-hook dc reference value on the telephone line. This algorithm does not allow any non-zero values for NLIU below 0x0007. The host may also initialize NLIU prior to issuing the %V2 command. Once the call has begun, the off-hook intrusion algorithm (described in “Off-Hook Intrusion Detection” on page 19) operates normally. In addition, the Si2456/33/14 will report “NO LINE” if the telephone line is completely disconnected. If the HOI (U77, bit 11) bit is set, “LINE IN USE” is reported upon intrusion.
<table>
<thead>
<tr>
<th>Command</th>
<th>Action</th>
</tr>
</thead>
<tbody>
<tr>
<td>$</td>
<td>Display AT\ command settings.</td>
</tr>
<tr>
<td>\Bn</td>
<td>Character length will be automatically set in autobaud mode.</td>
</tr>
<tr>
<td>\B0</td>
<td>6N1—six data bits, no parity, one stop bit, one start bit, eight bits total (N0 only)1</td>
</tr>
<tr>
<td>\B1</td>
<td>7N1—seven data bits, no parity, one stop bit, one start bit, nine bits total (N0 only)1</td>
</tr>
<tr>
<td>\B2</td>
<td>7P1—seven data bits, parity optioned by \P, one stop bit, one start bit, 10 bits total</td>
</tr>
<tr>
<td>\B3</td>
<td>8N1—eight data bits, no parity, one stop bit, one start bit, 10 bits total</td>
</tr>
<tr>
<td>\B5</td>
<td>8P1—eight data bits, parity optioned by \P, one stop bit, one start bit, 11 bits total (N0 only)1</td>
</tr>
<tr>
<td>\B6</td>
<td>8X1—eight data bits, one escape bit, one stop bit, one start bit, 11 bits total (enables ninth-bit escape mode)</td>
</tr>
<tr>
<td>\Nn</td>
<td>Asynchronous protocol</td>
</tr>
<tr>
<td>\N0</td>
<td>Wire mode (no error correction, no compression)</td>
</tr>
<tr>
<td>\N2</td>
<td>MNP reliable mode. The Si2456/33/14 attempts to connect with the MNP protocol. If unsuccessful, the call is dropped.</td>
</tr>
<tr>
<td>\N3</td>
<td>V.42 auto-reliable—The Si2456/33/14 attempts to connect with the V.42 protocol. If unsuccessful, the MNP protocol is attempted. If unsuccessful, wire mode is attempted.</td>
</tr>
<tr>
<td>\N4</td>
<td>V.42 (LAPM) reliable mode (or drop call)—Same as \N3 except that the Si2456/33/14 drops the call instead of connecting in MNP or wire mode.</td>
</tr>
<tr>
<td>\N5</td>
<td>V.42 and MNP reliable mode - The Si2456/33/14 attempts to connect with V.42. If unsuccessful, MNP is attempted. If MNP is unsuccessful, the call is dropped.</td>
</tr>
<tr>
<td>\Pn</td>
<td>Parity type will be automatically set in autobaud mode.</td>
</tr>
<tr>
<td>\P0</td>
<td>Even</td>
</tr>
<tr>
<td>\P1</td>
<td>Space1</td>
</tr>
<tr>
<td>\P2</td>
<td>Odd</td>
</tr>
<tr>
<td>\P3</td>
<td>Mark1</td>
</tr>
<tr>
<td>\Qn</td>
<td>Modem-to-DTE flow control</td>
</tr>
<tr>
<td>\Q0</td>
<td>Disable all flow control—Note that this may only be used if the DTE speed and the VF speed are guaranteed to match throughout the call.</td>
</tr>
<tr>
<td>\Q2</td>
<td>Use CTS only</td>
</tr>
</tbody>
</table>

Notes:
1. When in autobaud mode, \B0, \B1, and \P1 will not be detected automatically. The combination of \B2 and \P3 will be detected. This is compatible with seven data bits, no parity, two stop bits. Seven data bits, no parity, one stop bit may be forced by sending AT\T17\B1.  
2. The autobaud feature does not detect this rate.  
3. Default is \T16 if a pulldown is connected to pin 16; otherwise, the default is \T9.
### Table 11. Extended AT\ Command Set (Command Defaults in Bold) (Continued)

<table>
<thead>
<tr>
<th>Command</th>
<th>Action</th>
</tr>
</thead>
<tbody>
<tr>
<td>\Q3</td>
<td>Use RTS/CTS</td>
</tr>
<tr>
<td>\Q4</td>
<td>Use XON/XOFF flow control for modem-to-DTE interface. Does not enable modem-to-modem flow control.</td>
</tr>
<tr>
<td>\Tn</td>
<td>DTE rate - Change DTE rate. When changing rates, the result code &quot;OK&quot; is sent at the old DTE rate. All options except \T16 lock the DTE to the given rate, and subsequent commands must be sent at this rate. When \T16 is used (or at reset when pin 16 is pulled down), automatic baudrate detection is used for subsequent commands.</td>
</tr>
<tr>
<td>\T0</td>
<td>300 bps</td>
</tr>
<tr>
<td>\T1</td>
<td>600 bps</td>
</tr>
<tr>
<td>\T2</td>
<td>1200 bps</td>
</tr>
<tr>
<td>\T3</td>
<td>2400 bps</td>
</tr>
<tr>
<td>\T4</td>
<td>4800 bps</td>
</tr>
<tr>
<td>\T5</td>
<td>7200 bps</td>
</tr>
<tr>
<td>\T6</td>
<td>9600 bps</td>
</tr>
<tr>
<td>\T7</td>
<td>12.0 kbps²</td>
</tr>
<tr>
<td>\T8</td>
<td>14.4 kbps</td>
</tr>
<tr>
<td>\T9</td>
<td>19.2 kbps³</td>
</tr>
<tr>
<td>\T10</td>
<td>38.4 kbps</td>
</tr>
<tr>
<td>\T11</td>
<td>57.6 kbps</td>
</tr>
<tr>
<td>\T12</td>
<td>115.2 kbps</td>
</tr>
<tr>
<td>\T13</td>
<td>230.4 kbps</td>
</tr>
<tr>
<td>\T14</td>
<td>245.760 kbps²</td>
</tr>
<tr>
<td>\T15</td>
<td>307.200 kbps</td>
</tr>
<tr>
<td>\T16</td>
<td>Autobaud on²</td>
</tr>
<tr>
<td>\T17</td>
<td>Autobaud off; lock at current baud rate.</td>
</tr>
</tbody>
</table>

**Notes:**
1. When in autobaud mode, \B0, \B1, and \P1 will not be detected automatically. The combination of \B2 and \P3 will be detected. This is compatible with seven data bits, no parity, two stop bits. Seven data bits, no parity, one stop bit may be forced by sending AT\T17\B1.
2. The autobaud feature does not detect this rate.
3. Default is \T16 if a pulldown is connected to pin 16; otherwise, the default is \T9.
Table 11. Extended AT\Command Set (Command Defaults in Bold) (Continued)

<table>
<thead>
<tr>
<th>Command</th>
<th>Action</th>
</tr>
</thead>
<tbody>
<tr>
<td>\U</td>
<td>Serial mode—causes a low pulse (25 ms) on RI and DCD. INT to be the inverse of ESC. RTS to be the inverse of CTS. Parallel mode—causes a low pulse (25 ms) on INT. This command terminates with a RESET.</td>
</tr>
<tr>
<td>\Vn</td>
<td>Connect message type</td>
</tr>
<tr>
<td>\V0</td>
<td>Report connect message and protocol message</td>
</tr>
<tr>
<td>\V2</td>
<td>Report connect message only (exclude protocol message)</td>
</tr>
<tr>
<td>\V4</td>
<td>Report connect and protocol message with both upstream and downstream connect rates.</td>
</tr>
</tbody>
</table>

*Note:*

Notes:
1. When in autobaud mode, \B0, \B1, and \P1 will not be detected automatically. The combination of \B2 and \P3 will be detected. This is compatible with seven data bits, no parity, two stop bits. Seven data bits, no parity, one stop bit may be forced by sending AT\T17\B1.
2. The autobaud feature does not detect this rate.
3. Default is \T16 if a pulldown is connected to pin 16; otherwise, the default is \T9.
Table 12. Result Codes

<table>
<thead>
<tr>
<th>Numeric</th>
<th>Meaning</th>
<th>Verbal Response</th>
<th>X0</th>
<th>X1</th>
<th>X2</th>
<th>X3</th>
<th>X4</th>
<th>X5</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Command was successful</td>
<td>OK</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>1</td>
<td>Link established at 300 bps or higher</td>
<td>CONNECT</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>2</td>
<td>Incoming ring detected</td>
<td>RING</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>3</td>
<td>Link dropped</td>
<td>NO CARRIER</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>4</td>
<td>Command failed</td>
<td>ERROR</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>5</td>
<td>Link establish at 1200</td>
<td>CONNECT 1200</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>6</td>
<td>Dial tone not present</td>
<td>NO DIALTONE</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>Line busy</td>
<td>BUSY</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>Remote not answering</td>
<td>NO ANSWER</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>9</td>
<td>Ringback detected</td>
<td>RINGING</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>10</td>
<td>Link established at 2400</td>
<td>CONNECT 2400</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>11</td>
<td>Link established at 4800</td>
<td>CONNECT 4800</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>12</td>
<td>Link established at 9600</td>
<td>CONNECT 9600</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>14</td>
<td>Link established at 19200</td>
<td>CONNECT 19200</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>15</td>
<td>Link established at 7200</td>
<td>CONNECT 7200</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>16</td>
<td>Link established at 12000</td>
<td>CONNECT 12000</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>17</td>
<td>Link established at 14400</td>
<td>CONNECT 14400</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>18</td>
<td>Link established at 16800</td>
<td>CONNECT 16800</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>19</td>
<td>Link established at 21600</td>
<td>CONNECT 21600</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>20</td>
<td>Link established at 24000</td>
<td>CONNECT 24000</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>21</td>
<td>Link established at 26400</td>
<td>CONNECT 26400</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>22</td>
<td>Link established at 28800</td>
<td>CONNECT 28800</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>23</td>
<td>Link established at 31200</td>
<td>CONNECT 31200</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>24</td>
<td>Link established at 33600</td>
<td>CONNECT 33600</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>30</td>
<td>Caller ID mark detected</td>
<td>CIDM</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>75</td>
<td>Link established at 75</td>
<td>CONNECT 75</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>31</td>
<td>Hookswitch flash detected</td>
<td>FLASH</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>32</td>
<td>UK CID State Tone Alert Signal detected</td>
<td>STAS</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>33</td>
<td>Overcurrent condition</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>40</td>
<td>Blacklist is full</td>
<td>BLACKLIST FULL (enabled via S42 register)</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>41</td>
<td>Attempted number is blacklisted</td>
<td>BLACKLISTED (enabled via S42 register)</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

Notes:
1. Numeric result codes are of the format: Result code <CR>.
2. This message is only supported on the Si2456 and Si2433.
3. X is the only verbal response code that does not follow the <CR><LF>Result Code<CR><LF> standard. There is no leading <CR><LF>.
4. This message is only supported on the Si2456.
### Table 12. Result Codes (Continued)

<table>
<thead>
<tr>
<th>Numeric</th>
<th>Meaning</th>
<th>Verbal Response</th>
<th>X0</th>
<th>X1</th>
<th>X2</th>
<th>X3</th>
<th>X4</th>
<th>X5</th>
</tr>
</thead>
<tbody>
<tr>
<td>42</td>
<td>No phone line present</td>
<td>NO LINE (enabled via %Vn commands)</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>43</td>
<td>Telephone line is in use</td>
<td>LINE IN USE (enabled via %Vn commands)</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>44</td>
<td>A polarity reversal was detected</td>
<td>POLARITY REVERSAL (enabled via G modifier)</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>45</td>
<td>A polarity reversal was NOT detected</td>
<td>NO POLARITY REVERSAL (enabled via G modifier)</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>52</td>
<td>Link established at 56000</td>
<td>CONNECT 56000⁴</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>60</td>
<td>Link established at 32000</td>
<td>CONNECT 32000⁴</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>61</td>
<td>Link established at 48000</td>
<td>CONNECT 48000⁴</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>63</td>
<td>Link established at 28000</td>
<td>CONNECT 28000⁴</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>64</td>
<td>Link established at 29333</td>
<td>CONNECT 29333⁴</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>65</td>
<td>Link established at 30666</td>
<td>CONNECT 30666⁴</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>66</td>
<td>Link established at 33333</td>
<td>CONNECT 33333⁴</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>67</td>
<td>Link established at 34666</td>
<td>CONNECT 34666⁴</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>68</td>
<td>Link established at 36000</td>
<td>CONNECT 36000⁴</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>69</td>
<td>Link established at 37333</td>
<td>CONNECT 37333⁴</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>70</td>
<td>No protocol</td>
<td>PROTOCOL: NONE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>77</td>
<td>V.42 protocol</td>
<td>PROTOCOL: V42</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>79</td>
<td>V.42bis protocol</td>
<td>PROTOCOL: V42bis</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>80</td>
<td>MNP2 protocol</td>
<td>PROTOCOL: ALTERNATE, + CLASS 2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>81</td>
<td>MNP3 protocol</td>
<td>PROTOCOL: ALTERNATE, + CLASS 3</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>82</td>
<td>MNP4 protocol</td>
<td>PROTOCOL: ALTERNATE, + CLASS 4</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>83</td>
<td>MNP5 protocol</td>
<td>PROTOCOL: ALTERNATE, + CLASS 5</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>90</td>
<td>Link established at 38666</td>
<td>CONNECT 38666⁴</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>91</td>
<td>Link established at 40000</td>
<td>CONNECT 40000⁴</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>92</td>
<td>Link established at 41333</td>
<td>CONNECT 41333⁴</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>93</td>
<td>Link established at 42666</td>
<td>CONNECT 42666⁴</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>94</td>
<td>Link established at 44000</td>
<td>CONNECT 44000⁴</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>95</td>
<td>Link established at 45333</td>
<td>CONNECT 45333⁴</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>96</td>
<td>Link established at 46666</td>
<td>CONNECT 46666⁴</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>97</td>
<td>Link established at 49333</td>
<td>CONNECT 49333⁴</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

**Notes:**

1. Numeric result codes are of the format: Result code <CR>.
2. This message is only supported on the Si2456 and Si2433.
3. X is the only verbal response code that does not follow the <CR><LF>Result Code<CR><LF> standard. There is no leading <CR><LF>.
4. This message is only supported on the Si2456.
Table 12. Result Codes (Continued)

<table>
<thead>
<tr>
<th>Numeric</th>
<th>Meaning</th>
<th>Verbal Response</th>
<th>X0</th>
<th>X1</th>
<th>X2</th>
<th>X3</th>
<th>X4</th>
<th>X5</th>
</tr>
</thead>
<tbody>
<tr>
<td>98</td>
<td>Link established at 50666</td>
<td>CONNECT 50666$^4$</td>
<td>X</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>99</td>
<td>Link established at 52000</td>
<td>CONNECT 52000$^4$</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>100</td>
<td>Link established at 53333</td>
<td>CONNECT 53333$^4$</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td></td>
<td></td>
</tr>
<tr>
<td>101</td>
<td>Link established at 54666</td>
<td>CONNECT 54666$^4$</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>102</td>
<td>DTMF dial attempted on a pulse dial only line</td>
<td>UNOBTAINABLE NUMBER</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

Notes:
1. Numeric result codes are of the format: Result code <CR>.
2. This message is only supported on the Si2456 and Si2433.
3. X is the only verbal response code that does not follow the <CR><LF>Result Code<CR><LF> standard. There is no leading <CR><LF>.
4. This message is only supported on the Si2456.

The connect messages shown in Table 12 are sent when link negotiation is complete.
**S-Registers**

The S command allows reading (Sn?) or writing (Sn=x) the S-registers. The S-registers store values for functions that typically are rarely changed, such as timers or counters, and the ASCII values of control characters, such as carriage return. Table 13 summarizes the S-register set.

**Table 13. S-Register Descriptions**

<table>
<thead>
<tr>
<th>S-Register (Decimal)</th>
<th>Definition</th>
<th>Default (Decimal)</th>
<th>Range</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Automatic answer—Number of rings the Si2456/33/14 must detect before answering a call. 0 disables auto answer.</td>
<td>0</td>
<td>0–255</td>
<td>Rings</td>
</tr>
<tr>
<td>1</td>
<td>Ring counter.</td>
<td>0</td>
<td>0–255</td>
<td>Rings</td>
</tr>
<tr>
<td>2</td>
<td>ESC code character.</td>
<td>43 (+)</td>
<td>0–255</td>
<td>ASCII</td>
</tr>
<tr>
<td>3</td>
<td>Carriage return character.</td>
<td>13 (CR)</td>
<td>0–255</td>
<td>ASCII</td>
</tr>
<tr>
<td>4</td>
<td>Linefeed character.</td>
<td>10 (LF)</td>
<td>0–255</td>
<td>ASCII</td>
</tr>
<tr>
<td>5</td>
<td>Backspace character.</td>
<td>08 (BS)</td>
<td>0–255</td>
<td>ASCII</td>
</tr>
<tr>
<td>6</td>
<td>Dial tone wait timer—Number of seconds the Si2456/33/14 waits before blind dialing. Only applicable if blind dialing is enabled (X0, X1, X3).</td>
<td>02</td>
<td>0–255</td>
<td>seconds</td>
</tr>
<tr>
<td>7</td>
<td>Carrier wait timer—Number of seconds the Si2456/33/14 waits for carrier before timing out. This register also sets the number of seconds the modem waits for ringback when originating a call before hanging up. This register also sets the number of seconds the answer tone will continue while using the AT*Y2A command.</td>
<td>80</td>
<td>0–255</td>
<td>seconds</td>
</tr>
<tr>
<td>8</td>
<td>Dial pause timer for , and &lt; dial command modifiers.</td>
<td>02</td>
<td>0–255</td>
<td>seconds</td>
</tr>
<tr>
<td>9</td>
<td>Carrier presence timer—Time after a loss of carrier that a carrier must be detected before reactivating DCD. S9 is referred to as “carrier loss debounce time.”</td>
<td>06</td>
<td>1–255</td>
<td>0.1 seconds</td>
</tr>
<tr>
<td>10</td>
<td>Carrier loss timer—Time the carrier must be lost before the Si2456/33/14 disconnects. Setting 255 disables disconnect entirely. If S10 is less than S9, even a momentary loss of carrier causes a disconnect.</td>
<td>14</td>
<td>1–255</td>
<td>0.1 seconds</td>
</tr>
<tr>
<td>12</td>
<td>Escape code guard timer—Minimum guard time required before and after “+++” for the Si2456/33/14 to recognize a valid escape sequence.</td>
<td>50</td>
<td>1–255</td>
<td>0.02 seconds</td>
</tr>
<tr>
<td>14</td>
<td>Wait for dial tone delay value (in relation to the W dial modifier). Starts when “W” is executed in the dial string.</td>
<td>12</td>
<td>0–255</td>
<td>seconds</td>
</tr>
</tbody>
</table>
### Table 13. S-Register Descriptions (Continued)

<table>
<thead>
<tr>
<th>S-Register (Decimal)</th>
<th>Function</th>
<th>Default (Decimal)</th>
<th>Range</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>24</td>
<td>Sleep Inactivity Time—Sets the time that the modem operates in normal power mode with no activity on the serial port, parallel port, or telephone line before entering low-power sleep mode. This feature is disabled if the timer is set to 0.</td>
<td>0</td>
<td>0–255</td>
<td>seconds</td>
</tr>
<tr>
<td>30</td>
<td>Disconnect Activity Timer—Sets the length of time that the modem stays online before disconnecting with no activity on the serial port, parallel port, or telephone line (Ring, hookswitch flash, or caller ID). This feature is disabled if set to 0.</td>
<td>0</td>
<td>0–255</td>
<td>minutes</td>
</tr>
<tr>
<td>38</td>
<td>Hang Up Delay Time—Maximum delay between receipt of ATH0 command and hang up. If time out occurs before all data can be sent, the NO CARRIER (3) result code is sent (operates in V.42 mode only). “OK” response is sent if all data is transmitted before timeout. S38 = 255 disables timeout and modem disconnects only if data is successfully sent or carrier is lost.</td>
<td>20</td>
<td>0–255</td>
<td>seconds</td>
</tr>
<tr>
<td>40</td>
<td>Data Pattern - Data pattern generated during &amp;T4 and &amp;T5 transmit tests. 0 – All spaces (0s) 1 – All marks (1s) 2 – Random data</td>
<td>0</td>
<td>0–2</td>
<td>—</td>
</tr>
<tr>
<td>41</td>
<td>V.34 symbol rate - Symbol rate for V.34 when using the &amp;T4 and &amp;T5 commands. 0 – 2400 symbols/second 1 – 2743 symbols/second 2 – 2800 symbols/second 3 – 3000 symbols/second 4 – 3200 symbols/second 5 – 3429 symbols/second A valid combination of symbol rate (S41) and data rate (&amp;G) must be selected.</td>
<td>0</td>
<td>0–5</td>
<td>—</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Symbol Rate</th>
<th>Allowable Data Rates</th>
</tr>
</thead>
<tbody>
<tr>
<td>2400</td>
<td>2400 – 21600</td>
</tr>
<tr>
<td>2743</td>
<td>4800 – 26400</td>
</tr>
<tr>
<td>2800</td>
<td>4800 – 26400</td>
</tr>
<tr>
<td>3000</td>
<td>4800 – 28800</td>
</tr>
<tr>
<td>3200</td>
<td>4800 – 31200</td>
</tr>
<tr>
<td>3429</td>
<td>4800 – 33600</td>
</tr>
</tbody>
</table>
### Table 13. S-Register Descriptions (Continued)

<table>
<thead>
<tr>
<th>S-Register (Decimal)</th>
<th>Function</th>
<th>Default (Decimal)</th>
<th>Range</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>42</td>
<td>Blacklisting - The Si2456/33/14 will not dial the same number more than three times in three minutes. An attempt to dial a fourth time within three minutes will result in a “BLACKLISTED” result code. If the blacklist memory is full, any dial to a new number will result in a “BLACKLIST FULL” result code. Numbers are added to the blacklist only if the modem connection fails. The %B command will list the numbers on the blacklists.</td>
<td>0 (disabled)</td>
<td>0–1</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>0 – disabled</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 – enabled</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>43</td>
<td>Dial attempts to blacklist</td>
<td></td>
<td>0–4</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>When blacklisting is enabled with S42, this value controls the number of dial attempts that will result in a number being blacklisted.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>44</td>
<td>Blacklist Timer</td>
<td></td>
<td>0–255</td>
<td>seconds</td>
</tr>
<tr>
<td></td>
<td>Period during which blacklisting is active</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>50</td>
<td>Minimum on-hook time – Modem will remain on-hook for S50 seconds. Any attempt to go off-hook will be delayed until this timer expires.</td>
<td>3</td>
<td>0–255</td>
<td>seconds</td>
</tr>
<tr>
<td>51</td>
<td>Number to start checking for an outside line on a PBX.</td>
<td>1</td>
<td>0–9</td>
<td>—</td>
</tr>
</tbody>
</table>
User-Access Registers (U-Registers)

The :U AT command is used to write these 16-bit U-registers, and the :R command is used to read them. U-registers are identified by a hexadecimal (hex) address.

Table 14. U-Register Descriptions

<table>
<thead>
<tr>
<th>Register</th>
<th>Name</th>
<th>Description</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>U00</td>
<td>DT1A0</td>
<td>DT1 registers set the coefficients for stage 1 of the Dial Tone Detect filter. Default is for FCC countries. See “AN70: Si2456/Si2433/Si2414/Si2403 Modem Designer’s Guide” for other country settings.</td>
<td>0x0800</td>
</tr>
<tr>
<td>U01</td>
<td>DT1B1</td>
<td></td>
<td>0x0000</td>
</tr>
<tr>
<td>U02</td>
<td>DT1B2</td>
<td></td>
<td>0x0000</td>
</tr>
<tr>
<td>U03</td>
<td>DT1A2</td>
<td></td>
<td>0x0000</td>
</tr>
<tr>
<td>U04</td>
<td>DT1A1</td>
<td></td>
<td>0x0000</td>
</tr>
<tr>
<td>U05</td>
<td>DT2A0</td>
<td>Dial tone detect filters stage 2 biquad coefficients.</td>
<td>0x00A0</td>
</tr>
<tr>
<td>U06</td>
<td>DT2B1</td>
<td></td>
<td>0x6EF1</td>
</tr>
<tr>
<td>U07</td>
<td>DT2B2</td>
<td></td>
<td>0xC4F4</td>
</tr>
<tr>
<td>U08</td>
<td>DT2A2</td>
<td></td>
<td>0xC000</td>
</tr>
<tr>
<td>U09</td>
<td>DT2A1</td>
<td></td>
<td>0x0000</td>
</tr>
<tr>
<td>U0A</td>
<td>DT3A0</td>
<td>Dial tone detect filters stage 3 biquad coefficients.</td>
<td>0x00A0</td>
</tr>
<tr>
<td>U0B</td>
<td>DT3B1</td>
<td></td>
<td>0x78B0</td>
</tr>
<tr>
<td>U0C</td>
<td>DT3B2</td>
<td></td>
<td>0xC305</td>
</tr>
<tr>
<td>U0D</td>
<td>DT3A2</td>
<td></td>
<td>0x4000</td>
</tr>
<tr>
<td>U0E</td>
<td>DT3A1</td>
<td></td>
<td>0xB50A</td>
</tr>
<tr>
<td>U0F</td>
<td>DT4A0</td>
<td>Dial tone detect filters stage 4 biquad coefficients.</td>
<td>0x0400</td>
</tr>
<tr>
<td>U10</td>
<td>DT4B1</td>
<td></td>
<td>0x70D2</td>
</tr>
<tr>
<td>U11</td>
<td>DT4B2</td>
<td></td>
<td>0xC830</td>
</tr>
<tr>
<td>U12</td>
<td>DT4A2</td>
<td></td>
<td>0x4000</td>
</tr>
<tr>
<td>U13</td>
<td>DT4A1</td>
<td></td>
<td>0x80E2</td>
</tr>
<tr>
<td>U14</td>
<td>DTK</td>
<td>Dial tone detect filter output scaler.</td>
<td>0x009</td>
</tr>
<tr>
<td>U15</td>
<td>DTON</td>
<td>Dial tone detect ON threshold.</td>
<td>0x00A0</td>
</tr>
<tr>
<td>U16</td>
<td>DTOF</td>
<td>Dial tone detect OFF threshold.</td>
<td>0x0070</td>
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</table>
### Table 14. U-Register Descriptions (Continued)

<table>
<thead>
<tr>
<th>Register</th>
<th>Name</th>
<th>Description</th>
<th>Default</th>
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</thead>
<tbody>
<tr>
<td>U17</td>
<td>BT1A0</td>
<td>BT1 registers set the coefficients for stage 1 of the Busy Tone Detect filter. Default is for FCC countries. See AN70 for other country settings.</td>
<td>0x0800</td>
</tr>
<tr>
<td>U18</td>
<td>BT1B1</td>
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<td>0x0000</td>
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<td>U19</td>
<td>BT1B2</td>
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<td>0x0000</td>
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<td>U1A</td>
<td>BT1A2</td>
<td></td>
<td>0x0000</td>
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<tr>
<td>U1B</td>
<td>BT1A1</td>
<td></td>
<td>0x0000</td>
</tr>
<tr>
<td>U1C</td>
<td>BT2A0</td>
<td>Busy tone detect filter stage 2 biquad coefficients.</td>
<td>0x00A0</td>
</tr>
<tr>
<td>U1D</td>
<td>BT2B1</td>
<td></td>
<td>0x6EF1</td>
</tr>
<tr>
<td>U1E</td>
<td>BT2B2</td>
<td></td>
<td>0xC4F4</td>
</tr>
<tr>
<td>U1F</td>
<td>BT2A2</td>
<td></td>
<td>0xC000</td>
</tr>
<tr>
<td>U20</td>
<td>BT2A1</td>
<td></td>
<td>0x0000</td>
</tr>
<tr>
<td>U21</td>
<td>BT3A0</td>
<td>Busy tone detect filter stage 3 biquad coefficients.</td>
<td>0x00A0</td>
</tr>
<tr>
<td>U22</td>
<td>BT3B1</td>
<td></td>
<td>0x78B0</td>
</tr>
<tr>
<td>U23</td>
<td>BT3B2</td>
<td></td>
<td>0xC305</td>
</tr>
<tr>
<td>U24</td>
<td>BT3A2</td>
<td></td>
<td>0x4000</td>
</tr>
<tr>
<td>U25</td>
<td>BT3A1</td>
<td></td>
<td>0xB50A</td>
</tr>
<tr>
<td>U26</td>
<td>BT4A0</td>
<td>Busy tone detect filter stage 4 biquad coefficients.</td>
<td>0x0400</td>
</tr>
<tr>
<td>U27</td>
<td>BT4B1</td>
<td></td>
<td>0x70D2</td>
</tr>
<tr>
<td>U28</td>
<td>BT4B2</td>
<td></td>
<td>0xC830</td>
</tr>
<tr>
<td>U29</td>
<td>BT4A2</td>
<td></td>
<td>0x4000</td>
</tr>
<tr>
<td>U2A</td>
<td>BT4A1</td>
<td></td>
<td>0x80E2</td>
</tr>
<tr>
<td>U2B</td>
<td>BTK</td>
<td>Busy tone detect filter output scaler.</td>
<td>0x0009</td>
</tr>
<tr>
<td>U2C</td>
<td>BTON</td>
<td>Busy tone detect ON threshold.</td>
<td>0x00A0</td>
</tr>
<tr>
<td>U2D</td>
<td>BTOF</td>
<td>Busy tone detect OFF threshold.</td>
<td>0x0070</td>
</tr>
<tr>
<td>U2E</td>
<td>BMTT</td>
<td>Busy cadence minimum total time in seconds multiplied by 7200.</td>
<td>0x0870</td>
</tr>
<tr>
<td>U2F</td>
<td>BDLT</td>
<td>Busy cadence delta in seconds multiplied by 7200.</td>
<td>0x25F8</td>
</tr>
<tr>
<td>U30</td>
<td>BMOT</td>
<td>Busy cadence minimum on time in seconds multiplied by 7200.</td>
<td>0x0438</td>
</tr>
<tr>
<td>U31</td>
<td>RMTT</td>
<td>Ringback cadence minimum total time in seconds multiplied by 7200.</td>
<td>0x4650</td>
</tr>
<tr>
<td>U32</td>
<td>RDLT</td>
<td>Ringback cadence delta in seconds multiplied by 7200.</td>
<td>0xEF10</td>
</tr>
<tr>
<td>U33</td>
<td>RMOT</td>
<td>Ringback cadence minimum on time in seconds multiplied by 7200.</td>
<td>0x1200</td>
</tr>
<tr>
<td>U34</td>
<td>DTWD</td>
<td>Window to look for dialtone in seconds multiplied by 1000.</td>
<td>0x1B58</td>
</tr>
</tbody>
</table>
Table 14. U-Register Descriptions (Continued)

<table>
<thead>
<tr>
<th>Register</th>
<th>Name</th>
<th>Description</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>U35</td>
<td>DMOT</td>
<td>Minimum dialtone on time in seconds multiplied by 7200.</td>
<td>0x2D00</td>
</tr>
<tr>
<td>U37</td>
<td>PD0</td>
<td>Number of pulses to dial 0.</td>
<td>0x000A</td>
</tr>
<tr>
<td>U38</td>
<td>PD1</td>
<td>Number of pulses to dial 1.</td>
<td>0x0001</td>
</tr>
<tr>
<td>U39</td>
<td>PD2</td>
<td>Number of pulses to dial 2.</td>
<td>0x0002</td>
</tr>
<tr>
<td>U3A</td>
<td>PD3</td>
<td>Number of pulses to dial 3.</td>
<td>0x0003</td>
</tr>
<tr>
<td>U3B</td>
<td>PD4</td>
<td>Number of pulses to dial 4.</td>
<td>0x0004</td>
</tr>
<tr>
<td>U3C</td>
<td>PD5</td>
<td>Number of pulses to dial 5.</td>
<td>0x0005</td>
</tr>
<tr>
<td>U3D</td>
<td>PD6</td>
<td>Number of pulses to dial 6.</td>
<td>0x0006</td>
</tr>
<tr>
<td>U3E</td>
<td>PD7</td>
<td>Number of pulses to dial 7.</td>
<td>0x0007</td>
</tr>
<tr>
<td>U3F</td>
<td>PD8</td>
<td>Number of pulses to dial 8.</td>
<td>0x0008</td>
</tr>
<tr>
<td>U40</td>
<td>PD9</td>
<td>Number of pulses to dial 9.</td>
<td>0x0009</td>
</tr>
<tr>
<td>U42</td>
<td>PDBT</td>
<td>Pulse dial break time (ms units).</td>
<td>0x003D</td>
</tr>
<tr>
<td>U43</td>
<td>PDMT</td>
<td>Pulse dial make time (ms units).</td>
<td>0x0027</td>
</tr>
<tr>
<td>U45</td>
<td>PDIT</td>
<td>Pulse dial interdigit time (ms units).</td>
<td>0x0320</td>
</tr>
<tr>
<td>U46</td>
<td>DTPL</td>
<td>DTMF power level—16-bit format is 0x0(H)(L)0 where H is the ((-)dBm level of the high-frequency DTMF tone, and L is the ((-)dBm level of the low-frequency DTMF tone. Note that twist may be specified here.</td>
<td>0x09B0</td>
</tr>
<tr>
<td>U47</td>
<td>DTNT</td>
<td>DTMF on time (ms units).</td>
<td>0x0064</td>
</tr>
<tr>
<td>U48</td>
<td>DTFT</td>
<td>DTMF off time (ms units).</td>
<td>0x0064</td>
</tr>
<tr>
<td>U49</td>
<td>RGFH</td>
<td>Ring frequency high—Maximum frequency ring to be considered a valid ring.</td>
<td>0x0022</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RGFH = 2400/(maximum ring frequency).</td>
<td></td>
</tr>
<tr>
<td>U4A</td>
<td>RGFD</td>
<td>Ring delta</td>
<td>0x007A</td>
</tr>
</tbody>
</table>
|          |          | \[
|          |          | RGFD \leq 2400 \text{ Hz} \times \left(\frac{1}{\text{min ring freq (Hz)}} - \frac{1}{\text{max ring freq (Hz)}}\right)\] |          |
| U4B      | RGMN     | Ring cadence minimum ON time in seconds multiplied by 2400.                 | 0x0258   |
| U4C      | RGNX     | Ring cadence maximum total time in seconds multiplied by 2400.              | 0x6720   |
| U4D      | MOD1     | This is a bit-mapped register.                                             | 0x0000   |
| U4E      | PRDD     | Pre-dial delay-time after ATD command that modem waits to dial (ms units).  | 0x0000   |
|          |          | The Si2456/33/14 stays on-hook during this time.                           |          |
| U4F      | FHT      | Flash Hook Time. Time corresponding with “I” or “&” dial modifier that the | 0x01F4   |
|          |          | Si2456/33/14 goes on-hook during a flash hook (ms units).                   |          |
| U50      | LCDN     | Loop current debounce on time (ms units).                                  | 0x015E   |
### Table 14. U-Register Descriptions (Continued)

<table>
<thead>
<tr>
<th>Register</th>
<th>Name</th>
<th>Description</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>U51</td>
<td>LCDF</td>
<td>Loop current debounce off time (ms units).</td>
<td>0x00C8</td>
</tr>
<tr>
<td>U52</td>
<td>XMTL</td>
<td>Transmit level (1 dB units)—Sets the modem data pump transmitter level.</td>
<td>0x0000</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Default level of 0 corresponds to −9.85 dBm.</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Transmit level = −(9.85 + XMTL) dBm. Range = −9.85 to −48.</td>
<td></td>
</tr>
<tr>
<td>U53</td>
<td>MOD2</td>
<td>This is a bit-mapped register.</td>
<td>0x0000</td>
</tr>
<tr>
<td>U54</td>
<td>DAAC1</td>
<td>This is a bit-mapped register.</td>
<td>0x0804</td>
</tr>
<tr>
<td>U55</td>
<td>DAAC4</td>
<td>This is a bit-mapped register.</td>
<td>0x00E0</td>
</tr>
<tr>
<td>U56</td>
<td>DAAC5</td>
<td>This is a bit-mapped register.</td>
<td>0x0040</td>
</tr>
<tr>
<td>U57</td>
<td>ITC1</td>
<td>This is a bit-mapped register.</td>
<td>0x0008</td>
</tr>
<tr>
<td>U58</td>
<td>ITC2</td>
<td>This is a bit-mapped register.</td>
<td>0x0000</td>
</tr>
<tr>
<td>U59</td>
<td>ITC3</td>
<td>This is a bit-mapped register.</td>
<td>0x0006</td>
</tr>
<tr>
<td>U60</td>
<td>ITC4</td>
<td>This is a bit-mapped register.</td>
<td>n/a</td>
</tr>
<tr>
<td>U61</td>
<td>V29E</td>
<td>V29 EPOS handshake enable. (See AN70.)</td>
<td>0x0000</td>
</tr>
<tr>
<td>U62</td>
<td>CK1</td>
<td>This is a bit-mapped register.</td>
<td>0x1F20</td>
</tr>
<tr>
<td>U63</td>
<td>PTMR</td>
<td>This is a bit-mapped register.</td>
<td>0x00FF</td>
</tr>
<tr>
<td>U64</td>
<td>IO0</td>
<td>This is a bit-mapped register.</td>
<td>0x2700</td>
</tr>
<tr>
<td>U65</td>
<td>GEN1</td>
<td>This is a bit-mapped register.</td>
<td>0x3240</td>
</tr>
<tr>
<td>U66</td>
<td>GEN2</td>
<td>This is a bit-mapped register.</td>
<td>0x401E</td>
</tr>
<tr>
<td>U67</td>
<td>GEN3</td>
<td>This is a bit-mapped register.</td>
<td>0x0000</td>
</tr>
<tr>
<td>U68</td>
<td>GEN4</td>
<td>This is a bit-mapped register.</td>
<td>0x0000</td>
</tr>
<tr>
<td>U69</td>
<td>GENA</td>
<td>This is a bit-mapped register.</td>
<td>0x0000</td>
</tr>
<tr>
<td>U70</td>
<td>GENC</td>
<td>This is a bit-mapped register.</td>
<td>0x0000</td>
</tr>
<tr>
<td>U71</td>
<td>GEND</td>
<td>This is a bit-mapped register.</td>
<td>0x0000</td>
</tr>
<tr>
<td>U72</td>
<td>NOLN</td>
<td>No-Line threshold. If %V1 is set, NOLN sets the threshold for determination of line present vs. line not present.</td>
<td>0x0001</td>
</tr>
<tr>
<td>U73</td>
<td>LIUS</td>
<td>Line-in-use threshold. If %V1 is set, LIUS sets the threshold for determination of line in use vs. line not in use.</td>
<td>0x0007</td>
</tr>
<tr>
<td>U74</td>
<td>NLIU</td>
<td>Line-in-use/No line threshold. If %V2 is set, NLIU sets the threshold reference for the adaptive algorithm (see %V2).</td>
<td>0x0000</td>
</tr>
<tr>
<td>U75</td>
<td>V9AGG</td>
<td>V.90 rate reduction in 1333 bps units.</td>
<td>0x0000</td>
</tr>
</tbody>
</table>
Table 15. Bit-Mapped U-Register Summary

<table>
<thead>
<tr>
<th>Reg.</th>
<th>Name</th>
<th>Bit 15</th>
<th>Bit 14</th>
<th>Bit 13</th>
<th>Bit 12</th>
<th>Bit 11</th>
<th>Bit 10</th>
<th>Bit 9</th>
<th>Bit 8</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
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<tbody>
<tr>
<td>U4D</td>
<td>MOD1</td>
<td>TOCT</td>
<td>NHFP</td>
<td>NHFD</td>
<td>CLPD</td>
<td>FTP</td>
<td>SPDM</td>
<td>GT18</td>
<td>GT55</td>
<td>CTE</td>
<td>LLC</td>
<td>LCN</td>
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<td>U53</td>
<td>MOD2</td>
<td>REV</td>
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<tr>
<td>U62</td>
<td>DAAC1</td>
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<tr>
<td>U65</td>
<td>DAAC4</td>
<td>PWM</td>
<td>PWMG</td>
<td>PDN</td>
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<tr>
<td>U67</td>
<td>ITC1</td>
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<td>U7A</td>
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</tbody>
</table>
## Si2456/Si2433/Si2414

### Bit-Mapped U-Register Detail (defaults in bold)

#### U4D MOD1

<table>
<thead>
<tr>
<th>Bit</th>
<th>D15</th>
<th>D14</th>
<th>D13</th>
<th>D12</th>
<th>D11</th>
<th>D10</th>
<th>D9</th>
<th>D8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Name</td>
<td>TOCT</td>
<td>NHFP</td>
<td>NHFD</td>
<td>CLPD</td>
<td>FTP</td>
<td>SPDM</td>
<td>GT18</td>
<td>GT55</td>
<td>CTE</td>
<td>LLC</td>
<td>LCN</td>
<td></td>
<td></td>
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</tr>
<tr>
<td>Type</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
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<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td></td>
</tr>
</tbody>
</table>

Reset settings = 0x0000

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>Reserved</td>
<td>Read returns zero.</td>
</tr>
<tr>
<td>14</td>
<td>TOCT</td>
<td>Turn Off Calling Tone.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 = Disable. 1 = Enable.</td>
</tr>
<tr>
<td>13</td>
<td>Reserved</td>
<td>Read returns zero.</td>
</tr>
<tr>
<td>12</td>
<td>NHFP</td>
<td>No Hook Flash Pulse.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 = Disable. 1 = Enable.</td>
</tr>
<tr>
<td>11</td>
<td>NHFD</td>
<td>No Hook Flash Dial.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 = Disable. 1 = Enable.</td>
</tr>
<tr>
<td>10</td>
<td>CLPD</td>
<td>Check Loop Current Before Dialing.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 = Ignore. 1 = Check.</td>
</tr>
<tr>
<td>9</td>
<td>Reserved</td>
<td>Read returns zero.</td>
</tr>
<tr>
<td>8</td>
<td>FTP</td>
<td>Force Tone or Pulse.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 = Disable. 1 = Enable.</td>
</tr>
<tr>
<td>7</td>
<td>SPDM</td>
<td>Skip Pulse Dial Modifier.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 = No. 1 = Yes.</td>
</tr>
<tr>
<td>6</td>
<td>Reserved</td>
<td>Read returns zero.</td>
</tr>
<tr>
<td>5</td>
<td>GT18</td>
<td>1800 Hz Guard Tone Enable.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 = Disable. 1 = Enable.</td>
</tr>
<tr>
<td>4</td>
<td>GT55</td>
<td>550 Hz Guard Tone Enable.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 = Disable. 1 = Enable.</td>
</tr>
<tr>
<td>3</td>
<td>CTE</td>
<td>Calling Tone Enable.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 = Disable. 1 = Enable.</td>
</tr>
<tr>
<td>2</td>
<td>Reserved</td>
<td>Read returns zero.</td>
</tr>
</tbody>
</table>
### Si2456/Si2433/Si2414

#### Low Loop Current Detect

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>LLC</td>
<td>Low Loop Current Detect (required for CTR21). 0 = Disabled. 1 = Enabled.</td>
</tr>
<tr>
<td>0</td>
<td>LCN</td>
<td>Loop Current Needed. 0 = No. 1 = Yes.</td>
</tr>
</tbody>
</table>

#### U53 MOD2

<table>
<thead>
<tr>
<th>Bit</th>
<th>D15</th>
<th>D14</th>
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<th>D12</th>
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<th>D9</th>
<th>D8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
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</thead>
<tbody>
<tr>
<td>Name</td>
<td>REV</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Type</td>
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</table>

Reset settings = 0x0000

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>REV</td>
<td>V.23 Reversing. 0 = Disable. 1 = Enable.</td>
</tr>
<tr>
<td>14:0</td>
<td>Reserved</td>
<td>Read returns zero.</td>
</tr>
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</table>

#### U62 DAAC1

<table>
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<tr>
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<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
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</thead>
<tbody>
<tr>
<td>Name</td>
<td>FOH</td>
<td>DL</td>
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</table>

Reset settings = 0x0804

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:12</td>
<td>Reserved</td>
<td>Must be set to 0.</td>
</tr>
<tr>
<td>11</td>
<td>Reserved</td>
<td>Must be set to 1.</td>
</tr>
<tr>
<td>10:3</td>
<td>Reserved</td>
<td>Must be set to 0.</td>
</tr>
<tr>
<td>2</td>
<td>FOH</td>
<td>Fast Off-Hook. 0 = Automatic Calibration Time set to 426 ms 1 = Automatic Calibration Time set to 106 ms</td>
</tr>
<tr>
<td>1</td>
<td>DL</td>
<td>Isolation Digital Loopback (see the AT&amp;T commands). 0 = Loopback occurs beyond the ISOcap interface, out to and including the analog hybrid circuit. 1 = Enables digital loopback mode across isolation barrier only.</td>
</tr>
<tr>
<td>0</td>
<td>Reserved</td>
<td>Must be set to 0.</td>
</tr>
</tbody>
</table>
## Si2456/Si2433/Si2414

### U65 DAAC4

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<tr>
<th>Bit</th>
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<th>D12</th>
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<th>D8</th>
<th>D7</th>
<th>D6</th>
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<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
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<tbody>
<tr>
<td>Name</td>
<td>PWM</td>
<td>PWMG</td>
<td>PDN</td>
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<td>R/W</td>
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Reset settings = 0x00E0

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
</table>
| 15  | PWM      | **PWM Mode.**
|     |          | 0 = Normal. Classic PWM output waveform.                                   |
|     |          | 1 = Scrambled mode. Low-distortion mode if used with output circuit shown in “AN70: Si2456/Si2433/Si2414/Si2403 Modem Designer’s Guide”. |
| 14  | PWMG     | **PWM Gain.**
|     |          | 0 = No gain.                                                               |
|     |          | 1 = 6 dB gain applied to AOUT.                                             |
| 13  | PDN      | **Powerdown.**
|     |          | Completely powerdown the Si2456/33/14 and Si3015. Once set to 1, the Si2456/33/14 must be reset to power on. |
|     |          | 0 = Normal.                                                               |
|     |          | 1 = Powerdown.                                                            |
| 12:8| Reserved | Read returns zero.                                                       |
| 7:5 | Reserved | Must not change in a read-modify-write.                                   |
| 4   | PDL*     | **Powerdown Line-Side Chip.**
|     |          | 0 = Normal operation.                                                     |
|     |          | 1 = Places the Si3015 in powerdown mode.                                  |
| 3:0 | Reserved | Must not change in a read-modify-write.                                   |

*Note: Typically used only for board-level debug.*
### U66 DAAC5

<table>
<thead>
<tr>
<th>Bit</th>
<th>D15</th>
<th>D14</th>
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<th>D8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Name</td>
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</table>

Reset settings = 0x0040

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:7</td>
<td>Reserved</td>
<td>Read returns zero.</td>
</tr>
</tbody>
</table>
| 6   | FDT*  | **Frame Detect.**  
 0 = Indicates ISOcap has not established frame lock.  
1 = Indicates ISOcap frame lock has been established. |
| 5:4 | Reserved | Read returns zero. |
| 3:0 | Reserved | Do not modify. |

**Note:** Typically used only for board-level debug.
### Bit 15:8
<table>
<thead>
<tr>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>OFF</td>
<td>Read returns zero.</td>
</tr>
</tbody>
</table>

### Bit 7
<table>
<thead>
<tr>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>OFF</td>
<td><strong>DC Termination Off.</strong></td>
</tr>
<tr>
<td></td>
<td><em>0 = Normal operation.</em></td>
</tr>
<tr>
<td></td>
<td><em>1 = DC termination disabled and the device presents an 800 Ω dc impedance to the line, which is used to enhance operation with an off-hook parallel phone.</em></td>
</tr>
</tbody>
</table>

### Bit 6
<table>
<thead>
<tr>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>OHS</td>
<td><strong>On-Hook Speed.</strong></td>
</tr>
<tr>
<td></td>
<td><em>0 = The Si2456/33/14 will execute a fast on-hook.</em></td>
</tr>
<tr>
<td></td>
<td><em>1 = The Si2456/33/14 will execute a slow controlled on-hook.</em></td>
</tr>
</tbody>
</table>

### Bit 5
<table>
<thead>
<tr>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>ACT</td>
<td><strong>AC Termination Select.</strong></td>
</tr>
<tr>
<td></td>
<td><em>0 = Selects the real impedance.</em></td>
</tr>
<tr>
<td></td>
<td><em>1 = Selects the complex impedance.</em></td>
</tr>
</tbody>
</table>

### Bit 4
<table>
<thead>
<tr>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reserved</td>
<td>Read returns zero.</td>
</tr>
</tbody>
</table>

### Bit 3:2
<table>
<thead>
<tr>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>DCT[1:0]</td>
<td><strong>DC Termination Select.</strong></td>
</tr>
<tr>
<td></td>
<td><em>00 = low voltage mode (Transmit level = −13.85 dBm).</em></td>
</tr>
<tr>
<td></td>
<td><em>01 = Japan mode (Transmit level = −11.85 dBm).</em></td>
</tr>
<tr>
<td></td>
<td><em>10 = FCC mode. Standard voltage mode (Transmit level = −9.85 dBm).</em></td>
</tr>
<tr>
<td></td>
<td><em>11 = CTR21 mode. Current limiting mode (Transmit level = −9.85 dBm).</em></td>
</tr>
</tbody>
</table>

### Bit 1
<table>
<thead>
<tr>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>RZ</td>
<td><strong>Ringer Impedance.</strong></td>
</tr>
<tr>
<td></td>
<td><em>0 = Maximum (high) ringer impedance.</em></td>
</tr>
<tr>
<td></td>
<td><em>1 = Synthesize ringer impedance. C15, R14, Z2, and Z3 must not be installed when setting this bit. See the “Ringer Impedance” section in “AN70: Si2456/Si2433/Si2414/Si2403 Modem Designer’s Guide”.</em></td>
</tr>
</tbody>
</table>

### Bit 0
<table>
<thead>
<tr>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>RT</td>
<td><strong>Ringer Threshold Select.</strong></td>
</tr>
<tr>
<td></td>
<td><em>Used to satisfy country requirements on ring detection. Signals below the lower level do not generate a ring detection; signals above the upper level are guaranteed to generate a ring detection.</em></td>
</tr>
<tr>
<td></td>
<td><em>0 = 11 to 22 Vrms.</em></td>
</tr>
<tr>
<td></td>
<td><em>1 = 17 to 33 Vrms.</em></td>
</tr>
</tbody>
</table>
### U68 ITC2

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:8</td>
<td>Reserved</td>
<td>Read returns zero.</td>
</tr>
<tr>
<td>7:5</td>
<td>Reserved</td>
<td>Do not modify.</td>
</tr>
</tbody>
</table>
| 4  | LIM  | Current Limit.  
     |      | 0 = All other modes.  
     |      | 1 = CTR21 mode. |
| 3  | Reserved | Do not modify. |
| 2  | BTE  | Billing Tone Protect Enable.  
     |      | 0 = Disabled.  
     |      | 1 = Enabled.  
     |      | When set, the DAA responds automatically to a collapse of the line-derived power supply during a billing tone event. When off-hook, if BTE = 1 and BTD goes high, the dc termination is released (800 Ω presented to line). If BTE and RIM (U70, bit 9) are set, an RI (U70, bit 1) interrupt also occurs when BTD goes high. |
| 1  | ROV  | Receive Overload.  
     |      | The bit is set when the receive input (i.e., receive pin goes below ground) has an excessive input level. This bit is cleared by writing a 0 to this location.  
     |      | 0 = Normal receive input level.  
     |      | 1 = Excessive receive input level. |
| 0  | BTD  | Billing Tone Detected.  
     |      | This bit is set if a billing tone is detected. This bit is cleared by writing a 0 to this location.  
     |      | 0 = No billing tone.  
     |      | 1 = Billing tone detected. |

Reset settings = 0x0000
## Si2456/Si2433/Si2414

### U69 ITC3

<table>
<thead>
<tr>
<th>Bit</th>
<th>D15</th>
<th>D14</th>
<th>D13</th>
<th>D12</th>
<th>D11</th>
<th>D10</th>
<th>D9</th>
<th>D8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Name</td>
<td>DIAL</td>
<td>FJM</td>
<td>VOL</td>
<td>FLVM</td>
<td>MODE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Type</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td></td>
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</tr>
</tbody>
</table>

Reset settings = 0x0006

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:8</td>
<td>Reserved</td>
<td>Read returns zero.</td>
</tr>
<tr>
<td>7</td>
<td>Reserved</td>
<td>Do not modify. Must be set to zero.</td>
</tr>
<tr>
<td>6</td>
<td>DIAL</td>
<td><strong>DTMF Dialing Mode.</strong>&lt;br&gt;This bit should be set during DTMF dialing in CTR21 mode if LVCS &lt; 12.&lt;br&gt;<strong>0 = Normal operation.</strong>&lt;br&gt;<strong>1 = Increase headroom for DTMF dialing.</strong></td>
</tr>
<tr>
<td>5</td>
<td>FJM</td>
<td><strong>Force Japan DC Termination Mode.</strong>&lt;br&gt;<strong>0 = Normal Gain.</strong>&lt;br&gt;<strong>1 = When DCT = 2 (FCC mode), setting this bit forces Japan dc termination mode while allowing for a transmit level of –1 dBm. See the “DTMF Dialing” section in “AN70: Si2456/Si2433/Si2414/Si2403 Modem Designer’s Guide”</strong></td>
</tr>
<tr>
<td>4</td>
<td>VOL</td>
<td><strong>Line Voltage Adjust.</strong>&lt;br&gt;When set, this bit adjusts the TIP-RING line voltage. Lowering this voltage improves margin in low-voltage countries. Raising this voltage may improve large-signal distortion performance.&lt;br&gt;<strong>0 = Normal operation.</strong>&lt;br&gt;<strong>1 = Lower DCT voltage.</strong></td>
</tr>
<tr>
<td>3</td>
<td>FLVM</td>
<td><strong>Force Low Voltage Mode.</strong>&lt;br&gt;When DCT (U67, bits 3:2) = 10 (FCC mode), setting FLVM forces the low voltage mode (see DCT = 00) while allowing for a transmit level of –1 dBm.&lt;br&gt;<strong>0 = Disable.</strong>&lt;br&gt;<strong>1 = Enable.</strong></td>
</tr>
<tr>
<td>2</td>
<td>MODE</td>
<td><strong>Mode.</strong>&lt;br&gt;This bit enables on-hook line monitoring. It is automatically set while on-hook and cleared while off-hook.</td>
</tr>
<tr>
<td>1:0</td>
<td>Reserved</td>
<td>Do not modify.</td>
</tr>
</tbody>
</table>
Si2456/Si2433/Si2414

### U6A ITC4

<table>
<thead>
<tr>
<th>Bit</th>
<th>D15</th>
<th>D14</th>
<th>D13</th>
<th>D12</th>
<th>D11</th>
<th>D10</th>
<th>D9</th>
<th>D8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Name</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Type</td>
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</tr>
</tbody>
</table>

Reset settings = N/A

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:3</td>
<td>Reserved</td>
<td>Read returns zero.</td>
</tr>
</tbody>
</table>
| 2   | OVL*  | **Overload Detected.**  
This bit has the same function as ROV but clears itself after the overload has been removed.  
See the “Billing Tone Detection” section in “AN70: Si2456/Si2433/Si2414/Si2403 Modem Designer’s Guide”. This bit is not affected by the BTE bit. |
| 1:0 | Reserved | Do not modify. |

### U6E CK1

<table>
<thead>
<tr>
<th>Bit</th>
<th>D15</th>
<th>D14</th>
<th>D13</th>
<th>D12</th>
<th>D11</th>
<th>D10</th>
<th>D9</th>
<th>D8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Name</td>
<td>R1[4:0]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>Type</td>
<td>R/W</td>
<td>R/W</td>
<td></td>
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</tr>
</tbody>
</table>

Reset settings = 0xF20

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:13</td>
<td>Reserved</td>
<td>Do not modify.</td>
</tr>
</tbody>
</table>
| 12:8 | R1*[4:0] | **CLKOUT Divider**  
0  
CLKOUT off.  
R1  
R1 + 1 (default R1 = 31; 2.4576 MHz). R1 = 31 required for proper codec interface operation. |
| 7:0 | Reserved | Do not modify. |

**Note:** See Figure 5 on page 19.
### U6F PTMR

<table>
<thead>
<tr>
<th>Bit</th>
<th>D15</th>
<th>D14</th>
<th>D13</th>
<th>D12</th>
<th>D11</th>
<th>D10</th>
<th>D9</th>
<th>D8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Name</td>
<td>PTMR[7:0]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>Type</td>
<td>R/W</td>
<td></td>
<td></td>
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</tr>
</tbody>
</table>

Reset settings = 0x00FF

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:8</td>
<td>Reserved</td>
<td>Do not modify</td>
</tr>
<tr>
<td>7:0</td>
<td>PTMR[7:0]</td>
<td>Parallel Port Receive FIFO Interrupt Timer (msec units). See “AN70: Si2456/Si2433/Si2414/Si2403 Modern Designer’s Guide” for more details.</td>
</tr>
</tbody>
</table>
### Si2456/Si2433/Si2414

#### U70 IO0

<table>
<thead>
<tr>
<th>Bit</th>
<th>D15</th>
<th>D14</th>
<th>D13</th>
<th>D12</th>
<th>D11</th>
<th>D10</th>
<th>D9</th>
<th>D8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Name</td>
<td>HES</td>
<td>TES</td>
<td>CIDM</td>
<td>OCDM</td>
<td>PPDM</td>
<td>RIM</td>
<td>DCDM</td>
<td>CID</td>
<td>OCD</td>
<td>PPD</td>
<td>RI</td>
<td>DCD</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Type</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
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<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td></td>
</tr>
</tbody>
</table>

Reset settings = 0x2700

**Bit** | **Name**                | **Function**                                                                                                                                                                                                 |
--------|-------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
15      | HES                     | Hardware Escape Pin.                                                                                                                                                                                        |
        |                         | 0 = Disable.                                                                                                                                                                                               |
        |                         | 1 = Enable.                                                                                                                                                                                                |
14      | Reserved                | Read returns zero.                                                                                                                                                                                         |
13      | TES                     | Enable “+++” Escape.                                                                                                                                                                                       |
        |                         | 0 = Disable.                                                                                                                                                                                                |
        |                         | 1 = Enable.                                                                                                                                                                                                  |
12      | CIDM                    | Caller ID Mask.                                                                                                                                                                                            |
        |                         | 0 = Change in CID will not affect INT.                                                                                                                                                                     |
        |                         | 1 = A low-to-high transition in CID activates INT.                                                                                                                                                          |
11      | OCDM                    | Overcurrent Detect Mask.                                                                                                                                                                                   |
        |                         | 0 = Change in OCD does not affect INT. (“X” result code is not generated in Command mode.)                                                                                                              |
        |                         | 1 = A low-to-high transition in OCD will activate INT. (“X” result code is generated in Command mode.)                                                                                                  |
10      | PPDM                    | Parallel Phone Detect Mask.                                                                                                                                                                                  |
        |                         | 0 = Change in PPD does not affect INT.                                                                                                                                                                     |
        |                         | 1 = A low-to-high transition in PPD will activate INT.                                                                                                                                                      |
9       | RIM                     | Ring Indicator.                                                                                                                                                                                             |
        |                         | 0 = Change in RI does not affect INT.                                                                                                                                                                      |
        |                         | 1 = A low-to-high transition in RI activates INT.                                                                                                                                                          |
8       | DCDM                    | Data Carrier Detect Mask.                                                                                                                                                                                   |
        |                         | 0 = Change in DCD does not affect INT.                                                                                                                                                                     |
        |                         | 1 = A high-to-low transition in DCD (U70, bit 0), which indicates loss of carrier, activates INT.                                                                                                            |
7       | Reserved                | Must be set to zero.                                                                                                                                                                                        |
6:5    | Reserved                | Read returns zero.                                                                                                                                                                                         |
4       | CID                     | Caller ID (sticky).                                                                                                                                                                                         |
        |                         | Caller ID preamble has been detected; data will soon follow. Clears on :I read.                                                                                                                           |
3       | OCD                     | Overcurrent Detect (sticky).                                                                                                                                                                                 |
        |                         | Overcurrent condition has occurred. Clears on :I read.                                                                                                                                                    |
2       | PPD                     | Parallel Phone Detect (sticky).                                                                                                                                                                             |
        |                         | Parallel phone detected since last off-hook event. Clears on :I read.                                                                                                                                       |
1       | RI                      | Ring Indicator.                                                                                                                                                                                             |
        |                         | Active high bit when the Si2456/33/14 is on-hook indicates ring event has occurred. Clears on :I read.                                                                                                      |
0       | DCD                     | Data Carrier Detect (status).                                                                                                                                                                                |
        |                         | Active high bit indicates carrier detected (equivalent to inverse of DCD pin).                                                                                                                              |
### U76 GEN1

<table>
<thead>
<tr>
<th>Bit</th>
<th>D15</th>
<th>D14</th>
<th>D13</th>
<th>D12</th>
<th>D11</th>
<th>D10</th>
<th>D9</th>
<th>D8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Name</td>
<td>OHSR[6:0]</td>
<td>FACL</td>
<td>DCL[2:0]</td>
<td>ACL[4:0]</td>
<td></td>
<td></td>
<td></td>
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<td></td>
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<td></td>
</tr>
<tr>
<td>Type</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td></td>
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</tr>
</tbody>
</table>

Reset settings = 0x3240

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:9</td>
<td>OHSR[6:0]</td>
<td><strong>Off-Hook Sample Rate (40 ms units)</strong>&lt;br&gt;Sets the sample rate for the off-hook intrusion algorithms (1 second default).</td>
</tr>
<tr>
<td>8</td>
<td>FACL</td>
<td><strong>Force ACL.</strong>&lt;br&gt;0 = While off-hook, ACL is automatically updated with LVCS.&lt;br&gt;1 = While off-hook, ACL does not change from the value written to it while on-hook.</td>
</tr>
<tr>
<td>7:5</td>
<td>DCL[2:0]</td>
<td><strong>Differential Current Level (3 mA units).</strong>&lt;br&gt;Sets the differential level between ACL and LVCS that will trigger an off-hook PPD interrupt (default = 2).</td>
</tr>
<tr>
<td>4:0</td>
<td>ACL[4:0]</td>
<td><strong>Absolute Current Level (3 mA units, see Figure 7 on page 20).</strong>&lt;br&gt;ACL represents the value of LVCS current when the Si2456/33/14 is off-hook and all parallel phones are on-hook. If ACL = 0, it is ignored by the off-hook intrusion algorithm. The Si2456/33/14 will also write ACL with the contents of LVCS before an intrusion and before going on-hook (default = 0).</td>
</tr>
</tbody>
</table>
## Si2456/Si2433/Si2414

### U77 GEN2

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Type</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:12</td>
<td>IST[3:0]</td>
<td>R/W</td>
<td>Intrusion Settling Time (250 ms units). Delay between the time the Si2456/33/14 goes off-hook and the time the off-hook intrusion algorithm begins. Default is 1 s.</td>
</tr>
<tr>
<td>11</td>
<td>HOI</td>
<td>R/W</td>
<td>Hang-Up On Intrusion. 0 = Si2456/33/14 will not automatically hang up when an off-hook PPD interrupt occurs. 1 = Si2456/33/14 automatically hangs up on a PPD interrupt. If %Vn commands are set, HOI also causes the &quot;LINE IN USE&quot; result code upon PPD interrupt.</td>
</tr>
<tr>
<td>10</td>
<td>Reserved</td>
<td>R/W</td>
<td>Read returns zero.</td>
</tr>
<tr>
<td>9</td>
<td>AOC</td>
<td>R/W</td>
<td>Overcurrent Protection. Enable Overcurrent protection. 0 = Disable. 1 = Enable. Note: AOC may falsely detect an overcurrent condition in the presence of line reversals or other transients. Therefore, this feature should not be used in applications or locations, such as Japan, where line reversals are common or may be expected.</td>
</tr>
<tr>
<td>8:0</td>
<td>OHT[8:0]</td>
<td>R/W</td>
<td>Off-Hook Time (1 ms units). Time before LVCS is checked for overcurrent condition after going off-hook (30 ms default).</td>
</tr>
</tbody>
</table>

Reset settings = 0x401E
### Si2456/Si2433/Si2414

#### U78 GEN3

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:14</td>
<td>IB[1:0]</td>
<td><strong>Intrusion Blocking</strong>&lt;br&gt;Defines the method used to block the off-hook intrusion algorithm from operation after dialing has begun.&lt;br&gt;&lt;br&gt;0 = <strong>No intrusion blocking</strong>.&lt;br&gt;1 = Intrusion disabled from start of dial to end of dial.&lt;br&gt;2 = Intrusion disabled from start of dial to IS register time-out.&lt;br&gt;3 = Intrusion disabled from start of dial to connect (“CONNECT XXX”, “NO DIALTONE”, or “NO CARRIER”).</td>
</tr>
<tr>
<td>13:8</td>
<td>Reserved</td>
<td>Read returns zero.</td>
</tr>
<tr>
<td>7:0</td>
<td>IS[7:0]</td>
<td><strong>Intrusion Suspend (500 ms units).</strong>&lt;br&gt;When IB = 2, this register sets the length of time, starting when dialing begins, that the off-hook intrusion algorithm is blocked (suspended) (default = 00000000b).</td>
</tr>
</tbody>
</table>

Reset settings = 0x0000
### U79 GEN4

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:5</td>
<td>Reserved</td>
<td>Read returns zero.</td>
</tr>
</tbody>
</table>
| 4:0 | LVCS[4:0]           | **Line Voltage Current Sense.** Represents either the line voltage, loop current, or on-hook line monitor depending on the state of the MODE, OFHK, and ONHM bits. **On-Hook Voltage Monitor** (2.75 V/bit ±20%) (see Figure 6 on page 20).  
00000 = No line connected.  
00001 = Minimum line voltage (V_MIN = 3.0 V ± 0.5 V).  
11111 = Maximum line voltage (87 V ± 20%).  
The line voltage monitor full scale may be modified by changing R5 as follows:  
V_MAX = V_MIN + 4.2 (10M + R5 + 1.6k)/(R5 +1.6k)/5  
U69[2] (MODE) must be set to 1_b before reading LVCS while the Si2456/33/14 is on-hook. See MODE on page 50.  
U69[2] (MODE) must be disabled (MODE = 0_b) before the Si2456/33/14 can go off-hook, dial, or answer a call.  
**Off-Hook Loop Current Monitor** (3 mA/bit) (see Figure 7 on page 20).  
00000 = No loop current.  
00001 = Minimum loop current.  
11110 = Maximum loop current.  
11111 = Loop current is excessive (overload).  
Overload > 140 mA in all modes except CTR21  
Overload > 54 mA in CTR21 mode |

Reset settings = 0x0000
## U7A GENA

<table>
<thead>
<tr>
<th>Bit</th>
<th>D15 D14 D13 D12 D11 D10  D9  D8  D7  D6  D5  D4  D3  D2  D1  D0</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:8</td>
<td>Reserved</td>
<td>Read returns to zero.</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>DOP (Dial or Pulse)</td>
<td>Dial or Pulse.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 = Normal ATDTW operation</td>
<td>0 = Normal ATDTW operation</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 = Use ATDTW for Pulse/Tone Dial Detection (see also ATDW command)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>ADD (Adaptive Dialing)</td>
<td>Adaptive Dialing</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 = Enable</td>
<td>1 = Enable</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 = Disable</td>
<td>0 = Disable</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Attempt DTMF dial, then fall back to pulse dialing if unsuccessful. First digit is dialed as DTMF. If a dialtone is still present after two seconds, the Si2456/33/14 will redial the first digit and remaining digits as pulse. If a dialtone is not present after two seconds, the Si2456/33/14 will dial the remaining digits as DTMF.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5:2</td>
<td>Reserved</td>
<td>Read returns to zero.</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>HDLC (Synchronous Mode.*)</td>
<td>Synchronous Mode.*</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 = Normal asynchronous mode.</td>
<td>0 = Normal asynchronous mode.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 = Transparent HDLC mode.</td>
<td>1 = Transparent HDLC mode.</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>FAST (Fast Connect.*)</td>
<td>Fast Connect.*</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 = Normal modem handshake timing per ITU/Bellcore standards.</td>
<td>0 = Normal modem handshake timing per ITU/Bellcore standards.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 = Fast connect modem handshake timing.</td>
<td>1 = Fast connect modem handshake timing.</td>
<td></td>
</tr>
</tbody>
</table>

*Note: When V22HD, HDLC, or FAST bits are set, 'N0 (wire mode) must be used.
Si2456/Si2433/Si2414

### U7C GENC

<table>
<thead>
<tr>
<th>Bit</th>
<th>D15</th>
<th>D14</th>
<th>D13</th>
<th>D12</th>
<th>D11</th>
<th>D10</th>
<th>D9</th>
<th>D8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Name</td>
<td>RIGPO</td>
<td>RIGPOEN</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Type</td>
<td>R</td>
<td>R/W</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Reset settings = 0x0000

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:5</td>
<td>Reserved</td>
<td>Reads returns to zero.</td>
</tr>
<tr>
<td>4</td>
<td>RIGPO</td>
<td>RI. RI (pin 15), follows this bit when RIGPOEN = 1b.</td>
</tr>
<tr>
<td>3:1</td>
<td>Reserved</td>
<td>Reads returns to zero.</td>
</tr>
<tr>
<td>0</td>
<td>RIGPOEN</td>
<td>0 = RI indicates valid ring signal (Normal ring-indicator mode). 1 = RI (Pin 15) can be used as a general-purpose output and follows U7C[4] (RIGPO).</td>
</tr>
</tbody>
</table>

### U7D GEND

<table>
<thead>
<tr>
<th>Bit</th>
<th>D15</th>
<th>D14</th>
<th>D13</th>
<th>D12</th>
<th>D11</th>
<th>D10</th>
<th>D9</th>
<th>D8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Name</td>
<td>LLV</td>
<td>AUSDC</td>
<td>ATZD</td>
<td>FDP</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Type</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Reset settings = 0x0000

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:11</td>
<td>Reserved</td>
<td>Reads returns to zero.</td>
</tr>
<tr>
<td>10</td>
<td>LLV</td>
<td>0 = Normal operation. 1 = Enables an optional algorithm for countries, such as Japan and Malaysia, with low loop voltage. Also set U67[3:2] (DCT) = 00b, U69[4] VOL = 1b, and U52 = 0x0002 before going off-hook. When the modem goes off-hook, it samples LVCS and changes DCT and VOL as necessary to maximize transmit levels and optimize distortion.</td>
</tr>
<tr>
<td>9</td>
<td>AUSDC</td>
<td>0 = Normal operation. 1 = Causes the modem to go off-hook in Japan mode and then revert to FCC mode after 500 ms. This allows the modem to meet the Australian line seizure requirements while allowing the maximum transmit power (optional for Australia and when DCT = 01b).</td>
</tr>
<tr>
<td>8:2</td>
<td>Reserved</td>
<td>Reads returns to zero.</td>
</tr>
<tr>
<td>1</td>
<td>ATZD</td>
<td>ATZ Disable. 0 = ATZ functions normally. 1 = Disable ATZ command. This may be used to ensure modem settings are not lost in some systems.</td>
</tr>
<tr>
<td>0</td>
<td>FDP</td>
<td>FSK Data Processing. 0 = FSK data processing stops when carrier is lost. 1 = FSK data processing continued for 2 bytes after carrier is lost.</td>
</tr>
</tbody>
</table>
Si2456/Si2433/Si2414

Parallel Interface Registers

Parallel Interface 0 (0x00)

<table>
<thead>
<tr>
<th>Bit</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Name</td>
<td>TX/RX</td>
<td>Type</td>
<td>R/W</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Reset settings = 0x00

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7:0</td>
<td>TX/RX</td>
<td><strong>Parallel Interface Transmit/Receive.</strong> This register functions similarly to the serial port TX pin on writes to the parallel port, and similarly to the serial port RX pin on reads from the parallel port.</td>
</tr>
</tbody>
</table>
**Parallel Interface 1 (0x01)**

<table>
<thead>
<tr>
<th>Bit</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Name</td>
<td>RXF</td>
<td>TXE</td>
<td>REM</td>
<td>INTM</td>
<td>INT</td>
<td>ESC</td>
<td>RTS</td>
<td>CTS</td>
</tr>
<tr>
<td>Type</td>
<td>R</td>
<td>R</td>
<td>R</td>
<td>R/W</td>
<td>R</td>
<td>R/W</td>
<td>R/W</td>
<td>R</td>
</tr>
</tbody>
</table>

**Reset settings = 0110_0011**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
</table>
| 7   | RXF  | **Receive FIFO Almost Full (status).**
|     |      | 0 = Receive FIFO (12 deep) contains three or more empty locations (RXF ≤ 9). The host can clear the RXF interrupt without emptying the RX FIFO by writing a 0 to the RXF bit. This will disable the RXF interrupt until the host has emptied the FIFO.
|     |      | 1 = Receive FIFO contains two or less empty locations (RXF ≥ 10). |
| 6   | TXE  | **Transmit FIFO Almost Empty (status).**
|     |      | 0 = Transmit FIFO (14 deep) contains three or more characters (TXF ≥ 3).
|     |      | 1 = Transmit FIFO contains two or less characters (TXF ≤ 2). TXE interrupt will not trigger if the CTS bit is inactive. Therefore, the host does not need to poll CTS while waiting for transmit FIFO to empty. TXE can be cleared by writing it to 0. |
| 5   | REM  | **Receive FIFO Empty.**
|     |      | 0 = Receive FIFO has valid data.
|     |      | 1 = Receive FIFO empty.
|     |      | **Note:** If the interim timer (see PTMR - U6F, bits 7:0) set by PTMR expires, it will cause an interrupt. This interrupt will not set RXF, TXE, or INT. The interrupt handler on the host should then verify that REM = 0 and begin to empty the receive FIFO (Parallel Interface 0 register) until REM = 1. |
| 4   | INTM | **Interrupt Mask.**
|     |      | 0 = In parallel mode, the INT pin is triggered by a rising edge on RXF or TXE only (default).
|     |      | 1 = In parallel mode, the INT pin is triggered by a rising edge on RXF, TXE, or INT. |
| 3   | INT  | **Interrupt.**
|     |      | 0 = No interrupt has occurred.
|     |      | 1 = Indicates that an interrupt (CID, OCD, PPD, RI, or DCD from U70) has occurred. This bit is cleared via the AT:I command. |
| 2   | ESC  | **Escape.**
|     |      | Operation of this bit in parallel mode is functionally-equivalent to the ESC pin in serial mode. |
| 1   | RTS  | **Request-to-Send.**
|     |      | Operation of this bit in parallel mode is functionally equivalent to the RTS pin in serial mode.
|     |      | Use of the CTS and RTS bits (as opposed to the TXE and RXF bits) allows the flow control between the host and the Si2456/33/14 to operate 1 byte at a time rather than in blocks. |
| 0   | CTS  | **Clear-to-Send.**
|     |      | Operation of this bit in parallel mode is functionally-equivalent to the CTS pin in serial mode.
|     |      | Use of the CTS and RTS bits (as opposed to the TXE and RXF bits) allows the flow control between the host and the Si2456/33/14 to operate 1 byte at a time, rather than in blocks. |
## Pin Descriptions: Si2456/33/14

<table>
<thead>
<tr>
<th>Pin #</th>
<th>Pin Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>CLKIN/XTALI</td>
<td><strong>Clock Input/Crystal Oscillator Pin.</strong> This pin provides support for parallel-resonant, AT-cut crystals. XTALI also acts as an input in the event that an external clock source is used in place of a crystal. A 4.9152 MHz crystal or 4.9152 MHz clock is required.</td>
</tr>
<tr>
<td>2</td>
<td>XTALO</td>
<td><strong>Crystal Oscillator Pin.</strong> This pin provides support for parallel-resonant AT-cut crystals. XTALO serves as the output of the crystal amplifier.</td>
</tr>
<tr>
<td>3</td>
<td>CLKOUT/EECS/A0</td>
<td><strong>Clock Output/EEPROM Chip Select/Address Bit 0.</strong> Clock output in serial mode. Active low read/write enable for SPI EEPROM in serial mode when pin 4 is pulled low during powerup. Address Enable in parallel mode.</td>
</tr>
<tr>
<td>4</td>
<td>D6</td>
<td><strong>Data Bit.</strong> Bidirectional parallel bus data bit 6 in parallel mode.</td>
</tr>
<tr>
<td>5, 19</td>
<td>VD3.3</td>
<td><strong>Digital Supply Voltage.</strong> Provides the 3.3 V digital supply voltage to the Si2456/33/14.</td>
</tr>
<tr>
<td>6, 18</td>
<td>GND</td>
<td><strong>Ground.</strong> Connects to the system digital ground.</td>
</tr>
<tr>
<td>7, 17</td>
<td>VDA, VDB</td>
<td><strong>Digital Rail.</strong> Pin provides decoupling for the internal power supplies.</td>
</tr>
<tr>
<td>8</td>
<td>RTS/D7</td>
<td><strong>Request-to-Send/Data Bit.</strong> Request-to-send (for flow control) in serial mode. Bidirectional parallel bus data bit 7 in parallel mode.</td>
</tr>
<tr>
<td>9</td>
<td>RXD/RD</td>
<td><strong>Receive Data/Read Enable.</strong> Data output to DTE RXD pin in serial mode. Active low read enable pin in parallel mode.</td>
</tr>
<tr>
<td>Pin #</td>
<td>Pin Name</td>
<td>Description</td>
</tr>
<tr>
<td>-------</td>
<td>----------</td>
<td>-------------</td>
</tr>
</tbody>
</table>
| 10    | TXD/WR   | Transmit Data/Write Enable.  
*Data input from DTE TXD pin in serial mode. Active low write-enable pin in parallel mode.* |
| 11    | CTS/CS   | Clear-to-Send/Chip Select.  
*Active low clear-to-send (for flow control) in serial mode. Active low chip select in parallel mode.* |
| 12    | RESET    | Reset Input.  
*An active low input that is used to reset all control registers to a defined initialized state.* |
| 13    | AOUT/INT | Analog Output/Interrupt Output.  
*Analog output in serial mode. Active low interrupt output in parallel mode.* |
| 14    | INT/D0   | Interrupt Output/Data Bit.  
*Active low interrupt output in serial mode. Bidirectional parallel bus data bit 0 in parallel mode.* |
| 15    | RI/D1    | Ring Indicator/Data Bit.  
*The RI on (active low) indicates the presence of an ON segment of a ring signal on the telephone line. Bidirectional parallel bus data bit 1 in parallel mode.* |
| 16    | EESD/D2  | EEPROM Serial Data Input/Output/Data Bit.  
*Bidirectional Input/Output to SPI EEPROM in serial mode. Bidirectional parallel bus data bit 2 in parallel mode.* |
| 20    | ISOB     | Bias Voltage.  
*This pin provides decoupling for the power supply.* |
| 21    | C1A      | Isolation Capacitor 1A.  
*Connects to one side of the isolation capacitor, C1.* |
| 22    | ESC/D3   | Escape/Data Bit.  
*Hardware escape in serial mode. Bidirectional parallel bus data bit 3 in parallel mode.* |
| 23    | DCD/D4   | Carrier Detect/Data Bit.  
*Active low-carrier detect in serial mode. Bidirectional parallel bus data bit 4 in parallel mode.* |
| 24    | EECLK/D5 | EEPROM Clock/Data Bit.  
*Clock output for SPI EEPROM in serial mode. Bidirectional parallel bus data bit 5 in parallel mode.* |
## Pin Descriptions: Si3015

<table>
<thead>
<tr>
<th>Pin #</th>
<th>Pin Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>QE2</td>
<td>Transistor Emitter 2. Connects to the emitter of Q4.</td>
</tr>
<tr>
<td>2</td>
<td>DCT</td>
<td>DC Termination. Provides dc termination to the telephone network.</td>
</tr>
<tr>
<td>3</td>
<td>IGN D</td>
<td>Isolated Ground. Connects to ground on the line-side interface. Also connects to capacitor C2.</td>
</tr>
<tr>
<td>4</td>
<td>C1B</td>
<td>Isolation Capacitor 1B. Connects to one side of isolation capacitor C1.</td>
</tr>
<tr>
<td>5</td>
<td>RNG1</td>
<td>Ring 1. Connects through a capacitor to the TIP lead of the telephone line. Provides the ring and caller ID signals to the modem.</td>
</tr>
<tr>
<td>6</td>
<td>RNG2</td>
<td>Ring 2. Connects through a capacitor to the RING lead of the telephone line. Provides the ring and caller ID signals to the modem.</td>
</tr>
<tr>
<td>7</td>
<td>QB</td>
<td>Transistor Base. Connects to the base of transistor Q3.</td>
</tr>
<tr>
<td>8</td>
<td>QE</td>
<td>Transistor Emitter. Connects to the emitter of transistor Q3.</td>
</tr>
<tr>
<td>9</td>
<td>VREG</td>
<td>Voltage Regulator. Connects to an external capacitor to provide bypassing for an internal power supply.</td>
</tr>
<tr>
<td>10</td>
<td>VREG2</td>
<td>Voltage Regulator 2. Connects to an external capacitor to provide bypassing for an internal power supply.</td>
</tr>
<tr>
<td>11</td>
<td>REF</td>
<td>Reference. Connects to an external resistor to provide a high-accuracy reference current.</td>
</tr>
<tr>
<td>12</td>
<td>REXT2</td>
<td>External Resistor 2. Sets the complex ac termination impedance.</td>
</tr>
<tr>
<td>13</td>
<td>REXT</td>
<td>External Resistor. Sets the real ac termination impedance.</td>
</tr>
</tbody>
</table>
### Pin Description

<table>
<thead>
<tr>
<th>Pin #</th>
<th>Pin Name</th>
<th>Description</th>
</tr>
</thead>
</table>
| 14 RX | Receive Input.  
Serves as the receive side input from the telephone network. |
| 15 FILT | Filter.  
Provides filtering for the dc termination circuits. |
| 16 FILT2 | Filter 2.  
Provides filtering for the bias circuits. |
### Ordering Guide

<table>
<thead>
<tr>
<th>Chipset</th>
<th>Description</th>
<th>Digital</th>
<th>Line</th>
<th>Temperature</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si2456</td>
<td>Commercial</td>
<td>Si2456-KT</td>
<td>Si3015-KS</td>
<td>0 to 70 °C</td>
</tr>
<tr>
<td>Si2456</td>
<td>Commercial lead-free</td>
<td>Si2456-FT</td>
<td>Si3015-FS</td>
<td>0 to 70 °C</td>
</tr>
<tr>
<td>Si2456</td>
<td>Industrial</td>
<td>Si2456-BT</td>
<td>Si3015-BS</td>
<td>–40 to 85 °C</td>
</tr>
<tr>
<td>Si2433</td>
<td>Commercial</td>
<td>Si2433-KT</td>
<td>Si3015-KS</td>
<td>0 to 70 °C</td>
</tr>
<tr>
<td>Si2433</td>
<td>Commercial lead-free</td>
<td>Si2433-FT</td>
<td>Si3015-FS</td>
<td>0 to 70 °C</td>
</tr>
<tr>
<td>Si2433</td>
<td>Industrial</td>
<td>Si2433-BT</td>
<td>Si3015-BS</td>
<td>–40 to 85 °C</td>
</tr>
<tr>
<td>Si2414</td>
<td>Commercial</td>
<td>Si2414-KT</td>
<td>Si3015-KS</td>
<td>0 to 70 °C</td>
</tr>
<tr>
<td>Si2414</td>
<td>Commercial lead-free</td>
<td>Si2414-FT</td>
<td>Si3015-FS</td>
<td>0 to 70 °C</td>
</tr>
<tr>
<td>Si2414</td>
<td>Industrial</td>
<td>Si2414-BT</td>
<td>Si3015-BS</td>
<td>–40 to 85 °C</td>
</tr>
</tbody>
</table>
Package Outline: 24-Pin TSSOP

Figure 8 illustrates the package details for the Si2456/33/14. Table 16 lists the values for the dimensions shown in the illustration.

![Diagram of 24-Pin TSSOP Package]

Approximate device weight is 115.7 mg.

Figure 8. 24-Pin Thin Shrink Small Outline Package (TSSOP)

Table 16. Package Diagram Dimensions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Millimeters</th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Symbol</td>
<td>Min</td>
<td>Max</td>
</tr>
<tr>
<td>A</td>
<td>1.20</td>
<td></td>
<td></td>
</tr>
<tr>
<td>A1</td>
<td>0.05</td>
<td>0.15</td>
<td></td>
</tr>
<tr>
<td>B</td>
<td>0.19</td>
<td>0.30</td>
<td></td>
</tr>
<tr>
<td>C</td>
<td>0.09</td>
<td>0.20</td>
<td></td>
</tr>
<tr>
<td>D</td>
<td>7.70</td>
<td>7.90</td>
<td></td>
</tr>
<tr>
<td>E</td>
<td>4.30</td>
<td>4.50</td>
<td></td>
</tr>
<tr>
<td>e</td>
<td>0.65</td>
<td>BSC</td>
<td></td>
</tr>
<tr>
<td>H</td>
<td>6.40</td>
<td>BSC</td>
<td></td>
</tr>
<tr>
<td>L</td>
<td>0.45</td>
<td>0.75</td>
<td></td>
</tr>
<tr>
<td>θ</td>
<td>0°</td>
<td>8°</td>
<td></td>
</tr>
<tr>
<td>γ</td>
<td>0.10</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

*Note: To guarantee coplanarity (γ), the parameters marked “Typical” may be exceeded.
Package Outline: 16-Pin SOIC

Figure 9 illustrates the package details for the Si3015. Table 17 lists the values for the dimensions shown in the illustration.

Table 17. Package Diagram Dimensions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Millimeters</th>
<th>Typical*</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Min</td>
<td>Max</td>
</tr>
<tr>
<td>A</td>
<td>1.35</td>
<td>1.75</td>
</tr>
<tr>
<td>A1</td>
<td>.10</td>
<td>.25</td>
</tr>
<tr>
<td>A2</td>
<td>1.30</td>
<td>1.50</td>
</tr>
<tr>
<td>B</td>
<td>.33</td>
<td>.51</td>
</tr>
<tr>
<td>C</td>
<td>.19</td>
<td>.25</td>
</tr>
<tr>
<td>D</td>
<td>9.80</td>
<td>10.01</td>
</tr>
<tr>
<td>E</td>
<td>3.80</td>
<td>4.00</td>
</tr>
<tr>
<td>e</td>
<td>1.27</td>
<td></td>
</tr>
<tr>
<td>H</td>
<td>5.80</td>
<td>6.20</td>
</tr>
<tr>
<td>h</td>
<td>.25</td>
<td>.50</td>
</tr>
<tr>
<td>L</td>
<td>.40</td>
<td>1.27</td>
</tr>
<tr>
<td>γ</td>
<td>—</td>
<td>0.10</td>
</tr>
<tr>
<td>θ</td>
<td>0°</td>
<td>8°</td>
</tr>
</tbody>
</table>

*Note: Typical parameters are for information purposes only.
Document Change List
Revision 0.9 to Revision 1.0.
- The Si2456/33/14 data sheet has changed significantly since revision 0.9. In order to offer a simplified reference for customers, many of the detailed feature explanations have been moved to the Si2456/33/14 User’s Guide (“AN70: Si2456/Si2433/Si2414/Si2403 Modem Designer’s Guide”). Therefore, many of the following changes refer not only to this data sheet, but also to the new revision of AN70.
- Updated “Parallel Interface” on page 17.
- Updated register, "Parallel Interface 1 (0x01)" on page 61.
- Added register, “U6F PTMR” on page 52.
- Added “Autobaud” on page 17.
- Added “V.29 Fast Connect” on page 18 and associated AT commands.
- Added “EEPROM Interface” on page 21.
- Updated “Pin Assignments” on page 1, “Pin Descriptions: Si2456/33/14” on page 62, and “Typical Application Schematic” on page 11 to include EEPROM support.
- Updated "Clocking/Low Power Modes" on page 18
- Added &Pn, &Xn, &Dn, &G3, &G4, &T4, &T5, &T, \T16, \T17, %B, %Vn, +GCl, and \N5 commands.
- Added G modifier to ATD command
- Added S-registers S40, S41, S42, S50 in Table 13.
- Updated S-register S7 in Table 13
- Added result codes 40–45 in Table 12
- Updated Figure 8, “24-Pin Thin Shrink Small Outline Package (TSSOP)".
- Updated “Typical Application Schematic“.
- Added AT2D bit (U7D, bit 2).
- Removed Country-Specific Register Settings table.
- Updated Table 14.
- Updated Table 15.
- Added -FT, -FS lead-free commercial-grade device ordering option.
- Changed Note 3 in “Bill of Materials: Si2456/33/14 Chipset” on page 12.
- Removed U-register IO1 (U71)
- Added U-registers U7C and U7D
- Removed CCAD bit (U40, bit 9)
- Added LCN bit (U47, bit 0)
- Added RFWE bit (U69, bit 1)
- Removed RST bit (U6E, bit 4)
- Moved AOUT schematic and component values table to AN70.
- Updated Pullup Resistance Pins in Table 3.
Contact Information

Silicon Laboratories Inc.
4635 Boston Lane
Austin, TX 78735
Tel: 1+(512) 416-8500
Fax: 1+(512) 416-9669
Toll Free: 1+(877) 444-3032
Email: productinfo@silabs.com
Internet: www.silabs.com

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