

## Infrared Transceiver Module (SIR, 115.2 kbit/s) for IrDA® applications

### Description

The TFDU4300 is a low profile (2.5 mm) infrared transceiver module with independent logic reference voltage ( $V_{logic}$ ) for low voltage IO interfacing. It is compliant to the latest IrDA® physical layer standard for fast infrared data communication, supporting IrDA® speeds up to 115.2 kbit/s (SIR) and carrier based remote control. The transceiver module consists of a PIN photodiode, an infrared emitter (IRED), and a low-power control IC to provide a total front-end solution in a single package.

This device covers an extended IrDA® low power range of close to 1 m. With an external current control resistor the current can be adjusted for shorter ranges.

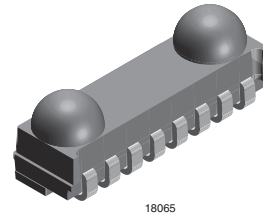
This Vishay SIR transceiver is built in a new smaller package using the experiences of the lead frame BabyFace technology.

### Features

- Compliant to the latest IrDA® physical layer specification (9.6 kbit/s to 115.2 kbit/s) and TV Remote Control, bi-directional operation included.
- Operates from 2.4 V to 5.5 V within specification over full temperature range from - 30 °C to + 85 °C
- Logic voltage 1.5 V to 5.5 V is independent of IRED driver and analog supply voltage
- Split power supply, transmitter and receiver can be operated from two power supplies with relaxed requirements saving costs, US Patent No. 6,157,476
- Extended IrDA® Low Power range to about 70 cm
- Typical Remote Control range 12 m
- Low power consumption (< 0.12 mA supply current)
- Power shutdown mode (< 5  $\mu$ A shutdown current in full temperature range, up to 85 °C)

### Applications

- Ideal for battery operated applications
- Telecommunication products (cellular phones, pagers)
- Digital still and video cameras
- Printers, fax machines, photocopiers, screen projectors
- Medical and industrial data collection
- Diagnostic systems



The Rxd output pulse width is independent of the optical input pulse width and stays always at a fixed pulse width thus making the device optimum for standard Endecs. TFDU4300 has a tri-state output and is floating in shut-down mode with a weak pull-up.

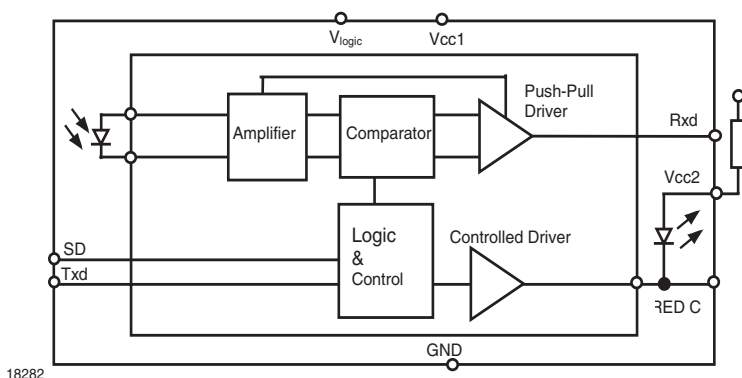
- Surface mount package, low profile (2.5 mm) - (L 8.5 mm x H 2.5 mm x W 2.9 mm)
- High efficiency emitter
- Low profile (universal) package capable of surface mount soldering to side and top view orientation
- Directly interfaces with various Super I/O and controller devices as e.g. TOIM4232
- Tri-state-receiver output, floating in shut down with a weak pull-up
- Compliant with IrDA background light specification
- EMI immunity in GSM bands > 300 V/m verified
- Lead(Pb)-free device
- Device in accordance to RoHS 2002/95/EC and WEEE 2002/96EC

- Notebook computers, desktop PCs, Palmtop computers (Win CE, Palm PC), PDAs
- Internet TV boxes, video conferencing systems
- External infrared adapters (Dongles)
- Data loggers
- GPS
- Kiosks, POS, Point and Pay devices including IrFM - applications

## Parts Table

Part	Description	Qty / Reel
TFDU4300-TR1	Oriented in carrier tape for side view surface mounting	750 pcs
TFDU4300-TR3	Oriented in carrier tape for side view surface mounting	2500 pcs
TFDU4300-TT1	Oriented in carrier tape for top view surface mounting	750 pcs
TFDU4300-TT3	Oriented in carrier tape for top view surface mounting	2500 pcs

## Functional Block Diagram

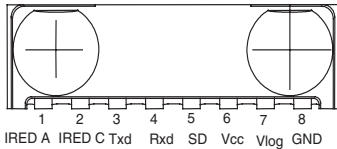


## Pin Description

Pin Number	Function	Description	I/O	Active
1	V <sub>CC2</sub> IRED Anode	Connect IRED anode directly to the power supply (V <sub>CC2</sub> ). IRED current can be decreased by adding a resistor in series between the power supply and IRED anode. A separate unregulated power supply can be used at this pin.		
2	IRED Cathode	IRED Cathode, internally connected to the driver transistor		
3	Txd	This Schmitt-Trigger input is used to transmit serial data when SD is low. An on-chip protection circuit disables the LED driver if the Txd pin is asserted for longer than 300 μs. The input threshold voltage adapts to and follows the logic voltage swing defined by the applied V <sub>logic</sub> voltage.	I	HIGH
4	Rxd	Received Data Output, push-pull CMOS driver output capable of driving standard CMOS or TTL loads. During transmission the Rxd output is inactive. No external pull-up or pull-down resistor is required. Floating with a weak pull-up of 500 kΩ (typ.) in shutdown mode. The voltage swing is defined by the applied V <sub>logic</sub> voltage.	O	LOW
5	SD	Shutdown. The input threshold voltage adapts to and follows the logic voltage swing defined by the applied V <sub>logic</sub> voltage.	I	HIGH
6	V <sub>CC1</sub>	Supply Voltage		
7	V <sub>logic</sub>	V <sub>logic</sub> defines the logic voltage level of the I/O ports to adapt the logic voltage swing to the IR controller. The Rxd output range is from 0 V to V <sub>logic</sub> , for optimum noise suppression the inputs- logic decision level is 0.5 x V <sub>logic</sub>	I	
8	GND	Ground		

### Pinout

TFDU4300  
weight 75 mg



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### Definitions:

In the Vishay transceiver data sheets the following nomenclature is used for defining the IrDA<sup>®</sup> operating modes:

SIR: 2.4 kbit/s to 115.2 kbit/s, equivalent to the basic serial infrared standard with the physical layer version IrPhy 1.0

MIR: 576 kbit/s to 1152 kbit/s

FIR: 4 Mbit/s

VFIR: 16 Mbit/s

MIR and FIR were implemented with IrPhy 1.1, followed by IrPhy 1.2, adding the SIR Low Power Standard. IrPhy 1.3 extended the Low Power Option to MIR and FIR and VFIR was added with IrPhy 1.4. A new version of the standard in any case obsoletes the former version.

With introducing the updated versions the old versions are obsolete. Therefore the only valid IrDA<sup>®</sup> standard is the actual version IrPhy 1.4 (in Oct. 2002).

### Absolute Maximum Ratings

Reference point Ground (pin 8) unless otherwise noted.

Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Parameter	Test Conditions	Symbol	Min	Typ.	Max	Unit
Supply voltage range, transceiver	- 0.3 V < V <sub>CC2</sub> < 6 V - 0.5 V < V <sub>logic</sub> < 6 V	V <sub>CC1</sub>	- 0.5		+ 6.0	V
Supply voltage range, transmitter	- 0.5 V < V <sub>CC1</sub> < 6 V - 0.5 V < V <sub>logic</sub> < 6 V	V <sub>CC2</sub>	- 0.5		+ 6.0	V
Supply voltage range, V <sub>logic</sub>	- 0.5 V < V <sub>CC1</sub> < 6 V - 0.3 V < V <sub>CC2</sub> < 6 V	V <sub>logic</sub>	- 0.5		+ 6.0	V
Rxd output voltage	- 0.5 V < V <sub>CC1</sub> < 6 V - 0.3 V < V <sub>logic</sub> < 6 V	V <sub>Rxd</sub>	- 0.5		V <sub>logic</sub> + 0.5	V
Voltage at all inputs	Note: V <sub>in</sub> ≥ V <sub>CC1</sub> is allowed	V <sub>IN</sub>	- 0.5		+ 6.0	V
Input current	for all pins, except IRED anode pin				10	mA
Output sinking current					25	mA
Power dissipation	see derating curve	P <sub>D</sub>			250	mW
Junction temperature		T <sub>J</sub>			125	°C
Ambient temperature range (operating)		T <sub>amb</sub>	- 30		+ 85	°C
Storage temperature range		T <sub>stg</sub>	- 40		+ 100	°C
Soldering temperature	see recommended solder profile				260	°C
Average output current, pin 1		I <sub>IRED(DC)</sub>			125	mA
Repetitive pulsed output current, pin 1 to pin 2	t < 90 μs, t <sub>on</sub> < 20 %	I <sub>IRED(RP)</sub>			600	mA

## Eye safety information

Parameter	Test Conditions	Symbol	Min	Typ.	Max	Unit
Virtual source size	Method: (1-1/e) encircled energy	d	1.3	1.8		mm
Maximum intensity for class 1	IEC60825-1 or EN60825-1, edition Jan. 2001, operating below the absolute maximum ratings	$I_e$			<sup>*)</sup> (500 <sup>**</sup> )	mW/sr

<sup>\*)</sup> Due to the internal limitation measures the device is a "class 1" device under all conditions.

<sup>\*\*</sup>) IrDA specifies the max. intensity with 500 mW/sr.

**Note:** We apologize to use sometimes in our documentation the abbreviation LED and the word Light Emitting Diode instead of Infrared Emitting Diode (IRED) for IR-emitters. That is by definition wrong; we are here following just a bad trend.

Typical values are for design aid only, not guaranteed nor subject to production testing and may vary with time.

**Electrical Characteristics**
**Transceiver**

 Tested @  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ,  $V_{CC1} = V_{CC2} = 2.7\text{ V to }5.5\text{ V}$  unless otherwise noted.

Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Parameter	Test Conditions	Symbol	Min	Typ.	Max	Unit
Supply voltage	Remark: For $2.4\text{ V} < V_{CC1} < 2.6\text{ V}$ @ $T_{amb} < -25\text{ }^{\circ}\text{C}$ a minor reduction of the receiver sensitivity may occur	$V_{CC1}$	2.4		5.5	V
Idle supply current @ $V_{CC1}$ (receive mode, no signal)	$SD = \text{Low}$ , $E_e = 1\text{ klx}^*)$ , $T_{amb} = -25\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ , $V_{CC1} = V_{CC2} = 2.7\text{ V to }5.5\text{ V}$	$I_{CC1}$		90	130	$\mu\text{A}$
	$SD = \text{Low}$ , $E_e = 1\text{ klx}^*)$ , $T_{amb} = 25\text{ }^{\circ}\text{C}$ , $V_{CC1} = V_{CC2} = 2.7\text{ V to }5.5\text{ V}$	$I_{CC1}$		75		$\mu\text{A}$
Idle supply current @ $V_{logic}$ (receive mode, no signal)	$SD = \text{Low}$ , $E_e = 1\text{ klx}^*)$ , $V_{log}$ , pin 7, no signal, no load @ Rxd	$I_{log}$			1	$\mu\text{A}$
Average dynamic supply current, transmitting	$I_{IRED} = 300\text{ mA}$ , 20 % Duty Cycle	$I_{CC1}$			0.65	mA
Standby supply current	$SD = \text{High}$ , $T = 25\text{ }^{\circ}\text{C}$ , $E_e = 0\text{ klx}$	$I_{SD}$			0.1	$\mu\text{A}$
	$SD = \text{High}$ , $T = 70\text{ }^{\circ}\text{C}$	$I_{SD}$			2	$\mu\text{A}$
	$SD = \text{High}$ , $T = 85\text{ }^{\circ}\text{C}$	$I_{SD}$			3	$\mu\text{A}$
Standby supply current, $V_{logic}$	no signal, no load	$I_{log}$			1	$\mu\text{A}$
Operating temperature range		$T_A$	-30		+85	$^{\circ}\text{C}$
Output voltage low, Rxd	$C_{Load} = 15\text{ pF}$	$V_{OL}$	-0.5		$0.15 \times V_{logic}$	V
Output voltage high, Rxd	$I_{OH} = -500\text{ }\mu\text{A}$	$V_{OH}$	$0.8 \times V_{logic}$		$V_{logic} + 0.5$	V
	$I_{OH} = -250\text{ }\mu\text{A}$ , $C_{Load} = 15\text{ pF}$	$V_{OH}$	$0.9 \times V_{logic}$		$V_{logic} + 0.5$	V
Rxd to $V_{CC1}$ impedance		$R_{Rxd}$	400	500	600	$\text{k}\Omega$
Input voltage low (Txd, SD)		$V_{IL}$	-0.5		0.5	V
Input voltage high (Txd, SD)	CMOS level**), $V_{logic} \geq 2.5\text{ V}$	$V_{IH}$	$V_{logic} - 0.5$		6	V
Input voltage high (Txd, SD)	CMOS level**), $V_{logic} < 2.5\text{ V}$	$V_{IH}$	$0.8 \times V_{logic}$		6	V
Input leakage current (Txd, SD)	$V_{IN} = 0.9 \times V_{logic}$	$I_{ICH}$	-2		+2	$\mu\text{A}$
Controlled pull down current	$SD$ , Txd = "0" to "1", $V_{IN} < 0.15 V_{logic}$	$I_{IRTX}$			+150	$\mu\text{A}$
	$SD$ , Txd = "0" to "1", $V_{IN} > 0.7 V_{logic}$	$I_{IRTX}$	-1	0	1	$\mu\text{A}$
Input capacitance (Txd, SD)		$C_{IN}$			5	pF

\*) Standard illuminant A

 \*\*) To provide an improved immunity with increasing  $V_{logic}$  the typical threshold level is increasing with  $V_{logic}$  and set to  $0.5 \times V_{logic}$ . It is recommended to use the specified min/max values to avoid increased operating current.

### Optoelectronic Characteristics

#### Receiver

Tested @  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ,  $V_{CC1} = V_{CC2} = 2.7\text{ V}$  to  $5.5\text{ V}$  unless otherwise noted.

Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Parameter	Test Conditions	Symbol	Min	Typ.	Max	Unit
Minimum irradiance $E_e$ in angular range **)	9.6 kbit/s to 115.2 kbit/s $\lambda = 850\text{ nm} - 900\text{ nm}$ $\alpha = 0\text{ }^{\circ}, 15\text{ }^{\circ}$	$E_e$		40 (4)	80 (8)	$\text{mW/m}^2$ ( $\mu\text{W/cm}^2$ )
Maximum Irradiance $E_e$ In Angular Range ***)	$\lambda = 850\text{ nm} - 900\text{ nm}$	$E_e$		5 (500)		$\text{kW/m}^2$ ( $\text{mW/cm}^2$ )
Maximum no detection irradiance	$\lambda = 850\text{ nm} - 900\text{ nm}$ $t_r, t_f < 40\text{ ns}$ , $t_{po} = 1.6\text{ }\mu\text{s}$ @ $f = 115\text{ kHz}$ , no output signal allowed	$E_e$	4 (0.4)			$\text{mW/m}^2$ ( $\mu\text{W/cm}^2$ )
Rise time of output signal	10 % to 90 %, $C_L = 15\text{ pF}$	$t_{r(Rxd)}$	20		100	ns
Fall time of output signal	90 % to 10 %, $C_L = 15\text{ pF}$	$t_{f(Rxd)}$	20		100	ns
Rxd pulse width of output signal	input pulse length $> 1.2\text{ }\mu\text{s}$	$t_{PW}$	1.65	2.0	3.0	$\mu\text{s}$
Stochastic jitter, leading edge	input irradiance = $100\text{ mW/m}^2$ , $\leq 115.2\text{ kbit/s}$				250	ns
Standby /Shutdown delay, receiver startup time	after shutdown active or power-on				150	$\mu\text{s}$
Latency		$t_L$		100	150	$\mu\text{s}$

) Equivalent to IrDA® Background Light and Electromagnetic Field Test: Fluorescent Lighting Immunity.

\*\*) IrDA sensitivity definition: **Minimum Irradiance  $E_e$  In Angular Range**, power per unit area. The receiver must meet the BER specification while the source is operating at the minimum intensity in angular range into the minimum half-angular range at the maximum Link Length.

\*\*\*) **Maximum Irradiance  $E_e$  In Angular Range**, power per unit area. The optical delivered to the detector by a source operating at the maximum intensity in angular range at Minimum Link Length must not cause receiver overdrive distortion and possible related link errors. If placed at the Active Output Interface reference plane of the transmitter, the receiver must meet its bit error ratio (BER). For more definitions see the document "Symbols and Terminology" on the Vishay Website (<http://www.vishay.com/docs/82512/82512.pdf>).

## Transmitter

Tested @  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ,  $V_{CC1} = V_{CC2} = 2.7\text{ V}$  to  $5.5\text{ V}$  unless otherwise noted.

Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Parameter	Test Conditions	Symbol	Min	Typ.	Max	Unit
IRED operating current limitation	No external resistor for current limitation <sup>*)</sup>	$I_D$	250	300	350	mA
Forward voltage of built-in IRED	$I_f = 300\text{ mA}$	$V_f$	1.4	1.8	1.9	V
Output leakage IRED current	$T_{xd} = 0\text{ V}$ , $0 < V_{CC1} < 5.5\text{ V}$	$I_{IRED}$	- 1		1	$\mu\text{A}$
Output radiant intensity	$\alpha = 0\text{ }^{\circ}$ , $15\text{ }^{\circ}$ $T_{xd} = \text{High}$ , $SD = \text{Low}$	$I_e$	30	65		mW/sr
	$V_{CC1} = 5.0\text{ V}$ , $\alpha = 0\text{ }^{\circ}$ , $15\text{ }^{\circ}$ $T_{xd} = \text{Low}$ or $SD = \text{High}$ (Receiver is inactive as long as $SD = \text{High}$ )	$I_e$			0.04	mW/sr
Output radiant intensity, angle of half intensity		$\alpha$		$\pm 24$		$^{\circ}$
Peak - emission wavelength <sup>**)</sup>		$\lambda_p$	880		900	nm
Spectral bandwidth		$\Delta\lambda$		45		nm
Optical rise time, fall time		$t_{ropt}$ , $t_{fopt}$			100	ns
Optical output pulse duration	input pulse width $1.6 < t_{Txd} < 20\text{ }\mu\text{s}$	$t_{opt}$	$t_{Txd} - 0.15$		$t_{Txd} + 0.15$	$\mu\text{s}$
	input pulse width $t_{Txd} \geq 20\text{ }\mu\text{s}$	$t_{opt}$		20	300	$\mu\text{s}$
Optical overshoot					25	%

<sup>\*)</sup> Using an external current limiting resistor is allowed and recommended to reduce IRED intensity and operating current when current reduction is intended to operate at the IrDA<sup>®</sup> low power conditions. E.g. for  $V_{CC2} \geq 3.3\text{ V}$  a current limiting resistor of  $R_S = 56\text{ }\Omega$  will allow a power minimized operation at IrDA<sup>®</sup> low power conditions.

<sup>\*\*)</sup> Note: Due to this wavelength restriction compared to the IrDA spec of 850 nm to 900 nm the transmitter is able to operate as source for the standard Remote Control applications with codes as e.g. Philips RC5/RC6<sup>®</sup> or RECS 80.

### Recommended Circuit Diagram

Operated with a clean low impedance power supply the TFDU4300 needs no additional external components. However, depending on the entire system design and board layout, additional components may be required (see figure 1).

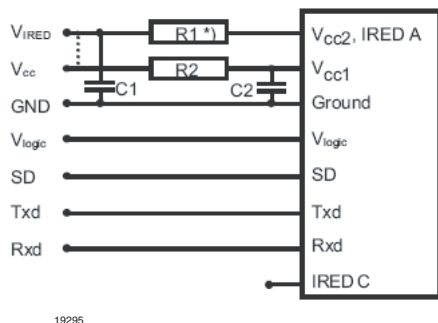


Figure 1. Recommended Application Circuit

\*) R1 is optional when reduced intensity is used

The capacitor C1 is buffering the supply voltage and eliminates the inductance of the power supply line. This one should be a Tantalum or other fast capacitor to guarantee the fast rise time of the IRED current. The resistor R1 is the current limiting resistor, which may be used to reduce the operating current to levels below the specified controlled values for saving battery power.

Vishay's transceivers integrate a sensitive receiver and a built-in power driver. The combination of both needs a careful circuit board layout. The use of thin, long, resistive and inductive wiring should be avoided. The shutdown input must be grounded for normal operation, also when the shutdown function is not used.

**Table 1.**  
**Recommended Application Circuit Components**

Component	Recommended Value	Vishay Part Number
C1	4.7 $\mu$ F, 16 V	293D 475X9 016B
C2	0.1 $\mu$ F Ceramic	VJ 1206 Y 104 J XXMT
R1	depends on current to be adjusted	
R2	47 $\Omega$ , 0.125 W	CRCW-1206-47R0-F-RT1

The inputs (TXD, SD) and the output RXD should be directly connected (DC - coupled) to the I/O circuit. The capacitor C2 combined with the resistor R2 is the low pass filter for smoothing the supply voltage. R2, C1 and C2 are optional and dependent on the quality of the supply voltages VCC1 and injected noise. An unstable power supply with dropping voltage during transmission may reduce the sensitivity (and transmission range) of the transceiver.

The placement of these parts is critical. It is strongly recommended to position C2 as close as possible to the transceiver pins.

When extended wiring is used as in bench tests the inductance of the power supply can cause dynamically a voltage drop at VCC2. Often some power supplies are not able to follow the fast current rise time. In that case another 4.7 $\mu$ F (type, see table under C1) at VCC2 will be helpful.

Under extrem EMI conditions as placing an RF-transmitter antenna on top of the transceiver, we recommend to protect all inputs by a low-pass filter, as a minimum a 12 pF capacitor, especially at the RXD port. The transceiver itself withstands EMI at a GSM frequencies above 500 V/m. When interference is observed, the wiring to the inputs picks it up. It is verified by DPI measurements that as long as the interfering RF-voltage is below the logic threshold levels of the inputs and equivalent levels at the outputs no interferences are expected.

One should keep in mind that basic RF - design rules for circuits design should be taken into account. Especially longer signal lines should not be used without termination. See e.g. "The Art of Electronics" Paul Horowitz, Winfield Hill, 1989, Cambridge University Press, ISBN: 0521370957.



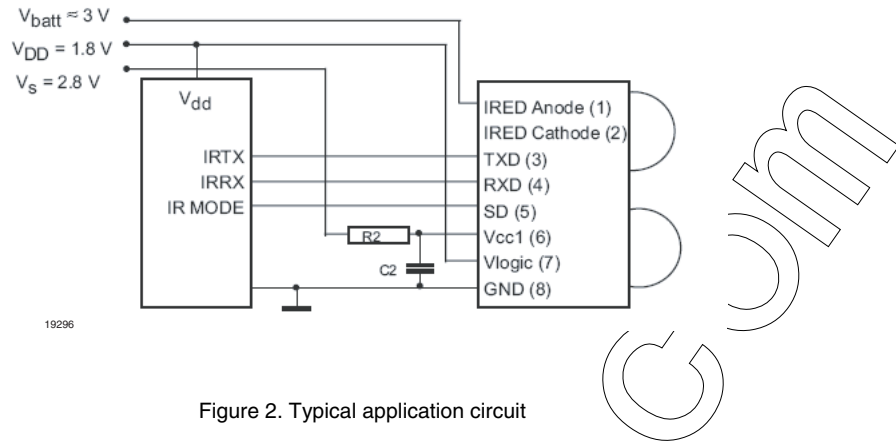


Figure 2. Typical application circuit

Figure 2 shows an example of a typical application for to work with low voltage logic (connected to  $V_{DD}$ ), a separate supply voltage  $V_S$  and using the transceiver with the IRED Anode connected to the unregulated battery  $V_{batt}$ . This method reduces the peak load of the regulated power supply and saves therefore costs. Alternatively all supplies can also be tied to only one voltage source. R1 and C1 are not used in this case and are depending on the circuit design in most cases not necessary.

### I/O and Software

In the description, already different I/Os are mentioned. Different combinations are tested and the function verified with the special drivers available from the I/O suppliers. In special cases refer to the I/O manual, the Vishay application notes, or contact directly Vishay Sales, Marketing or Application. For operating at RS232 ports the ENDEC TOIM4232 is recommended.

### Current Derating Diagram

Figure 3 shows the maximum operating temperature when the device is operated without external current limiting resistor.

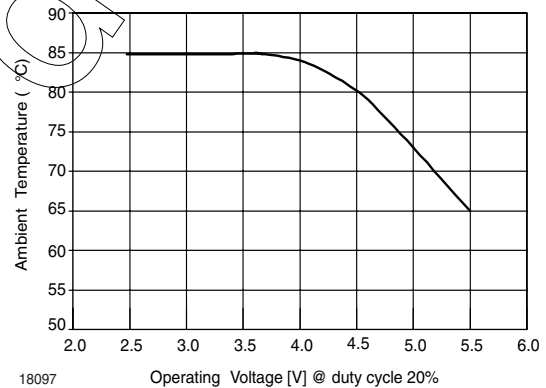


Figure 3. Current Derating Diagram

**Table 2. Truth table**

Inputs			Outputs		Remark
SD	Txd	Optical input Irradiance mW/m <sup>2</sup>	Rxd	Transmitter	Operation
high > 1 ms	x	x	weakly pulled (500 kΩ) to V <sub>CC1</sub>	0	Shutdown
low	high	x	high inactive	I <sub>e</sub>	Transmitting
low	high > 50 μs	x	high inactive	0	Protection is active
low	low	< 4	high inactive	0	Ignoring low signals below the IrDA <sup>®</sup> defined threshold for noise immunity
low	low	> Min. irradiance E <sub>e</sub> < Max. irradiance E <sub>e</sub>	low (active)	0	Response to an IrDA <sup>®</sup> compliant optical input signal
low	low	> Max. Irradiance E <sub>e</sub>	undefined	0	Overload conditions can cause unexpected outputs

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## Recommended Solder Profiles for TFDU4100

### Solder Profile for Sn/Pb soldering

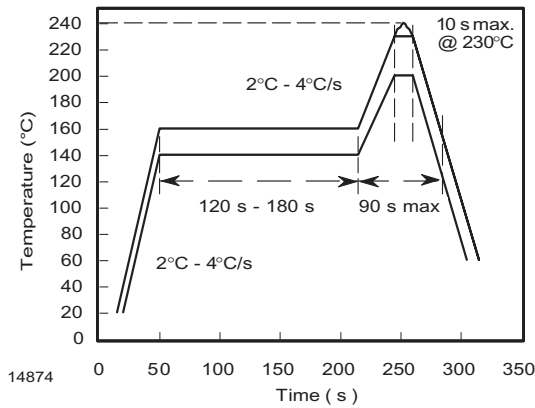


Figure 4. Recommended Solder Profile for Sn/Pb soldering

### Lead-Free, Recommended Solder Profile

The TFDU4300 is a lead-free transceiver and qualified for lead-free processing. For lead-free solder paste like  $\text{Sn}_{(3.0 - 4.0)}\text{Ag}_{(0.5 - 0.9)}\text{Cu}$ , there are two standard reflow profiles: Ramp-Soak-Spike (RSS) and Ramp-To-Spike (RTS). The Ramp-Soak-Spike profile was developed primarily for reflow ovens heated by infrared radiation. With widespread use of forced convection reflow ovens the Ramp-To-Spike profile is used increasingly. Shown below in figure 5 is Vishay's recommended profile for use with the TFDU4300 transceivers. For more details please refer to Application note: [SMD Assembly Instruction](#).

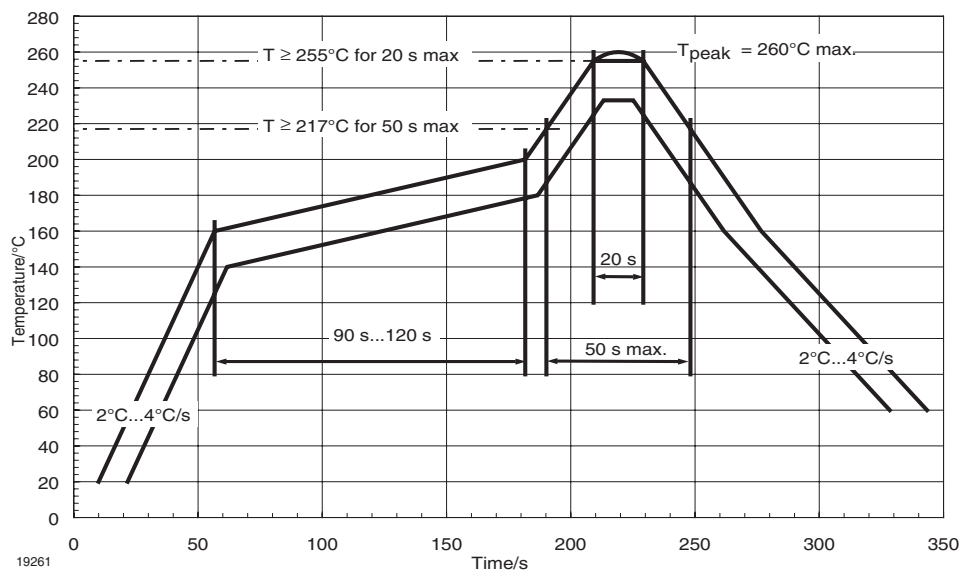


Figure 5. Solder Profile, RSS Recommendation

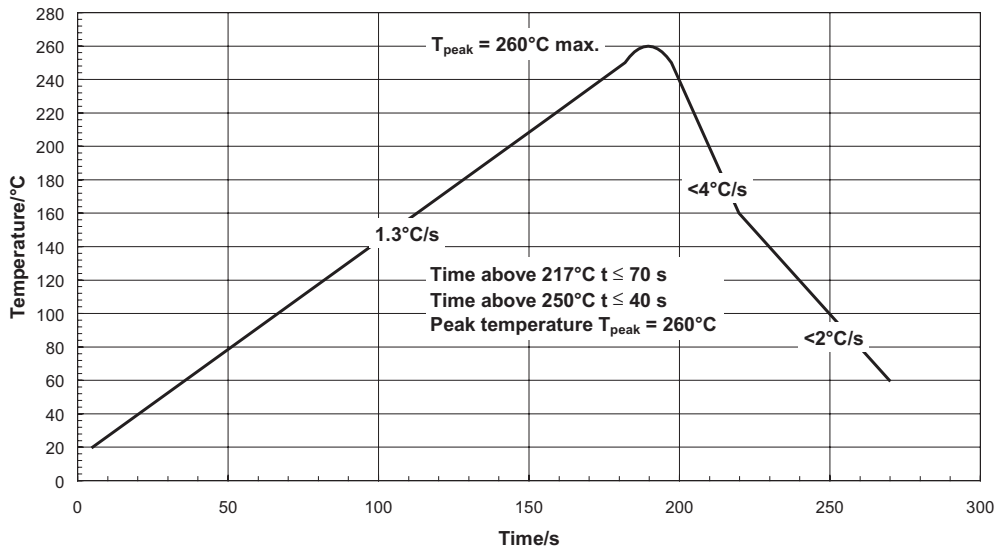
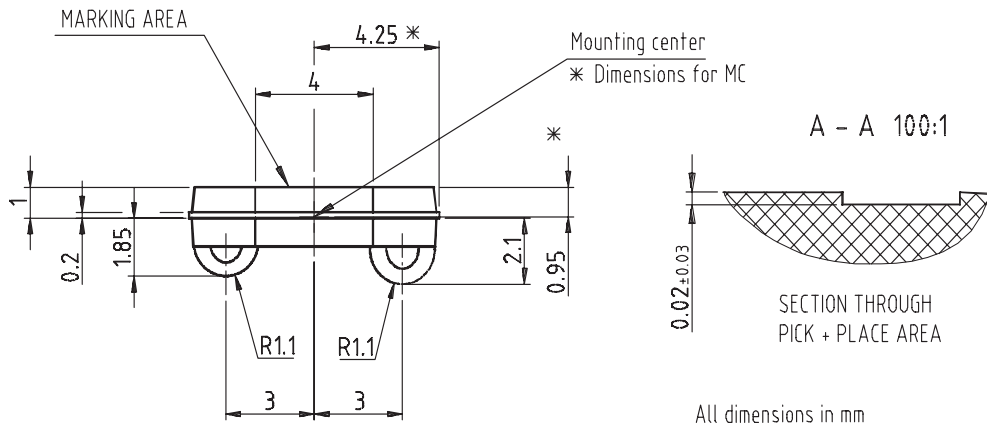
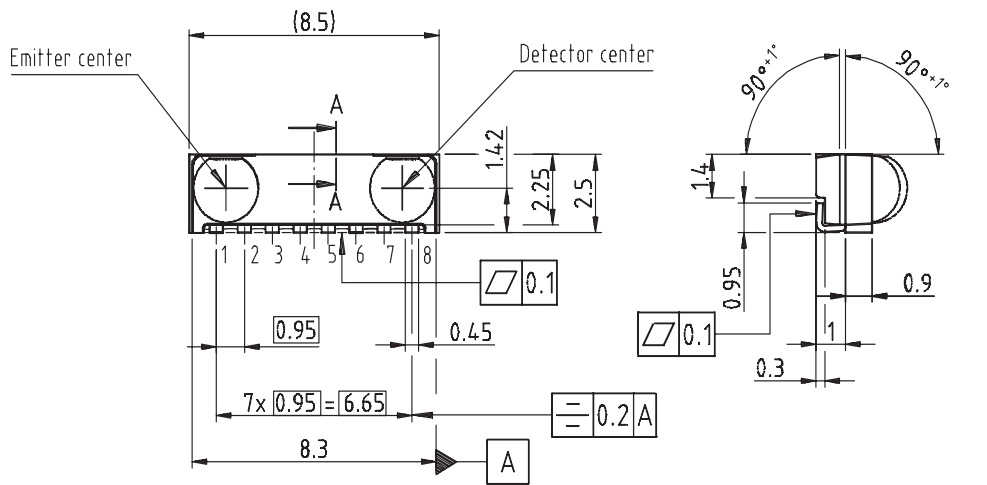


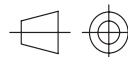
Figure 6. Solder Profile, RTS Recommendation

A ramp-up rate less than  $0.9^{\circ}\text{C/s}$  is not recommended. Ramp-up rates faster than  $1.3^{\circ}\text{C/s}$  damage an optical part because the thermal conductivity is less than compared to a standard IC.

## Package Dimensions in mm



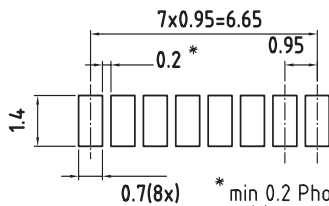
All dimensions in mm



technical drawings according to DIN specifications

Drawing-No.: 6.550-5252.01-4

Issue: 1; 17.01.03

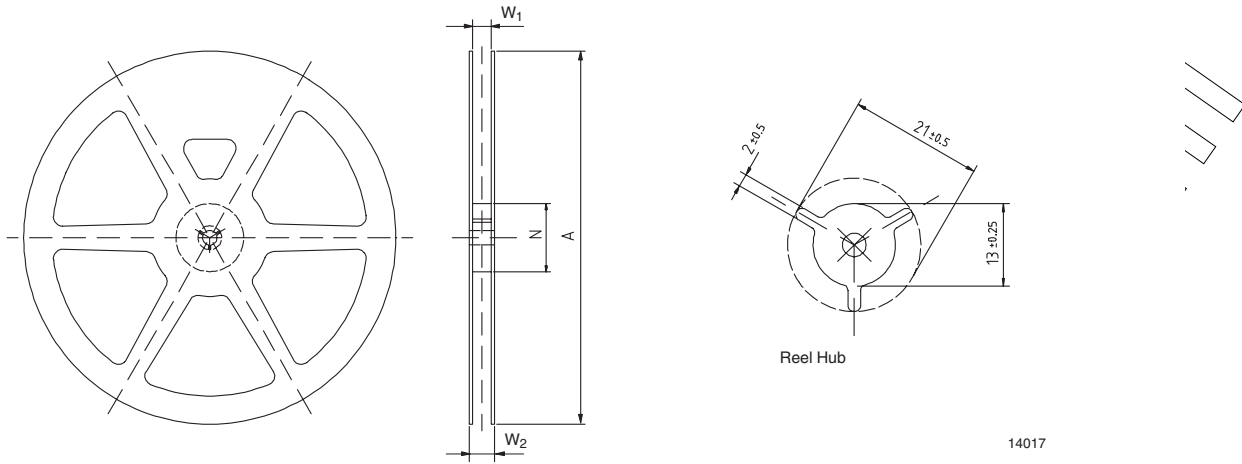


\* min 0.2 Photoimageable solder mask recommended between pads to prevent bridging

18100

W L

## Reel Dimensions

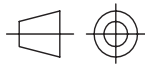


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Tape Width	A max.	N	W <sub>1</sub> min.	W <sub>2</sub> max.	W <sub>3</sub> min.	W <sub>3</sub> max.
mm	mm	mm	mm	mm	mm	mm
16	180	60	16.4	22.4	15.9	19.4
16	330	50	16.4	22.4	15.9	19.4

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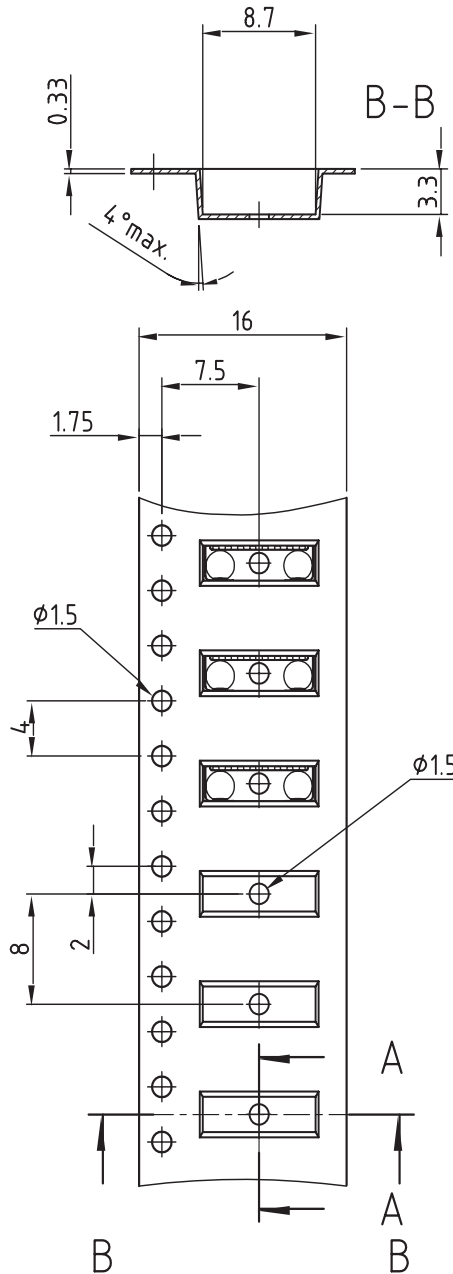
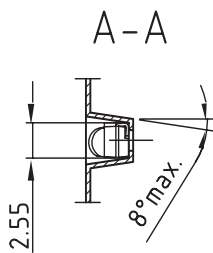
## Tape Dimensions in mm



technical drawings  
according to DIN  
specifications

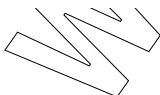
All dimensions in mm

Progressive direction ↑

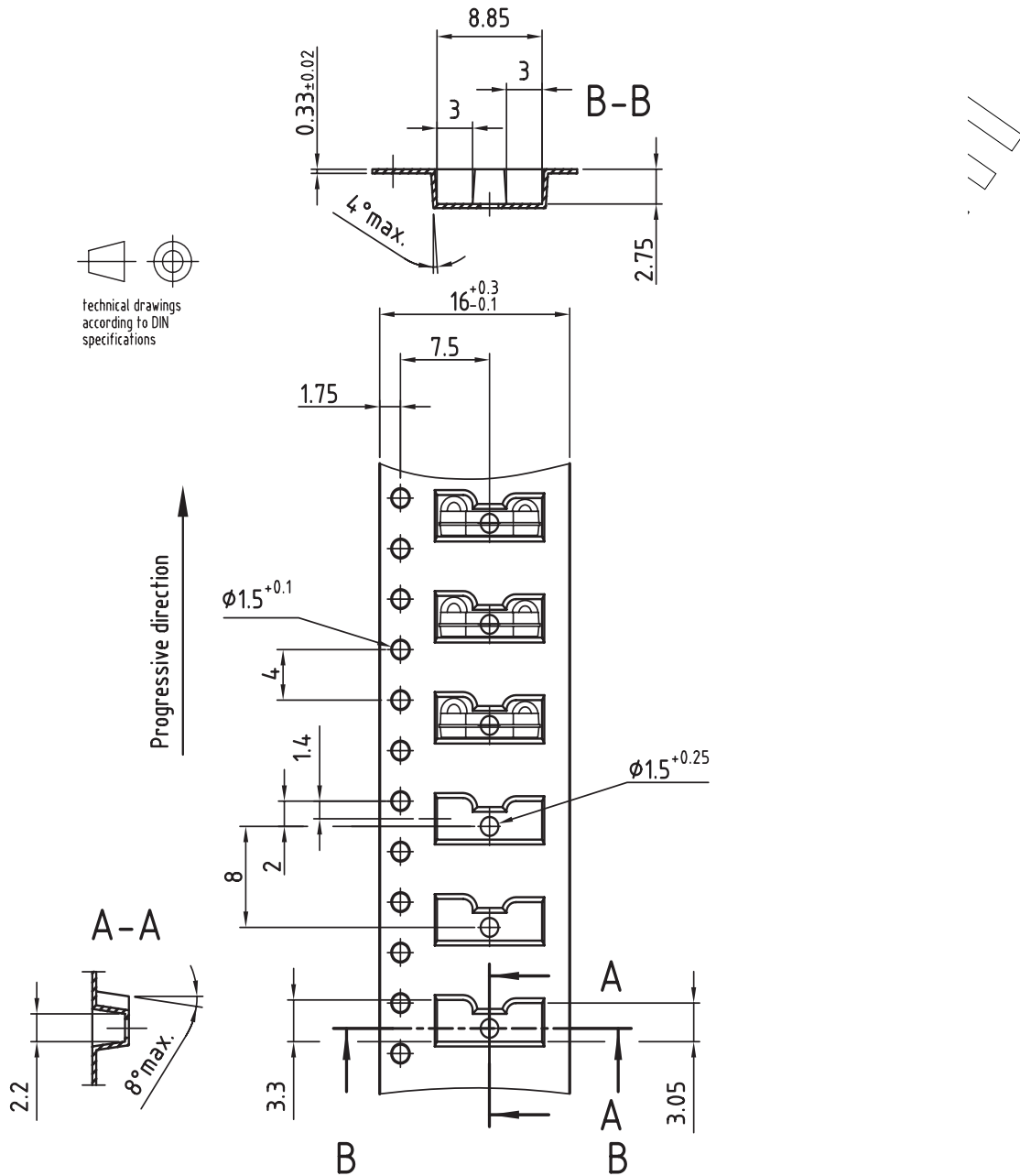


Drawing-No.: 9.700-5280.01-4

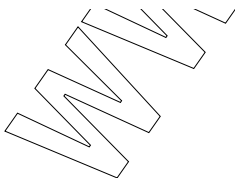
Issue: 1; 03.11.03



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## Ozone Depleting Substances Policy Statement

It is the policy of Vishay Semiconductor GmbH to

1. Meet all present and future national and international statutory requirements.
2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

Vishay Semiconductor GmbH has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively
2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA
3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

Vishay Semiconductor GmbH can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

We reserve the right to make changes to improve technical design and may do so without further notice.

Parameters can vary in different applications. All operating parameters must be validated for each customer application by the customer. Should the buyer use Vishay Semiconductors products for any unintended or unauthorized application, the buyer shall indemnify Vishay Semiconductors against all claims, costs, damages, and expenses, arising out of, directly or indirectly, any claim of personal damage, injury or death associated with such unintended or unauthorized use.

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