OV7635 Color CMOS VGA (640 x 480) CAMERACHIP™
OV7135 B&W CMOS VGA (640 x 480) CAMERACHIP™

General Description

The OV7635 (color) and OV7135 (black and white) CMOS CAMERACHIPS™ are single-chip video/imaging camera devices designed to provide a high level of functionality in a single, small-footprint package. The devices incorporate a 640 x 480 image array capable of operating at up to 30 frames per second (fps). Proprietary sensor technology utilizes advanced algorithms to cancel Fixed Pattern Noise (FPN), eliminate smearing, and drastically reduce blooming. All required camera functions including exposure control, gamma, gain, white balance, color matrix, color saturation, hue control, windowing, and more, are programmable through the serial SCCB interface. The device can be programmed to provide image output in different 8-bit formats.

Features

- 326,688 pixels, 1/4" lens, VGA/QVGA format
- Wide dynamic range, anti-blooming, zero smearing
- Interlaced/Progressive scan
- 8-bit Data output formats:
  - YCbCr 4:2:2 ITU-656
  - RGB 4:2:2
  - RGB Raw Data
- Wide dynamic range, anti-blooming, zero smearing
- Electronic exposure/gain/white balance control
- Image quality controls - brightness, contrast, gamma, saturation, sharpness, windowing, hue, etc.
- Internal and external synchronization
- Line exposure option
- 3.3-Volt operation, low power dissipation
  - < 25 mA active power at 30 fps
  - < 10 µA in power-down mode
- Built-in Gamma correction (0.45/0.55/1.00)
- SCCB programmable:
  - Color saturation, brightness, hue, white balance, exposure time, gain, etc.

Ordering Information

Product	Package
OV07635-C02A (Color, VGA, QVGA)	CLCC-24
OV07135-C02A (B&W, VGA, QVGA)	CLCC-24

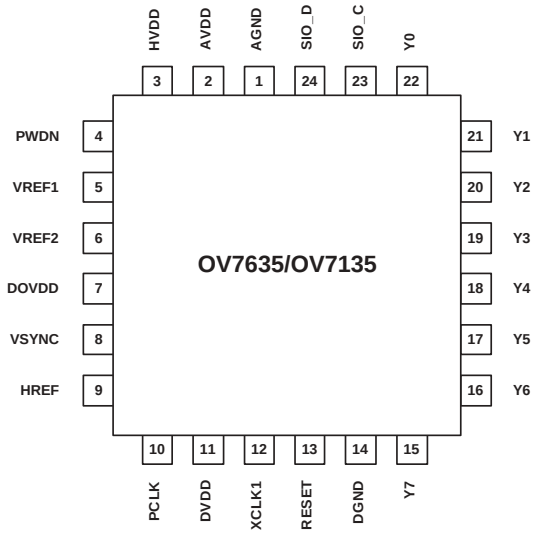
Applications

- Cellular and Picture Phones
- Toys
- PC Multimedia
- PDAs

Key Specifications

Array Size	**VGA**	640 x 480
	QVGA	320 x 240
Power Supply		3.3VDC ± 10%
Power Requirements	**Active**	< 25 mA
	Standby	< 10 µA
Electronics Exposure		Up to 648:1 (for selected fps)
Output Format		YCbCr 4:2:2, RGB 4:2:2 and RGB Raw Data
Lens Size		1/4"
Max. Image Transfer Rate	**VGA**	30 fps
	QVGA	60 fps
Min. Illumination (3000K)	**OV7635**	< 5 lux @ f1.2
	OV7135	< 0.8 lux @ f1.2
S/N Ratio		> 48 dB (AGC off, Gamma = 1)
Dynamic Range		> 72 dB
Scan Mode		Progressive or Interlaced
Gamma Correction		0.45/0.55/1.00
Pixel Size		5.6 µm x 5.6 µm
Dark Current		< 1.9 nA/cm^2
Fixed Pattern Noise		< 0.03% of $V_{PEAK-TO-PEAK}$
Image Area		3.6 mm x 2.7 mm
Package Dimensions		.400 in. x .400 in.

Figure 1 OV7635/OV7135 Pin Diagram



Functional Description

Figure 2 shows the functional block diagram of the OV7635/OV7135 image sensor. The OV7635/OV7135 includes:

- Image Sensor Array (664 x 492 resolution)
- Analog Signal Processor
- Dual 10-Bit Analog-to-Digital Converters
- Exposure Control
- White Balance Control
- Video Timing Generator
- SCCB Interface
- Video Output Ports
  - Digital Video Port
  - Zoom Video Port (ZV)

Figure 2 Functional Block Diagram

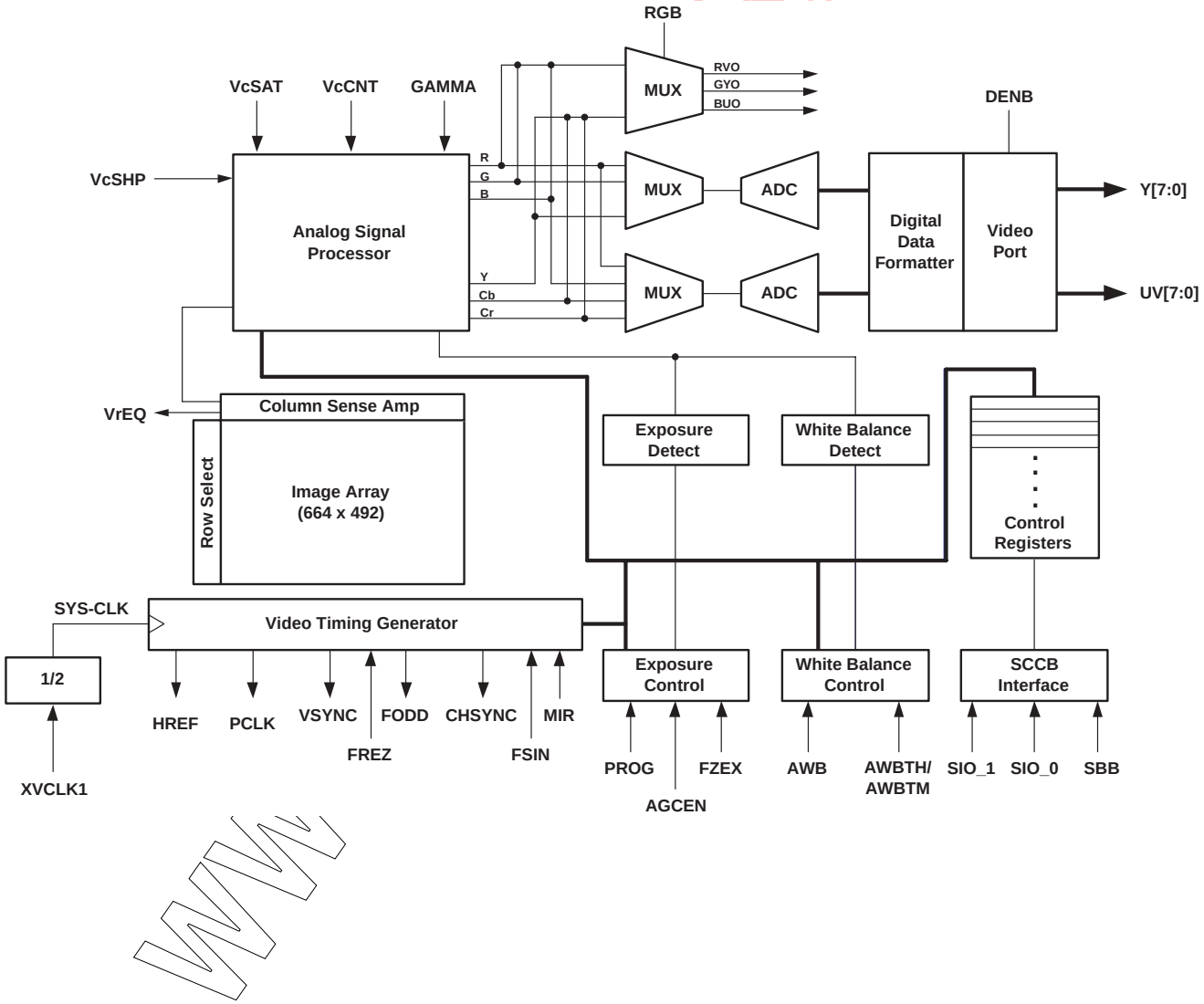
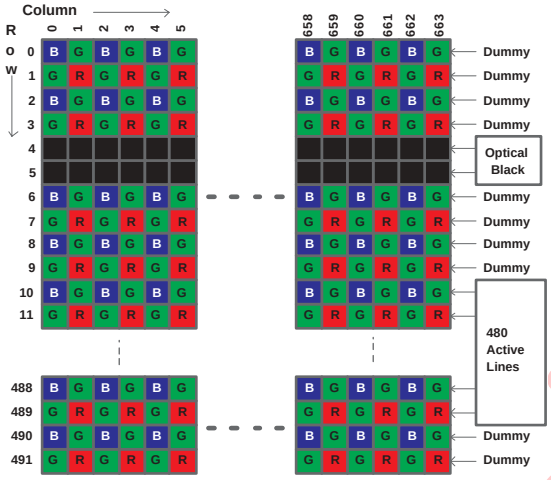


Image Sensor Array

The OV7635/OV7135 sensor is a 0.25" CMOS imaging device. The sensor contains approximately 326,688 pixels (664 x 492). Figure 3 shows the active regions of the sensor array.

Figure 3 Sensor Array Region



The color filters are Bayer pattern. The primary color BG/GR array is arranged in line-alternating fashion. Of the 326,688 pixels 307,200 are active. The other pixels are used for black level calibration and interpolation.

The sensor array design is based on a field integration read-out system with line-by-line transfer and an electronic shutter with a synchronous pixel read-out scheme.

When the column sample/hold circuit has sampled two rows of pixels, the pixel data will shift out one-by-one into an analog amplifier. The amplifier gain can either be programmed by the user or controlled by the internal automatic gain control circuit (AGC). The gain adjustment range is 0-24 dB.

Analog Signal Processor

The amplified signals are then routed to the analog processing section where the majority of signal processing occurs. Specifically, in the channel balance block, Red/Blue channel gain is increased or decreased to match Green channel luminance level. The adjustment range is 54 dB. This function can be done manually by the user or with the internal automatic white balance controller (AWB).

The analog processing block also contains the circuitry that performs color separation, color correction, automatic gain control (AGC), gamma correction, black level calibration, "knee" smoothing, aperture correction, controls for picture luminance and chrominance, and hue control for color. The analog video signals are based on the following formula:

Y = 0.59G + 0.31R + 0.11B
U = B - Y
V = R - Y

where R, G, B are the equivalent color components in each pixel.

YCbCr format is also supported, based on the formula below:

Y = 0.59G + 0.31R + 0.11B
Cr = 0.713 (R - Y)
Cb = 0.564 (B - Y)

Dual 10-Bit Analog-to-Digital Converters

The YCbCr/RGB data signal from the analog processing section is fed to two on-chip 10-bit analog-to-digital (A/D) converters: one for the Y/G channel and one shared by the CbCr/BR channels. The converted data stream is further conditioned in the digital formatter. The processed signal is delivered to the digital video port through the video multiplexer which routes the user-selected 8-, or 4-bit video data to the correct output pins.

The on-chip 10-bit A/D operates at up to 12 MHz, and is fully synchronous to the pixel rate. Actual conversion rate is related to the frame rate. A/D black-level calibration circuitry ensures:

- Black level of Y/RGB is normalized to a value of 16
- Peak white level is limited to 240
- CbCr black level is 128
- CbCr Peak/bottom is 240/16
- RGB raw data output range is 16/240

Note: Values 0 and 255 are reserved for sync flag.

Exposure Control

The algorithm used for the electronic exposure control is based on the brightness of the full image. The exposure is optimized for a "normal" scene that assumes the subject is well lit relative to the background. In situations where the image is not well lit, the automatic exposure control (AEC) white/black ratio may be adjusted to suit the needs of the application.

Additional CAMERACHIP functions include:

- AGC that provides a gain boost of up to 24 dB
- White balance control that enables setting of proper color temperature and can be programmed for automatic or manual operation
- Separate saturation, brightness, hue, and sharpness adjustments allow for further fine-tuning of the picture quality and characteristics

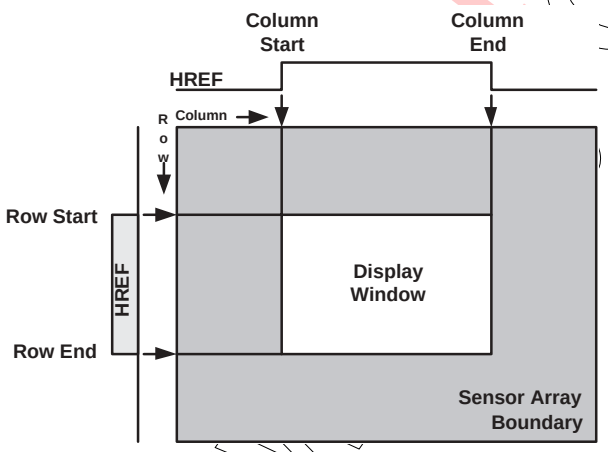
White Balance Control

The OV7635/OV7135 CAMERACHIP also provides control over the White Balance ratio for increasing/decreasing the image field Red/Blue component ratio. The sensor provides a default setting sufficient for most applications.

Windowing

The windowing feature of the OV7635/OV7135 CAMERACHIPS allows user-definable window sizing as required by the application. Window size setting (in pixels) ranges from 4 x 2 to 640 x 480, and can be positioned anywhere inside the 664 x 492 boundary. Note that modifying window size and/or position does not change frame or data rate. The OV7635 CAMERACHIP alters the assertion of the HREF signal to be consistent with the programmed horizontal and vertical region. The default output window is 640 x 480. See Figure 4 for details

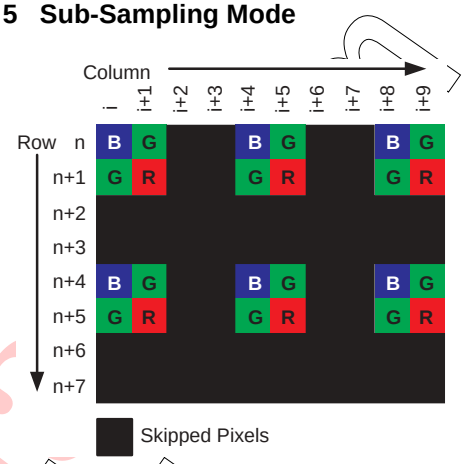
Figure 4 Windowing



Sub-sampling Mode

The OV7635/OV7135 can be programmed to output in 320 x 240 (QVGA) images. This mode is available for applications where higher resolution image capture is not required. Default resolution is 640 x 480 pixels. The entire array is sub-sampled for maximal image quality. Only half of the pixel rate is required when programmed in this mode. Both horizontal and vertical pixels are sub-sampled to an aspect ratio of 4:2 as illustrated in Figure 5.

Figure 5 Sub-Sampling Mode



Video Timing Generator

In general, the timing generator controls the following functions:

- Frame Rate Adjust
- Frame Division
- Frame Rate Timing

Frame Rate Adjust

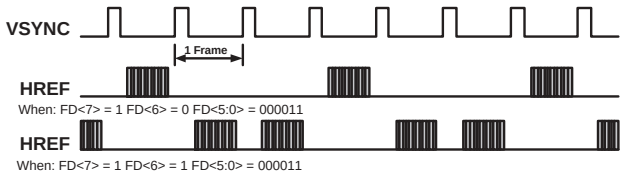
OV7635/OV7135 offers two methods of frame rate adjustment.

1. Clock prescaler (see "CLKRC" on page 22)
   By changing the system clock divide ratio, the frame rate and pixel rate will change together. This method can be used for dividing the frame/pixel rate by: 1/2, 1/3, 1/4 … 1/64 of the input clock rate.
2. Line adjustment (see "FRARH" on page 31 and see "FRARL" on page 31)
   By adding dummy pixel timing in each line, the frame rate can be changed while leaving the pixel rate as is.

Frame Division

The OV7635/OV7135 frame rate divider can divide live video output into a programmed number of time slots in units of frames. The frame divider does not alter the video data rate. Figure 6 illustrates the operation of the frame rate divider. Refer to register FSD (see "FSD" on page 25) for details on setting the divider.

Figure 6 Frame Division Example



Frame Rate Timing

Default frame timing is illustrated in Figure 13 and Figure 14. Refer to Table 1 for the actual pixel rate at different frame rates.

Table 1 Frame and Pixel Rates

Frame Rage (fps)	15	10	7.5	6	5
PCLK (MHz)	24	16	12	9.6	8
NOTE: Based on 24 MHz external clock and internal PLL on, frame rate is adjusted by the main clock divide method.					

Slave Operation Mode

The OV7635/OV7135 can be programmed to operate in slave mode (default is master mode).

When used as a slave device, the OV7635/OV7135 changes the HSYNC and VSYNC outputs to input pins for use as horizontal and vertical synchronization input triggers supplied by the master device. The master device must provide the following signals:

1. System clock MCLK to XCLK1 pin
2. Horizontal sync MHSYNC to CHSYNC pin
3. Vertical frame sync MVSYNC to VSYNC pin

See Figure 7 for slave mode connections and Figure 8 for detailed timing considerations.

Figure 7 Slave Mode Connection

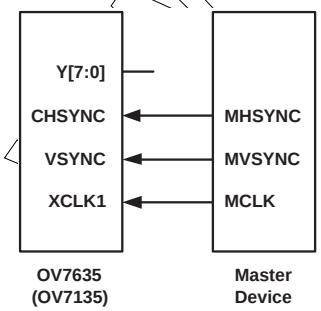
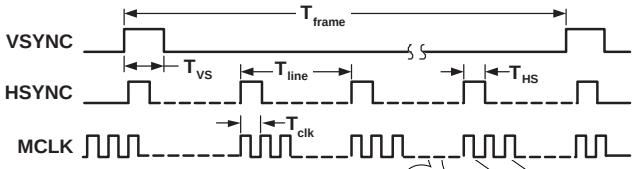


Figure 8 Slave Mode Timing



NOTE:

1) $T_{HS} > 6\ T_{clk}$, $Tvs > T_{line}$
2) $T_{line} = 1520 \times T_{clk}$ (SXGA); $T_{line} = 800 \times T_{clk}$ (VGA)
3) $T_{frame} = 1050 \times T_{line}$ (SXGA); $T_{frame} = 500 \times T_{line}$ (VGA)

Luminance Average Calculator

The OV7635/OV7135 provides frame-averaged luminance level. Access to the data is via the serial control port. Average values are calculated from 128 pixels per line (64 in VGA).

Reset

The OV7635/OV7135 includes a RESET pin (pin 13 - see "RESET" on page 11) that forces a complete hardware reset when it is pulled high (VCC). The OV7635/OV7135 clears all registers and resets them to their default values when a hardware reset occurs. Reset can also be initiated through the SCCB interface.

Power-Down Mode

Two methods are available to place the OV7635/OV7135 into power-down mode: hardware power-down and SCCB software power-down.

To initiate hardware power-down, the PWDN pin (pin 4 - see "PWDN" on page 11) must be tied to high (+3.3 VDC). When this occurs, the OV7635 internal device clock is halted and all internal counters are reset. The current draw is less than 10 µA in this standby mode.

Executing a software power-down through the SCCB interface suspends internal circuit activity, but does not halt the device clock. The current requirements drop to less than 1mA in this mode.

SCCB Interface

The OV7635/OV7135 provides an on-chip SCCB serial control port that allows access to all internal registers, for complete control and monitoring of the OV7635/OV7135 operation.

Refer to *OmniVision Technologies SCCB (Serial Camera Control Bus) Specification* for detailed usage of the serial control port.

Video Output Ports

The OV7635/OV7135 has the following ports:

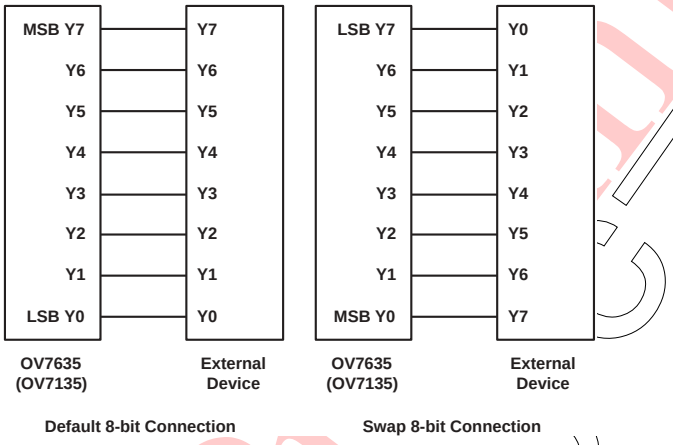
- Digital Video Port
- Zoom Video Port (ZV)

Digital Video Port

MSB/LSB Swap

The OV7635/OV7135 has an 8-bit digital video port. The MSB and LSB can be swapped with the control registers. Figure 9 shows some examples of connections with external devices.

Figure 9 Connection Examples



Line/Pixel Timing

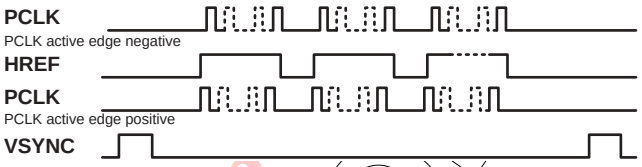
The OV7635/OV7135 digital video port can be programmed to work in either master or slave mode.

In both master and slave modes, pixel data output is synchronous with PCLK (or MCLK if port is a slave), HREF and VSYNC. The default PCLK edge for valid data is the negative edge but may be programmed with register COMD[6] (see "COMD" on page 24) for the positive edge.

Basic line/pixel output timing is illustrated in Figure 11 and Figure 12.

To minimize image capture circuitry and conserve memory space, PCLK output can be programmed with register COMJ[6] (see "COMJ" on page 35) to be gated by the active video period as defined by the HREF signal. See Figure 10 for illustration.

Figure 10 PCLK Output Only at Valid Pixels



Pixel Output Pattern

Table 2 shows the output data order from the OV7635/OV7135. The data output sequence following the first HREF and after VSYNC is: $B_{0,0}$ $G_{0,1}$ $B_{0,2}$ $G_{0,3}$... $B_{0,648}$ $G_{0,649}$. After the second HREF the output is $G_{1,0}$ $R_{1,1}$ $G_{1,2}$ $R_{1,3}$... $G_{1,648}$ $R_{1,649}$..., etc. If the OV7635/OV7135 is programmed to output VGA resolution data, horizontal and vertical sub-sampling will occur. The default output sequence for the first line of output will be: $B_{0,0}$ $G_{0,1}$ $B_{0,4}$ $G_{0,5}$... $B_{0,646}$ $G_{0,647}$,. The second line of output will be: $G_{1,0}$ $R_{1,1}$ $G_{1,4}$ $R_{1,5}$... $G_{1,646}$ $R_{1,647}$.

Table 2 Data Pattern

R/C	0	1	2	3	. . .	648	649
0	$B_{0,0}$	$G_{0,1}$	$B_{0,2}$	$G_{0,3}$	. . .	$B_{0,648}$	$G_{0,649}$
1	$G_{1,0}$	$R_{1,1}$	$G_{1,2}$	$R_{1,3}$	. . .	$G_{1,648}$	$R_{1,649}$
2	$B_{2,0}$	G_2	$B_{2,2}$	$G_{2,3}$	. . .	$B_{2,648}$	$G_{2,649}$
3	$G_{3,0}$	$R_{3,1}$	$G_{3,2}$	$R_{3,3}$	. . .	$G_{3,648}$	$R_{3,649}$
. .					. .		
482	$B_{482,0}$	$G_{482,1}$	$B_{482,2}$	$G_{482,3}$		$B_{482,648}$	$G_{482,649}$
483	$G_{483,0}$	$R_{483,1}$	$G_{483,2}$	$R_{483,3}$		$G_{483,648}$	$R_{483,649}$

Zoom Video Port (ZV)

The ZV port is a single-source unidirectional video bus between a PC Card socket and a VGA controller. The ZV port complies with ITU601 timing to allow NTSC decoders to deliver real-time digital video straight into the VGA frame buffer from a PC Card. The OV7635/OV7135 supports standard ZV port interface timing. Signals available include VSYNC, CHSYNC, PCLK and 16-bit data bus: Y[7:0] and UV[7:0]. The rising edge of PCLK clocks data into the ZV port. See Figure 17 for details.

Video Output Formats

The video output port of the OV7635/OV7135 CAMERACHIP provides a number of output format/standard options to suit many different application requirements. Table 3 lists the available output formats. These formats are user-programmable through the SCCB interface.

ITU-601

The OV7635 offers a 16-bit 4:2:2 format which complies with the 60 Hz ITU-601 timing standard. Output is 8-bit in RGB ITU-656 format. Start of Active Video (SAV) and End of Active Video (EAV) are inserted at the beginning and ending of HREF, which synchronize the acquisition of VSYNC and HSYNC. 8-bit data bus configuration (without VSYNC and CHSYNC) can provide timing and data in this format.

ITU-656

In RGB raw data ITU-656 mode, the OV7635/OV7135 asserts SAV and EAV to indicate the beginning and the ending of HREF window. As a result, SAV and EAV change with the active pixel window. 8-bit RGB raw data is also available without SAV and EAV encoding.

YUV

The OV7635 CAMERACHIP offers flexibility in YUV output format. The CAMERACHIP may be programmed as standard YUV 4:2:2. It may also be configured to "swap" the UV channel output sequence. When swapped, the output sequence becomes:

- V Y U Y··· for the 8-bit configuration
- V U V U ··· for the 16-bit configuration

Another swap format available only in the 8-bit configuration is the Y/UV sequence swap:

- Y U Y V···

For YUV output, refer to Table 4, Table 5, Table 6, Table 7, Table 8, and Figure 15.

RGB Raw Data Output

The OV7635/OV7135 also supports two RGB raw data output formats: RGB progressive scan mode and RGB single-line output. The pixel pattern is shown in Table 9.

RGB Raw Data Progressive Scan Mode

The OV7635/OV7135 outputs each line twice for each frame. Each horizontal SYNC outputs two lines of data. The output clock rate will be double the rate of the pixel clock. The sequence for the output is BGRG...

- RGB full resolution progressive scan mode (total 492 HREFs)
  - First HREF Y channel output unstable data
  - Second HREF Y channel output $B_{11}G_{21}$ R_{22} G_{12} $B_{13}G_{23}$ R_{24} G_{14} ...
  - Third HREF Y channel output B_{31} G_{21} R_{22} G_{32} B_{33} G_{23} R_{24} G_{34} ...
  - Every line of data is output twice for each frame.
  - PCLK is double
- RGB QVGA resolution progressive scan mode (total 246 HREFs)
  - First HREF Y channel output $B_{11}G_{21}$ R_{22} G_{12} $B_{15}G_{25}$ R_{26} G_{16} ...
  - Second HREF Y channel output $B_{31}G_{41}$ R_{42} G_{32} $B_{35}G_{45}$ R_{46} G_{36}...
  - Third HREF Y channel output B_{51} G_{61} R_{62} G_{52} B_{55} G_{65} R_{66} G_{56} ...
  - Every line of data is output once for each frame.
  - Max frame rate is 60 fps
- RGB full resolution raw data single-line format (total 492 HREFs)
  - First HREF Y channel output B_{11} G_{12} B_{13} G_{14} ...
  - Second HREF Y channel output G_{21} R_{22} G_{23} R_{24} ...
  - Third HREF Y channel output B_{31} G_{32} B_{33} G_{34} ...
  - PCLK rising edge latches data bus.
- RGB QVGA resolution raw data single-line format (total 246 HREFs)
  - First HREF Y channel output B_{11} G_{12} B_{15} G_{16} ...
  - Second HREF Y channel output G_{21} R_{22} G_{25} R_{26} ...
  - Third HREF Y channel output B_{51} G_{52} B_{55} G_{56} ...
  - Third HREF Y channel output G_{61} R_{62} G_{65} R_{66} ...
  - PCLK rising edge latches data bus

RGB Raw Data Single-Line Output

The OV7635/OV7135 supports single-line output, also known as one-line format. The sequence is BGBG for even lines and GRGR for odd lines. This format exactly matches the Bayer pattern color filter in the sensor array. See Table 9 for further details.

For RGB output, the OV7635/OV7135 CAMERACHIP also offers some format swaps:

- Device may be configured to "swap" the BR sequence, meaning the sequence is R G B G··· rather than BGRG ···
- Another swap format available is when the Y/UV sequence is swapped, meaning the sequence is GBGR···

B&W Output

The CAMERACHIP can be configured for use as a black and white imaging device. The vertical resolution is higher than in color mode. Video data output is provided at the Y port.

The MSB and LSB of Y/UV or RGB output can be reversed. Y[7] is MSB and Y[0] is LSB in the default setting. Y[7] becomes LSB and Y[0] becomes MSB in the reverse order configuration. Y[6:2] is also reversed appropriately.

Table 3 Digital Output Formats

Resolution	Pixel Clock	Interlaced		Progressive	
		600 x 480 (VGA)	320 x 240 (QVGA)	640 x 480 (VGA)	320 x 240 (QVGA)
YUV	16-bit	Y	Y	Y	Y
	ITU-601	Y	Y	Y	Y
	8-bit	Y	Y	Y	Y
	ITU-656	Y	Y	Y	Y
RGB	16-bit	Y	Y	Y	Y
	ITU-601	Y	Y	Y	Y
	8-bit	Y	Y	Y	Y
	ITU-656	Y	Y	Y	Y
Y/UV Swap	16-bit				
	8-bit	Y	Y	Y	Y
U/V Swap	YUV	Y	Y	Y	Y
	RGB	Y	Y	Y	Y
YG	16-bit	Y	Y	Y	Y
	8-bit				
Single-Line RGB Raw Data	16-bit			Y	
	8-bit				
MSB/LSB Swap	16-bit	Y	Y	Y	Y
	8-bit	Y	Y	Y	Y
B&W		Y	Y	Y	Y
Digital Video Port		Y	Y	Y	Y
ZV Port Interface		Y	Y	Y	Y

Note: "Y" indicates mode/combination is supported by the OV7635/OV7135.

Table 4 4:2:2 8-bit Format

Data Bus	Pixel Byte Sequence							
Y7	U7	Y7	V7	Y7	U7	Y7	V7	Y7
Y6	U6	Y6	V6	Y6	U6	Y6	V6	Y6
Y5	U5	Y5	V5	Y5	U5	Y5	V5	Y5
Y4	U4	Y4	V4	Y4	U4	Y4	V4	Y4
Y3	U3	Y3	V3	Y3	U3	Y3	V3	Y3
Y2	U2	Y2	V2	Y2	U2	Y2	V2	Y2
Y1	U1	Y1	V1	Y1	U1	Y1	V1	Y1
Y0	U0	Y0	V0	Y0	U0	Y0	V0	Y0
Y Frame	0		1		2		3	
UV Frame	0 1				2 3			

Table 5 4:2:2 16-bit Format

Data Bus	Pixel Byte Sequence					
Y7	Y7	Y7	Y7	Y7	Y7	Y7
Y6	Y6	Y6	Y6	Y6	Y6	Y6
Y5	Y5	Y5	Y5	Y5	Y5	Y5
Y4	Y4	Y4	Y4	Y4	Y4	Y4
Y3	Y3	Y3	Y3	Y3	Y3	Y3
Y2	Y2	Y2	Y2	Y2	Y2	Y2
Y1	Y1	Y1	Y1	Y1	Y1	Y1
Y0	Y0	Y0	Y0	Y0	Y0	Y0
UV7	UV7	UV7	UV7	UV7	UV7	UV7
UV6	UV6	UV6	UV6	UV6	UV6	UV6
UV5	UV5	UV5	UV5	UV5	UV5	UV5
UV4	UV4	UV4	UV4	UV4	UV4	UV4
UV3	UV3	UV3	UV3	UV3	UV3	UV3
UV2	UV2	UV2	UV2	UV2	UV2	UV2
UV1	UV1	UV1	UV1	UV1	UV1	UV1
UV0	UV0	UV0	UV0	UV0	UV0	UV0
Y Frame	0	1	2	3	4	5
UV Frame	0 1		2 3		4 5	

Table 6 shows the default Y/UV channel output port relationship before an MSB/LSB swap.

Table 6 Default Output Sequence

	MSB							LSB
Output port	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
Internal output data	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

Table 7 and Table 8 shows the relationship after an MSB/LSB swap changes.

Table 7 Swapped MSB/LSB Output Sequence

	MSB							LSB
Output port	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
Internal output data	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7

Table 8 QVGA Digital Output Format (YUV Beginning-of-Line)

Pixel No.	1	2	3	4	5	6	7	8
Y	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
UV	U0, V0	U1, V1	U2, V2	U3, V3	U4, V4	U5, V5	U6, V6	U7, V7

Y channel output U2Y2V3 Y3U6 Y6V7 Y7 U10Y10 V11Y11...
Every other pixel (total 400 pixels) and every other line (total 300 lines) is output in each frame.

Table 9 RGB Raw Data Format

R/C	1	2	3	4	. . .	641	642	643	644
1	$B_{1,1}$	$G_{1,2}$	$B_{1,3}$	$G_{1,4}$	. . .	$B_{1,641}$	$G_{1,642}$	$B_{1,643}$	$G_{1,644}$
2	$G_{2,1}$	$R_{2,2}$	$G_{2,3}$	$R_{2,4}$	. . .	$G_{2,641}$	$R_{2,642}$	$G_{2,643}$	$R_{2,644}$
3	$B_{3,1}$	$G_{3,2}$	$B_{3,3}$	$G_{3,4}$	. . .	$B_{3,641}$	$G_{3,642}$	$B_{3,643}$	$G_{3,644}$
4	$G_{4,1}$	$R_{4,2}$	$G_{4,3}$	$R_{4,4}$	. . .	$G_{4,641}$	$R_{4,642}$	$G_{4,643}$	$R_{4,644}$
491	$B_{491,1}$	$G_{491,2}$	$B_{491,3}$	$G_{491,4}$	. . .	$B_{491,641}$	$G_{491,642}$	$B_{491,643}$	$G_{491,644}$
492	$G_{492,1}$	$R_{492,2}$	$G_{492,3}$	$R_{492,4}$	. . .	$G_{492,641}$	$R_{492,642}$	$G_{492,643}$	$R_{492,644}$

Pin Description

Table 10 Pin Description

Pin Number	Name	Pin Type	Function/Description
01	AGND	Power	Analog ground
02	AVDD	Power	Analog power supply (+3.3 VDC)
03	HVDD	V_{REF} (4V)	Charge pump voltage - connect to ground using a 10 µF capacitor
04	PWDN	Function (default = 0)	Power-down Mode Selection 0: Normal mode 1: Power-down mode
05	VREF1	V_{REF} (1.5V)	Internal voltage reference - connect to ground using a 0.1 µF capacitor
06	VREF2	V_{REF} (2.7V)	Internal voltage reference - connect to ground using a 0.1 µF capacitor
07	DOVDD	Power	Power supply (+3.3 VDC) for digital output drive
08	VSYNC	Output	Vertical sync output
09	HREF	Output	HREF output
10	PCLK	Output	Pixel clock (PCLK) output
11	DVDD	Power	Digital power supply (+3.3 VDC)
12	XCLK1	Input	Crystal clock input
13	RESET	Function (default = 0)	Chip reset, active high
14	DGND	Power	Digital ground
15	Y7	Output	Y video component output bit[7]
16	Y6	Output	Y video component output bit[6]
17	Y5	Output	Y video component output bit[5]
18	Y4	Output	Y video component output bit[4]
19	Y3	Output	Y video component output bit[3]
20	Y2	Output	Y video component output bit[2]
21	Y1	Output	Y video component output bit[1]
22	Y0	Output	Y video component output bit[0]
23	SIO_C	Input	SCCB serial interface clock input
24	SIO_D	I/O	SCCB serial interface data I/O

Electrical Characteristics

Table 11 Operating Conditions

Parameter	Min	Max	Unit
Operating temperature	0	40	°C
Storage temperature	-40	125	°C
Operating humidity	TBD	TBD	
Storage humidity	TBD	TBD	

Table 12 DC Characteristics (0°C < T_A < 85°C, Voltages referenced to GND)

Symbol	Parameter	Min	Typ	Max	Unit
Supply					
V_{DD}	Supply voltage - internal analog (DEVDD, ADVDD, AVDD, SVDD, DVDD)	3.0	3.3	3.6	V
I_{DD1}	Supply current (V_{DD} = 3 V at 50 Hz frame rate without digital I/O loading)		30		mA
I_{DD2}	Standby supply current		5	15	µA
Digital Inputs					
V_{IL}	Input voltage LOW			0.8	V
V_{IH}	Input voltage HIGH	2			V
C_{IN}	Input capacitor			10	pF
Digital Outputs (standard loading 25 pF, 1.2 KΩ to 3 V)					
V_{OH}	Output voltage HIGH	2.4			V
V_{OL}	Output voltage LOW			0.6	V
SCCB Inputs					
V_{IL}	SIO_C and SIO_D	-0.5	0	1	V
V_{IH}	SIO_C and SIO_D	2.5	3	3.5	V

Table 13 AC Characteristics (T_A = 25°C, V_{DD} = 3V)

Symbol	Parameter	Min	Typ	Max	Unit
RGB/YCbCr Output					
I_{SO}	Maximum sourcing current		15		mA
V_Y	DC level at zero signal		1		V
	Y_{PP} 100% amplitude (without sync)		1		V
	Sync amplitude		0.3		V
ADC Parameters					
B	Analog bandwidth		TBD		MHz
Φ_{DIFF}					
DLE	DC differential linearity error		0.5		LSB
ILE	DC integral linearity error		0.5		LSB
	Settling time for hardware reset			<1	ms
	Settling time for software reset			<1	ms
	Settling time for VGA/XSGA mode change			<1	ms
	Settling time for register setting			<300	ms

Table 14 Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
Oscillator and Clock Input					
f_{OSC}	Frequency (XCLK1)	10	27	30	MHz
t_r, t_f	Clock input rise/fall time			5	ns
	Clock input duty cycle	45	50	55	%
SCCB Timing (400 Kbps) (see Figure 18)					
f_{SIO_C}	Clock Frequency			400	KHz
t_{LOW}	Clock Low Period	1.3			µs
t_{HIGH}	Clock High Period	600			ns
t_{AA}	SIO_C low to Data Out valid	100		900	ns
t_{BUF}	Bus free time before new START	1.3			µs
$t_{HD:STA}$	START condition Hold time	600			ns
$t_{SU:STA}$	START condition Setup time	600			ns
$t_{HD:DAT}$	Data-in Hold time	0			µs
$t_{SU:DAT}$	Data-in Setup time	100			ns
$t_{SU:STO}$	STOP condition Setup time	600			ns
t_{R}, t_{F}	SCCB Rise/Fall times			300	ns
t_{DH}	Data-out Hold time	50			ns
Digital Timing					
t_{PCLK}	PCLK cycle time — 16-bit operation	74			ns
	PCLK cycle time — 8-bit operation	37			ns
t_r, t_f	PCLK rise/fall time			15	ns
t_{PDD}	PCLK to data valid			15	ns
t_{PHD}	PCLK to HREF delay	0	5	20	ns

Timing Specifications

Figure 11 VGA Line/Pixel Output Timing

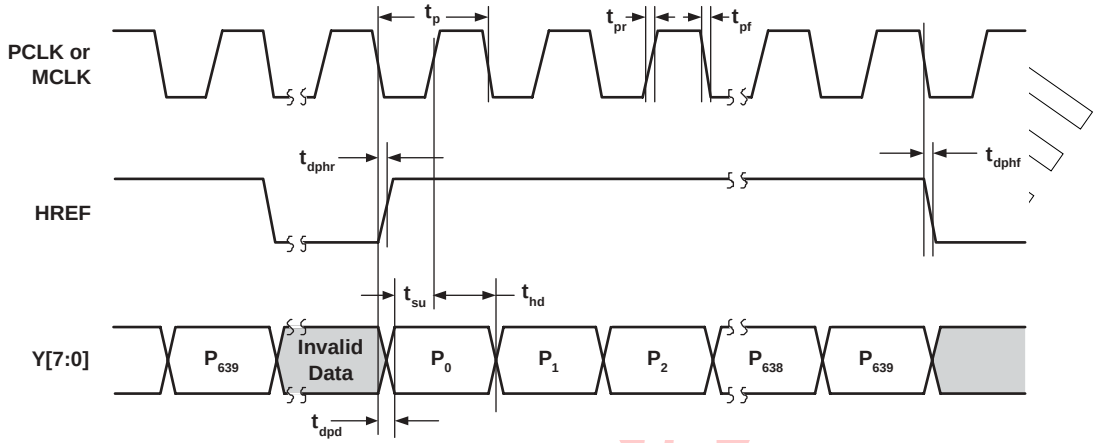


Figure 12 QVGA Line/Pixel Output Timing

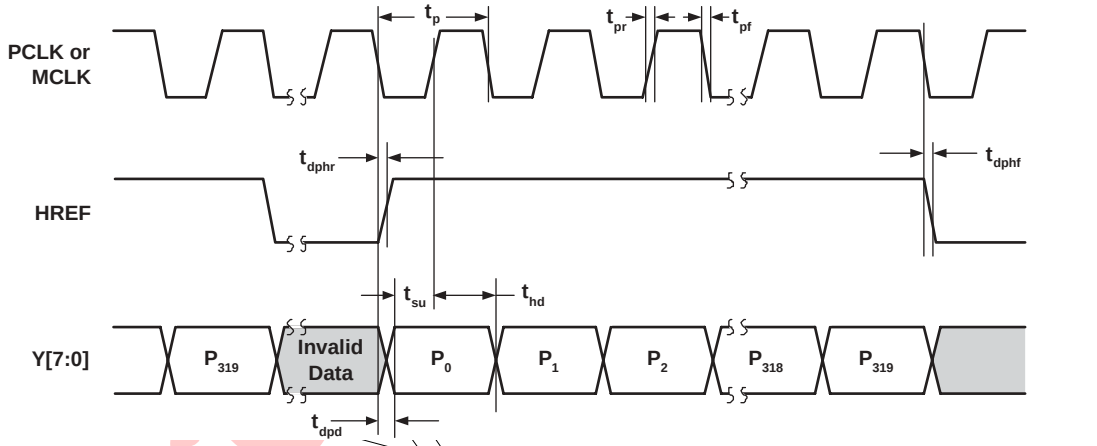


Figure 13 VGA Frame Timing

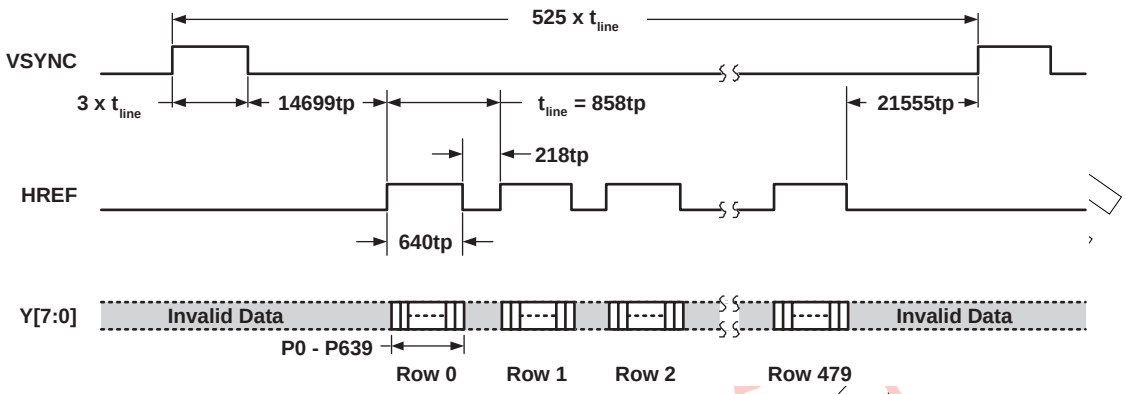


Figure 14 QVGA Frame Timing

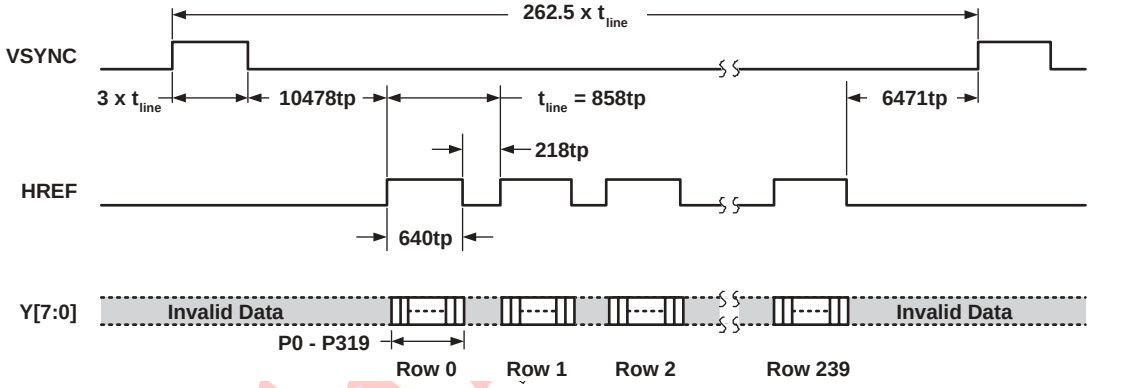
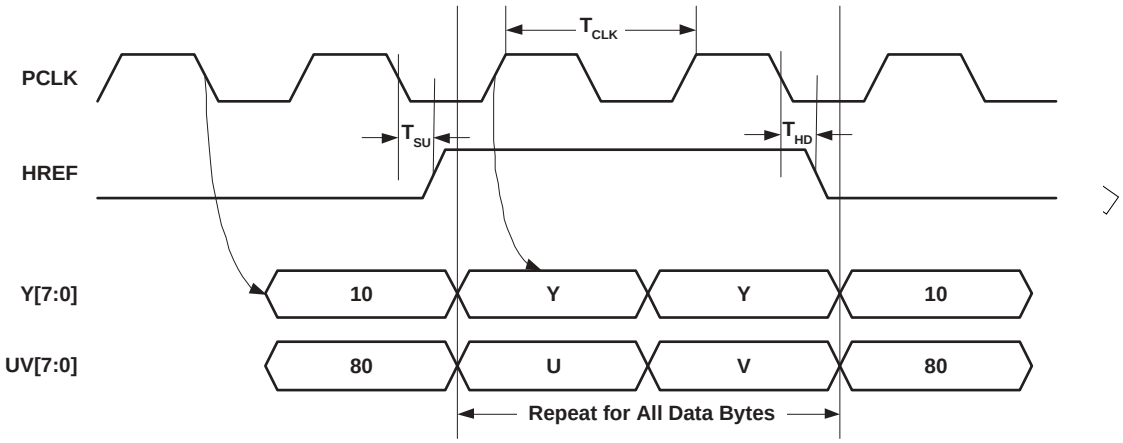


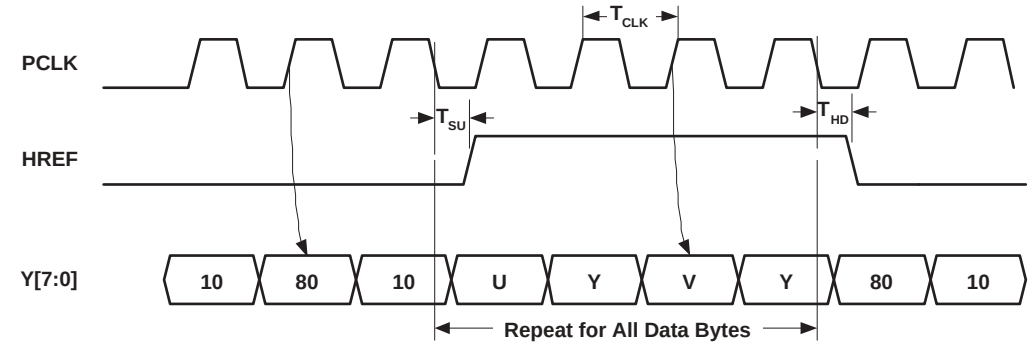
Table 15 Pixel Timing Specification

Symbol	Parameter	Min	Typ	Max	Unit
t_p	PCLK period		41.67		ns
t_{pr}	PCLK rising time		10		ns
t_{pf}	PCLK falling time		5		ns
t_{dphr}	PCLK negative edge to HREF rising edge	0		5	ns
t_{dphf}	PCLK negative edge to HREF negative edge	0		5	ns
t_{dpd}	PCLK negative edge to data output delay	0		5	ns
t_{su}	Data bus setup time	15			ns
t_{hd}	Data bus hold time	8			ns

Figure 15 Pixel Data Bus (YUV Output) Timing



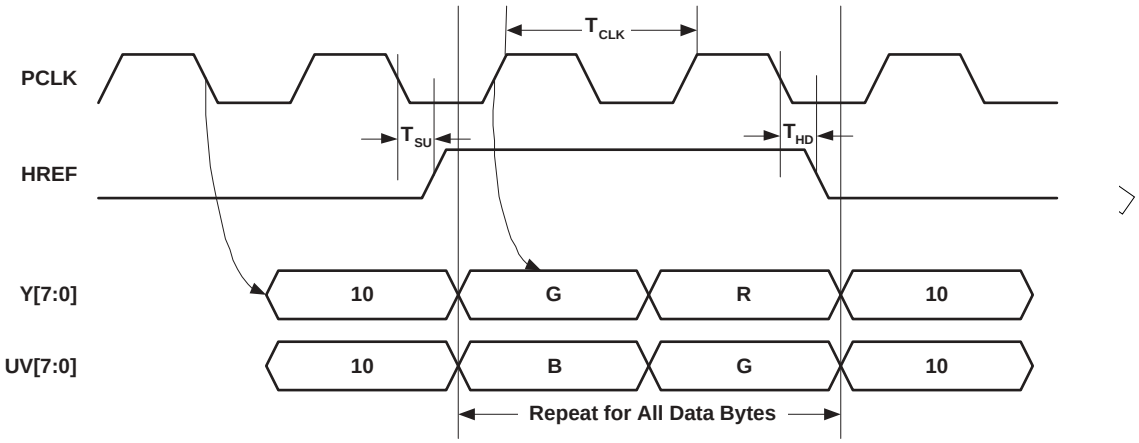
Pixel Data 16-bit Timing
(PCLK rising edge latches data bus)



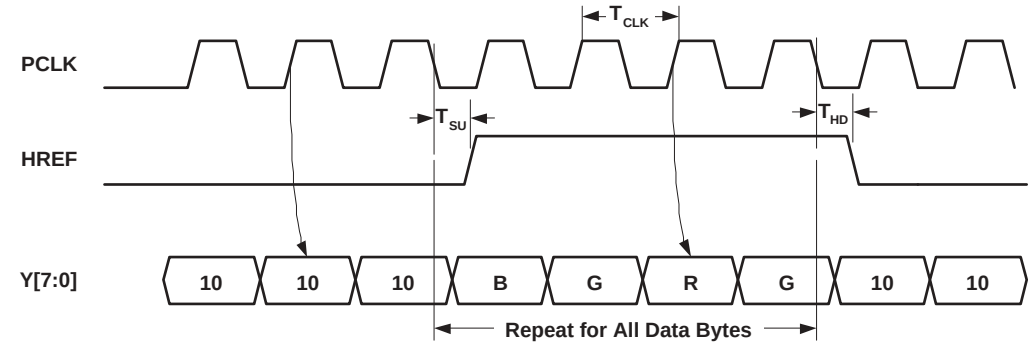
Pixel Data 8-bit Timing
(PCLK rising edge latches data bus)

NOTES:
1. T_{CLK} is the pixel clock period. T_{CLK} = 50 ns for 16-bit output and T_{CLK} = 25 ns for 8-bit output if the system clock is 20 MHz with on-chip 2x PLL.
2. T_{SU} is the setup time for HREF with a maximum time of 15 ns.
3. T_{HD} is the hold time for HREF with a maximum time of 15 ns.

Figure 16 Pixel Data Bus (RGB Output) Timing



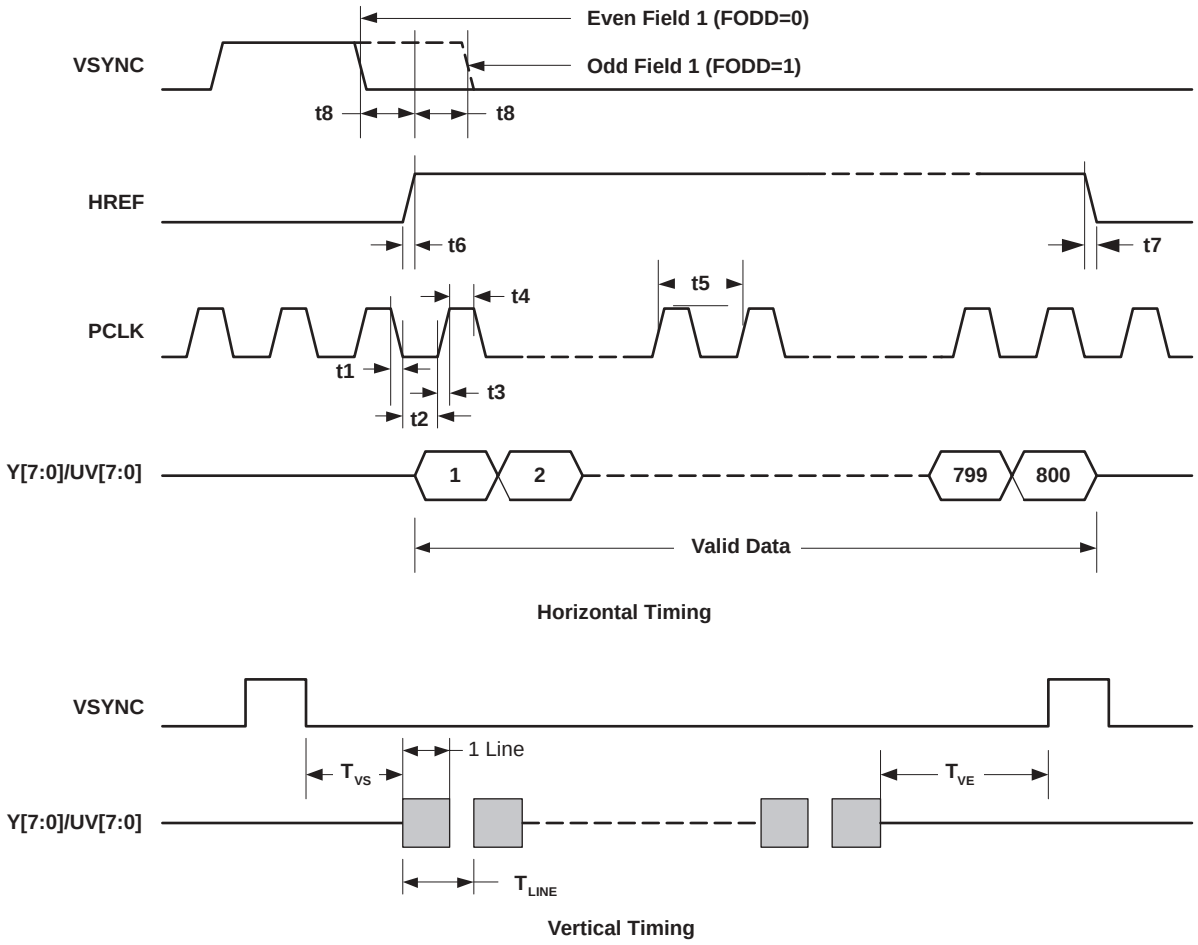
Pixel Data 16-bit Timing
(PCLK rising edge latches data bus)



Pixel Data 8-bit Timing
(PCLK rising edge latches data bus)

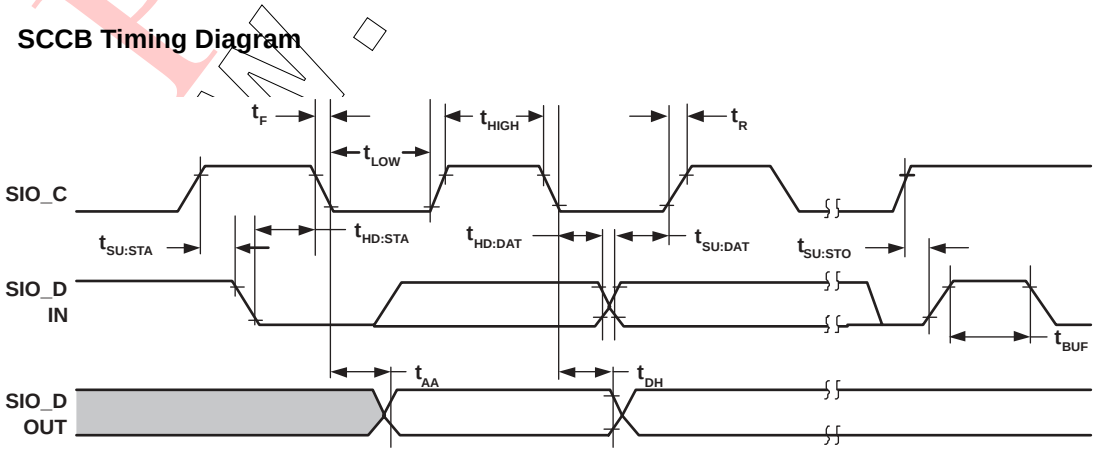
NOTES:
1. T_{CLK} is the pixel clock period. T_{CLK} = 50 ns for 16-bit output and T_{CLK} = 25 ns for 8-bit output if the system clock is 20 MHz with on-chip 2x PLL.
2. T_{SU} is the setup time for HREF with a maximum time of 15 ns.
3. T_{HD} is the hold time for HREF with a maximum time of 15 ns.

Figure 17 Zoom Video Port Timing



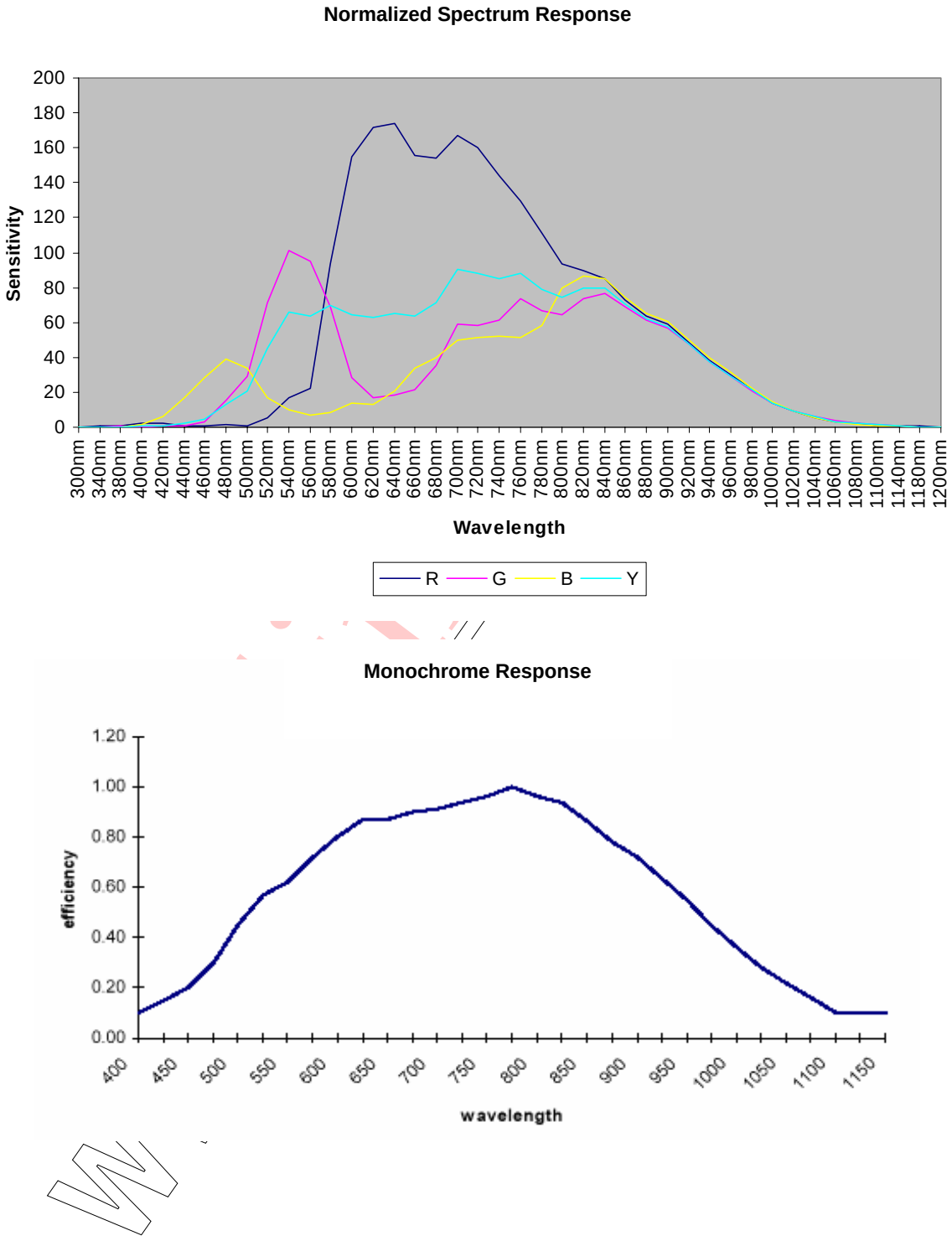
NOTE: Zoom Video Port format output signal includes:
- VSYNC: Vertical sync pulse
- HREF: Horizontal valid data output window
- PCLK: Pixel clock used to clock valid data and CHSYNC into Zoom Video Port. Default frequency is 20 MHz when using 20 MHz as system clock plus 2x PLL implemented on the chip. Rising edge of PCLK is used to clock 16-bit data.
- Y[7:0]: 8-bit luminance data bus
- UV[7:0]: 8-bit chrominance data bus

Figure 18 SCCB Timing Diagram



OV7635/OV7135 Light Response

Figure 19 OV7635/OV7135 Light Response



Register Set

Table 16 provides a list and description of the Device Control registers contained in the OV7635/OV7135. The device slave addresses for the OV7635/OV7135 are 42 for write and 43 for read.

Table 16 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
00	GAIN	00	RW	AGC – Gain Control Setting Bit[7:6]: Reserved Bit[5:0]: Current gain setting This register is updated automatically if AGC is enabled. The internal controller stores the optimal gain value in this register. The current value is stored in this register if AGC is not enabled.
01	BLUE	80	RW	Blue Gain Control Bit[7:0]: Blue channel gain balance value • Range: [00] to [FF] ***Note:*** *This function is not available on the B&W OV7135.*
02	RED	80	RW	Red Gain Control Bit[7:0]: Red channel gain balance value • Range: [00] to [FF] ***Note:*** *This function is not available on the B&W OV7135.*
03	SAT	80	RW	Color Saturation Control Bit[7:4]: Saturation adjustment • Range: [00] to [F0] Bit[3:0]: Reserved ***Note:*** *This function is not available on the B&W OV7135.*
04	HUE	10	RW	Color Hue Control Bit[7:6]: Reserved Bit[5]: Enable hue control Bit[4:0]: Hue control • Range: -30° to 30° ***Note:*** *This function is not available on the B&W OV7135.*
05	CNT	20	RW	Contrast Control Bit[7:6]: Reserved Bit[5]: Enable contrast control Bit[4:0]: Contrast control • Range: 0.6 to 1.6
06	BRT	80	RW	Brightness Control Bit[7:0]: Brightness adjustment • Range: [00] to [FF]
07-09	RSVD	XX	–	Reserved
0A	PID	76	R	Product ID number (Read only)
0B	VER	30	R	Product version number (Read only)

Table 16 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
0C	ABLU	20	RW	White Balance Background - Blue Channel Bit[7:6]: Reserved Bit[5:0]: White balance blue ratio adjustment • [3F] is most blue ***Note:*** *This function is not available on the B&W OV7135.*
0D	ARED	20	RW	White Balance Background - Red Channel Bit[7:6]: Reserved Bit[5:0]: White balance red ratio adjustment • [3F] is most red ***Note:*** *This function is not available on the B&W OV7135.*
0E-0F	RSVD	XX	–	Reserved
10	AEC	41	RW	Automatic Exposure Control (MSB) Bit[7:0]: AEC[9:2] MSB (see "COMO" on page 36 for AEC[1:0] LSB) AEC[9:0] = Set exposure time $T_{EX} = T_{LINE} \times AEC[9:0]$
11	CLKRC	00	RW	Clock Rate Control Bit[7:6]: Sync output polarity selection 00: HSYNC = NEG, CHSYNC = NEG, VSYNC = POS 01: HSYNC = NEG, CHSYNC = NEG, VSYNC = NEG 10: HSYNC = POS, CHSYNC = NEG, VSYNC = POS 11: HSYNC = POS, CHSYNC = POS, VSYNC = POS Bit[5:0]: Clock Pre-Scalar PCLK = (MAIN_CLOCK / ((CLKRC[5:0] + 1) x 2)) / n where n = 1, if COMD[5] = 1 (see "COMD" on page 24) and n = 2, if otherwise.

Table 16 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
12	COMA	24	RW	Common Control A Bit[7]: SRST 1: Initiates a soft reset. All registers are set to default values, and chip is reset to known state and resumes normal operation. Bit[6]: Reserved Bit[5]: AGC enable 1: Enables AGC Bit[4]: Digital output format 0: U Y V Y U Y V Y 1: Y U Y V Y U Y V Bit[3]: Select video data output 0: YCbCr 1: RGB ***Note:*** *Bit[3] is not programmable on the B&W OV7135.* Bit[2]: Auto White Balance (AWB) 0: Disable AWB 1: Enable AWB Bit[1]: Color bar test pattern 1: Enable color bar test pattern Bit[0]: ADC BLC method 0: More stable but less precise 1: Precise
13	COMB	21	RW	Common Control B Bit[7]: Clock used to generate 30 fps frame rate 0: 27 MHz clock 1: 24 MHz clock Bit[6]: Banding filter option 1: Main clock is 13MHz/12MHz Bit[5]: Reserved Bit[4]: Digital output 1: Enable digital output in ITU-656 format Bit[3]: CHSYNC output 0: Horizontal sync 1: Composite sync - only effective when COMJ[5]=1 (see "COMJ" on page 35) Bit[2]: Y and UV buses 0: Enable both buses 1: Tri-state Y and UV buses Bit[1]: Reserved Bit[0]: Auto adjust mode enable 0: Disable auto adjust mode 1: Enable auto adjust mode

Table 16 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
14	COMC	04	RW	Common Control C Bit[7]: AWB threshold selection 0: More accurate but less stable 1: More stable but less accurate Bit[6]: Reserved Bit[5]: QVGA digital output format selection 0: 640 x 480 1: 320 x 240 Bit[4]: Field/Frame vertical sync output in VSYNC port selection 0: Field sync, in effect when in interlaced mode 1: Frame sync, only ODD field vertical sync Bit[3]: HREF polarity selection 0: HREF positive effective 1: HREF negative Bit[2]: Gamma selection 0: RGB gamma is 1 1: RGB gamma ON Bit[1:0]: Reserved
15	COMD	01	RW	Common Control D Bit[7]: Output range 0: [00] and [FF] reserved and flag bits 1: Output at full range as [00] to [FF] Bit[6]: PCLK polarity selection 0: Output data at PCLK falling edge and data bus will be stable at PCLK rising edge 1: Rising edge output data and stable at PCLK falling edge Bit[5:4]: AWB step selection - affects stability and speed of AWB 00: 1 bit each step, total 256 steps 01: 4 bits each step, total 64 steps 10: 2 bits each step, total 128 steps 11: 4 bits each step, total 64 steps Bit[3]: Fast AEC step selection 0: Small step (effective only when COMD[2] = 1) 1: Big step Bit[2]: Fast AEC mode 1: Enables fast AEC small step selection (see COMD[3] = 1) Bit[1]: Reserved Bit[0]: UV digital output sequence exchange control 0: V Y U Y 1: U Y V Y ***Note:*** *Bit[0] is not programmable on the B&W OV7135.*

Table 16 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
16	FSD	03	RW	Field Slot Division Bit[7:2]: Field interval selection It functions in EVEN and ODD modes defined by FSD[1:0]. It is disabled in OFF and FRAME modes. The purpose of FSD[7:2] is to divide the video signal into programmed number of time slots, allowing HREF to be active for only one field in every FSD[7:2] fields. It does not affect the video data or pixel rate. 01: Outputs one field every field 10: Outputs one field every two fields All other selections: Output black reference Bit[1:0]: Field mode selection Each frame consists of two fields, Odd and Even. FSD[1:0] define the assertion of HREF in relation to the two fields. 00: OFF mode - HREF is not asserted in both fields, one exception is the single frame transfer operation (see description of COMJ[7]) 01: Interlaced mode (ODD mode) - HREF is asserted in ODD field only Progressive mode - HREF is asserted in frame according to FSD[7:2] 10: Interlaced mode (EVEN mode) - HREF is asserted in EVEN field only Progressive mode - HREF is asserted in frame according to FSD[7:2] 11: FRAME mode - HREF is asserted in both Odd field and Even field. FSD[7:2] is disabled.
17	HREFST	2D	RW	Horizontal HREF Start Bit[7:0]: Selects the starting point of the HREF window. Each LSB represents four pixels for VGA resolution mode, two pixels for QVGA resolution mode, and one pixel for QQVGA mode. This value is based on an internal column counter. The default value corresponds to 640 horizontal windows. Maximum window size is 664. HREFST[7:0] should be less than HREFEND[7:0].
18	HREFEND	CD	RW	Horizontal HREF End Bit[7:0]: Selects the ending point of the HREF window. Each LSB represents four pixels for full resolution, two pixels for QVGA resolution mode, and one pixel for QQVGA mode. This value is based on an internal column counter. The default value corresponds to the last available pixel. HREFEND[7:0] should be larger than HREFST[7:0].

Table 16 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
19	VSTRT	06	RW	Vertical Line Start Bit[7:0]: Selects the starting row of the vertical window. In full resolution mode, each LSB represents 2 scan lines in one field for Interlaced scan mode, 4 scan lines in one frame for Progressive scan mode. In QVGA mode, each LSB represents 1 scan line in one field for Interlaced mode, 2 scan lines in one frame for Progressive scan mode. VSTRT[7:0] should be less than VEND[7:0]. • Range: [02] to [98]
1A	VEND	F6	RW	Vertical Line End Bit[7:0]: Selects the ending row of the vertical window. In full resolution mode, each LSB represents 2 scan line in one field for Interlaced scan mode, 4 scan lines in one frame for Progressive scan mode. In QVGA mode, each LSB represents 1 scan line in one field for Interlaced mode, 2 scan lines in one frame for Progressive scan mode. VEND[7:0] should be larger than VSTRT[7:0]. • Range: [03] to [98]
1B	PSHIFT	00	RW	Pixel Shift Bit[7:0]: Provides a way to fine tune the output timing of the pixel data relative to that of HREF. It physically shifts the video data output time late in unit of pixel clock. This function is different from changing the size of the window as defined by HREFST[7:0] (see "HREFST" on page 25) and HREFEND[7:0] (see "HREFEND" on page 25). It just delays the output pixels relative to HREF and does not change the window size. The highest number is [FF] and the maximum shift number is delay 256 pixels.
1C	MIDH	7F	R	Manufacturer ID Byte – High (Read only = 0x7F)
1D	MIDL	A2	R	Manufacturer ID Byte – Low (Read only = 0xA2)
1E	RSVD	XX	–	Reserved
1F	SOFT	00	RW	Soft Reset Option for Array Bit[7]: Frame exposure reset option 0: Line reset - only in effect when SOFT[6] = 1 1: Whole array reset at the same time Bit[6]: Frame exposure option 1: Enables line reset (see SOFT[7]) Bit[5]: Refers to the gap of AEC/AGC when exposure time is less than 8 lines 1: Large gap Bit[4:1]: Reserved Bit[0]: Array soft reset

Table 16 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
20	COME	80	RW	Common Control E Bit[7]: Reserved Bit[6]: Field/Frame luminance average value calculation enable Value is stored in AVG[7:0] (see "AVG" on page 37) Bit[5]: Reserved Bit[4]: Aperture correction enable - correction strength and threshold value will be decided by COMF[7:6] and COMF[5:4] (see "COMF" on page 29). 1: Enables aperture correction Bit[3]: AWB smart mode enable 0: Count all pixels to get AWB result. Valid only when COMB[0] = 1 (see "COMB" on page 23) and COMA[2] = 1 (see "COMA" on page 23) 1: Do not count pixels when luminance level is not in the range defined in AWBC[7:6] and AWBC[5:4] (see "AWBC" on page 34) ***Note:*** *Bit[3] is not programmable on the B&W OV7135.* Bit[2]: Enable AWB manual adjustable in auto mode Bit[1]: AWB fast/slow mode selection 0: AWB is in slow mode. Registers BLUE[7:0] (see "BLUE" on page 21) and RED[7:0] (see "RED" on page 21) change every 16/64 field decided by COMK[1]. When AWB is enabled by setting COMA[2] = 1 (see "COMA" on page 23), AWB begins working in fast mode until AWB reaches a stable state, then it changes to slow mode. 1: AWB is always in fast mode, where registers BLUE[7:0] and RED[7:0] change every field. ***Note:*** *Bit[1] is not programmable on the B&W OV7135.* Bit[0]: Digital output driver capability increase selection 0: Low output driver current status 1: Double digital output driver current
21	YOFF	80	RW	Y Channel Offset Adjustment Bit[7]: Offset adjustment direction 0: Add YOFF[6:0] 1: Subtract YOFF[6:0] Bit[6:0]: Y channel digital output offset adjustment If COMG[2] = 0 (see "COMG" on page 30), this register will updated by internal circuit. Writing a value to this register through the SCCB interface will have no affect. If COMG[2] = 1, Y channel offset adjustment will use the stored value which can be changed through the SCCB interface. This register has no affect on ADC output data if COMF[1] = 0 (see "COMF" on page 29). If output is RGB raw data, this register will adjust G channel data. • Range: -127 to 127

Table 16 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
22	UOFF	80	RW	U Channel Offset Adjustment Bit[7]: Offset adjustment direction 0: Add UOFF[6:0] 1: Subtract UOFF[6:0] Bit[6:0]: U channel digital output offset adjustment If COMG[2] = 0 (see "COMG" on page 30), this register will updated by internal circuit. Writing a value to this register through the SCCB interface will have no affect. If COMG[2] = 1, U channel offset adjustment will use the stored value which can be changed through the SCCB interface. This register has no affect on ADC output data if COMF[1] = 1 (see "COMF" on page 29). If output is RGB raw data, this register will adjust B channel data. • Range: -128 to 128
23	CLKC	DE	RW	Oscillator Circuit and Common Mode Control Bit[7:6]: Select different crystal circuit power level • [11] minimum Bit[5]: ADC current control 0: Full current 1: Half current Bit[4]: Optical black register update option 0: Disable optical black register update option 1: Automatically update optical black register Bit[3:2]: Reserved Bit[1]: QVGA format clock option - effective only in QVGA one line mode. Changes to this bit by users is NOT recommended Bit[0]: Data output every two lines - effective only in QVGA one line mode
24	AEW	10	RW	AEC - Bright Pixel Ratio Adjustment Bit[7:0]: Used to calculate bright pixel ratio. The OV7635/OV7135 algorithm is a count of the whole field/frame bright pixel ratio (pixels whose luminance level is higher than a fixed level) and black pixel ratio (pixels whose luminance level is lower than a fixed level). When the bright/black pixel ratio in the range of the ratio defined by the registers AEW[7:0] and AEB[7:0] (see "AEB" on page 29), the image is stable. This register is used to define bright pixel ratio, default is 25%. Each LSB represents step: 1.3% for interlaced and 0.7% for progressive scan. Change range is [01] to [9A]. Increasing AEW[7:0] will increase the bright pixel ratio. For same light condition, the image brightness will increase if AEW[7:0] increases. ***Note:*** *AEW[7:0] must combine with register AEB[7:0]. The relationship must be as follows:* *AEW[7:0] + AEB[7:0] > [9A]*

Table 16 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
25	AEB	8A	RW	AEC - Black Pixel Ratio Adjustment Bit[7:0]: Used to calculate black pixel ratio. The OV7635/OV7135 algorithm is a count of the whole field/frame bright pixel ratio (pixels whose luminance level is higher than a fixed level) and black pixel ratio (pixels whose luminance level is lower than a fixed level). When the bright/black pixel ratio in the range of the ratio defined by the registers AEW[7:0] (see "AEW" on page 28) and AEB[7:0], the image is stable. This register is used to define black pixel ratio, default is 75%. Each LSB represents step: 1.3% for interlaced and 0.7% for progressive scan. Change range is [01] to [9A]. Increasing AEB[7:0] will increase the black pixel ratio. For same light condition, the image brightness will decrease if AEB[7:0] increases. ***Note:*** *AEW[7:0] must combine with register AEB[7:0]. The relationship must be as follows:* *AEW[7:0] + AEB[7:0] > [9A]*
26	COMF	A2	RW	Common Control F Bit[7:6]: Aperture correction threshold selection • Range: 1% to 6.4% of difference of neighbor pixel luminance Bit[5:4]: Aperture correction strength selection • Range: 0% to 200% of difference of neighbor pixel luminance Bit[3]: Reserved Bit[2]: Digital data MSB/LSB swap 0: Normal 1: LSB to bit[7] and MSB to bit[0] Bit[1]: Digital offset adjustment enable 0: Disable 1: Enable Bit[0]: Black level output 0: No black level output 1: Output first 4/8 line black level before valid data output, Interlaced/Progressive scan mode respectively. HREF number will increase 4/8 lines, relatively.

Table 16 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
27	COMG	E2	RW	Common Control G Bit[7]: Reserved Bit[6]: Enable band gap reference for array other than diode reference Bit[5]: Reserved Bit[4]: Bypass RGB matrix, which is used to cancel the crosstalk of color filter Bit[3]: Enable ADC black level calibration offset defined by registers YBAS[7:0] (see "YBAS" on page 36), UBAS[7:0] (see "UBAS" on page 37), and VBAS[7:0] (see "VBAS" on page 37) Bit[2]: Digital offset adjustment manual mode enable 0: Digital data is added/subtracted by a value defined by registers YOFF[7:0] (see "YOFF" on page 27), UOFF (see "UOFF" on page 28), and VCOFF (see "VCOFF" on page 32), which are updated by internal circuit. Effective only when COMF[1] = 1 (see "COMF" on page 29). 1: Digital data is added/subtracted by a value defined by registers YOFF[7:0] (see "YOFF" on page 27), UOFF (see "UOFF" on page 28), and VCOFF (see "VCOFF" on page 32). The contents are programmed through the SCCB interface. Bit[1]: Digital output full range selection 0: Output data range is [10] to [F0] 1: Output data range is [01] to [FE] with signal overshoot and undershoot level Bit[0]: Reserved
28	COMH	00	RW	Common Control H Bit[7]: RGB raw data output format selection 0: Selects normal two-line RGB raw data output format 1: Selects one-line RGB raw data output format Bit[6]: Black/white mode enable 0: Normal color mode 1: Enable black/white mode ***Note:*** *The vertical resolution will be higher than color mode when the image sensor works as B&W mode. OV7635/OV7135 outputs data from Y port. COMB will be set to "0".* Bit[5]: Progressive scan mode selection 0: Interlaced 1: Progressive Bit[4]: Freeze AEC/AGC value. Effective only when COMB[0] = 1 (see "COMB" on page 23) 0: AEC/AGC normal working status 1: Registers GAIN[7:0] (see "GAIN" on page 21) and AEC (see "AEC" on page 22) will not be updated. Hold latest value. Bit[3:2]: Reserved Bit[1]: Gain control bit 0: No change to the channel gain 1: Channel gain increases 3 dB Bit[0]: Reserved

Table 16 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
29	COMI	34	RW	Common Control I Bit[7]: Reserved Bit[6]: Double clock rate 2x option Bit[5:4]: Reserved Bit[3]: AEC/AGC calculation selection 0: Use whole image to calculate AEC/AGC 1: Use central 1/4 image area to calculate AEC/AGC Bit[2]: Reserved Bit[1:0]: Version flag - these two bits are read-only 00: Version A
2A	FRARH	00	RW	Frame Rate Adjust High Bit[7]: Frame rate adjustment enable 0: Disable 1: Enable Bit[6:5]: Highest 2 bits of frame rate adjust control byte Bit[4]: UV delay 2 pixels if this bit is high Bit[3]: Y brightness manual adjustment. Effective only if COMF[1] = 1 (see "COMF" on page 29) Bit[2]: Reserved Bit[1]: Data output 1: One frame data output. Only when in Frame Exposure mode Bit[0]: Use internal average of luminance to determine the AEC/AGC rather than comparator counter
2B	FRARL	00	RW	Frame Rate Adjust Low Bit[7:0]: Frame rate adjust control byte. Frame rate adjustment resolution is 0.12%. Control byte is 10 bit. Every LSB equals decrease frame rate 0.12%. • Range: 0.12% to 112%
2C	EXBK	88	RW	Auto Brightness Ratio Control Bit[7:4]: Ratio for auto brightness control • Range: 0.06% to 3.85% Bit[3:0]: Ratio for auto brightness control • Range: 0.06% to 3.85% If the pixel that is lower than reference level percentage is larger than EXBK[7:4] + EXBK[3:0], the brightness determined by BRT[7:0] (see "BRT" on page 21) will decrease. If this percentage is less than EXBK[3:0], the brightness will increase. If this percentage is between EXBK[3:0] and EXBK[7:4] + EXBK[3:0], auto brightness will be stable.

Table 16 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
2D	COMJ	81	RW	Common Control J Bit[7]: AEC update rate selection 0: AEC update every one field 1: AEC update every two or four fields Bit[6]: QVGA format option 0: Every field array data output and the data is dropped every other line at digital format output, maximum frame rate is 30 fps 1: Only odd field array data output and the read format is interlaced, maximum frame rate is 60 fps Bit[5]: Reserved Bit[4]: Auto black expanding mode enable Bit[3]: Reserved Bit[2]: Band filter enable - enables a different exposure algorithm to cut light banding induced by fluorescent lighting. Bit[1:0]: Reserved
2E	VCOFF	2C	RW	V Channel Offset Adjustment Bit[7]: Offset adjustment direction 0: Add VCOFF[6:0] 1: Subtract VCOFF[6:0] Bit[6:0]: V channel digital output offset adjustment If COMG[2] = 0 (see "COMG" on page 30), this register will updated by internal circuit. Writing to this register through the SCCB interface will have no affect. If COMG[2] = 1, V channel offset adjustment will use the stored value which can be changed through the SCCB interface. This bit is only effective if COMF[1] = 0. If output is RGB raw data, this register will adjust R channel data. • Range: -128 to 128 ***Note:*** *This function is not available on the B&W OV7135.*
2F	REF1	31	RW	Internal Doubler and Internal Voltage Reference Control Bit[7]: Internal doubler enable Bit[6:0]: Internal voltage reference control
30	REF2	38	RW	Internal Voltage Reference and Current Control Changes to this value by the user is NOT recommended.
31	ARRAY	00	RW	Array Work Mode Selection Changes to this value by the user is NOT recommended.
32	DBL	06	RW	Double Drive Current Control Bit[7:4]: Double drive current control. Each bit represents 1x current drive capability Bit[3:0]: Reserved

Table 16 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
33	BGP	08	RW	Band Gap Reference Control Bit[7]: Band gap reference function enable Bit[6:0]: Band gap reference adjustment control
34-4B	RSVD	XX	–	Reserved
4C	MEDC	00	RW	Medium Filter Option Control Bit[7]: AWB step and range x 1.5 when this register = 1 Bit[6]: Reserved Bit[5]: Medium filter for RGB channel Bit[4]: Medium filter for Y channel controlled by GAIN[5:0] (see "GAIN" on page 21) Bit[3]: Reserved Bit[2:0]: Medium filter for Y channel component R/G/B controlled manually, respectively
4D	ADDC	00	RW	ADC Converter Option Control Bit[7:4]: Reserved Bit[3:2]: UV delay selection 00: No delay 01: No delay 10: 2tp delay 11: 4tp delay Bit[1:0]: Reserved
4E-5F	RSVD	XX	–	Reserved
60	SPCA	00	RW	Signal Process Control A Bit[7]: Channel 1.5x preamplifier gain enable Bit[6]: Analog half current selection Bit[5]: Gev/God switch instead of average for G in RGB and UV channel Bit[4]: Gev/God switch instead of average for Y channel in YUV mode Bit[3:2]: Red channel preamplifier gain selection 00: 1x 01: 1.2x 10: 1.4x 11: 1.6x Bit[1:0]: Blue channel preamplifier gain selection 00: 1x 01: 1.2x 10: 1.4x 11: 1.6x

Table 16 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
61	SPCB	80	RW	Signal Process Control B Bit[7]: AGC/AEC feedback loop using Y channel. When RGB output must set it to "0". Bit[6:4]: Reserved Bit[3]: RGB brightness control enable Bit[2]: Brightness control BRT[7:0] (see "BRT" on page 21) range and step half Bit[1:0]: Auto brightness reference level 00: 0 IRE 01: 6 IRE 10: 10 IRE 11: 20 IRE
62-64	RSVD	XX	–	RGB and Y Gamma Curve Control Changes to this value by the user is NOT recommended.
65	SPCC	02	RW	Signal Process Control C Bit[7:0]: Reserved for internal use.
66	AWBC	55	RW	AWB Process Control Bit[7:6]: Selectable highest luminance level to be available in AWB control. Pixels whose value is larger than this threshold is excluded from AWB Bit[5:4]: Selectable lowest luminance level to be available in AWB control. Pixels whose value is less than this threshold is excluded from AWB Bit[3:2]: Selectable U level to be available in AWB control. This bit is only in effect if COMM[7] = 1 (see "COMM" on page 36) Bit[1:0]: Selectable V level to be available in AWB control. This bit is only in effect if COMM[7] = 1 (see "COMM" on page 36)
67	YMXB	01	RW	YUV Matrix Control Bit[7:6]: UV coefficient selection, u = B - Y, v = R - Y 00: U = u, V = v 01: U = 0.938u, V = 0.838v 10: U = 0.563u, V = 0.613v 11: U = 0.5u, V = 0.877v Bit[5]: Reserved Bit[4]: UV signal with 3 points average Bit[3:2]: Y delay selection • Range: 0tp to 3tp Bit[1:0]: Reserved
68	ARL	AC	RW	AEC/AGC Reference Level Bit[7:5]: Voltage reference selection (higher voltage equals brighter final stable image) • Range: [000] to [111] Bit[4:0]: Reserved

Table 16 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
69	ADRC	42	RW	ADC Reference Adjustment and Control Bit[7:4]: ADC control bit - changes to this value by the user is NOT recommended Bit[3]: ADC range selection 0: Full range - ADC is equal to about 0.6V analog level 1: Full range - ADC is equal to about 0.9V analog level Bit[2:0]: ADC reference control - affects the ADC signal range. Changes to this value by the user is NOT recommended.
6A-6E	RSVD	XX	–	Reserved
6F	EOC	00	RW	Even/Odd Noise Compensation Bit[7]: Disable analog output at pin GYYO Bit[6:5]: Reserved Bit[4]: Sign of Even/Odd noise compensation Bit[3:0]: Even/Odd noise compensation • Range: 6.4 bits
70	COMK	01	RW	Common Control K Bit[7]: Enable one line output for optical black Bit[6]: Output port drive current 2x larger option Bit[5]: Aperture correction option Bit[4:3]: Reserved Bit[2]: Double aperture correction strength Bit[1]: 4x stable time less when in AWB slow mode 0: AWB updates every 16 fields/frames 1: AWB updates every 64 fields/frames Bit[0]: Reserved
71	COMJ	00	RW	Common Control J Bit[7]: AEC update rate option 0: Fast 1: Slow Bit[6]: PCLK output gated by HREF Bit[5]: Change CHSYNC output port to HREF Bit[4]: Reserved Bit[3:2]: Highest 2 bits for HSYNC rising edge shift control (see "HSDY" on page 35) Bit[1:0]: Highest 2 bits for HSYNC falling edge shift control (see "HEDY" on page 36)
72	HSDY	10	RW	Horizontal SYNC Rising Edge Shift Bit[7:0]: HSDY[7:0] together with COMJ[3:2] (see "COMJ" on page 35) for the HSYNC rising edge shift control. Value must be less than HEDY[7:0] (see "HSDY" on page 35). Step is 1 pixel. • Range: [000] to [35A]

Table 16 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
73	HEDY	50	RW	Horizontal SYNC Falling Edge Shift Bit[7:0]: HEDY[7:0] together with COMJ[1:0] (see "COMJ" on page 35) for the HSYNC falling edge shift control. Value must be larger than HSDY[7:0] (see "HSDY" on page 35). Step is 1 pixel. • Range: [000] to [35A]
74	COMM	20	RW	Common Control M Bit[7]: UV smart AWB enable Bit[6:5]: AGC maximum gain boost control 00: 6 dB 01: 12 dB 10: 6 dB 11: 18 dB Bit[4]: Reserved Bit[3]: AEC update rate option 0: 32/64/128 fields depending upon COMM[2:0] 1: 64/128/256 fields depending upon COMM[2:0] Bit[2:0]: AEC update rate option 001: Every 128/256 fields according to COMM[3] 010: Every 64/128 fields according to COMM[3] 100: Every 32/64 fields according to COMM[3] All other values are invalid
75	COMN	02	RW	Common Control N Bit[7]: Vertical flip enable Bit[6:4]: Reserved for internal test mode Bit[3]: Drop one field/frame when exposure line change is bigger than a fixed number Bit[2]: Enable exposure to go down to less than 1/120" in smooth AEC mode Bit[1:0]: Reserved
76	COMO	01	RW	Common Control O Bit[7]: Tri-state output bus in power-down mode when high Bit[6]: Reserved Bit[5]: Software power-down mode Bit[4:3]: Reserved Bit[2]: Tri-state all timing output except data line Bit[1:0]: AEC[1:0] LSB (see "AEC" on page 22 for AEC[9:2] MSB)
77	AEGR	F3	RW	AEC/AGC Fast Mode Threshold Control Bit[7]: AEC/AGC fast mode high threshold control. Same as AEW[7:0] (see "AEW" on page 28) Bit[6]: AEC/AGC fast mode low threshold control. Same as AEB[7:0] (see "AEB" on page 29)
78	YBAS	80	RW	Y/G ADC Offset Bit[7:0]: Fixed offset to final Y/G data • Range: -128 to 128

Table 16 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
79	UBAS	80	RW	U/B ADC Offset Bit[7:0]: Fixed offset to final U/B data • Range: -128 to 128
7A	VBAS	80	RW	V/R ADC Offset Bit[7:0]: Fixed offset to final V/R data • Range: -128 to 128
7B	RSVD	XX	–	Reserved
7C	AVG	00	RW	Field/Frame Average Level Storage Only effective if COME[6] = 1 (see "COME" on page 27)
7D	COMP	77	RW	Common Control P Bit[7]: Optical black line as black level calibration. Only effective when COMP[6] = 1. Bit[6]: Optical black line enable. Bit[5:3]: Reserved Bit[2]: VSYNC drop option 0: VSYNC always exists 1: VSYNC will drop when frame data drops Bit[1:0]: Reserved
7E-7F	RSVD	XX	–	Reserved
NOTE: All other registers are factory-reserved. Please contact OmniVision Technologies for reference register settings.				

Package Specifications

The OV7635/OV7135 uses a 24-pin ceramic package. Refer to Figure 20 for package information, Table 17 for package dimensions, and Figure 21 for the array center on the chip.

Figure 20 OV7635/OV7135 Package Specifications

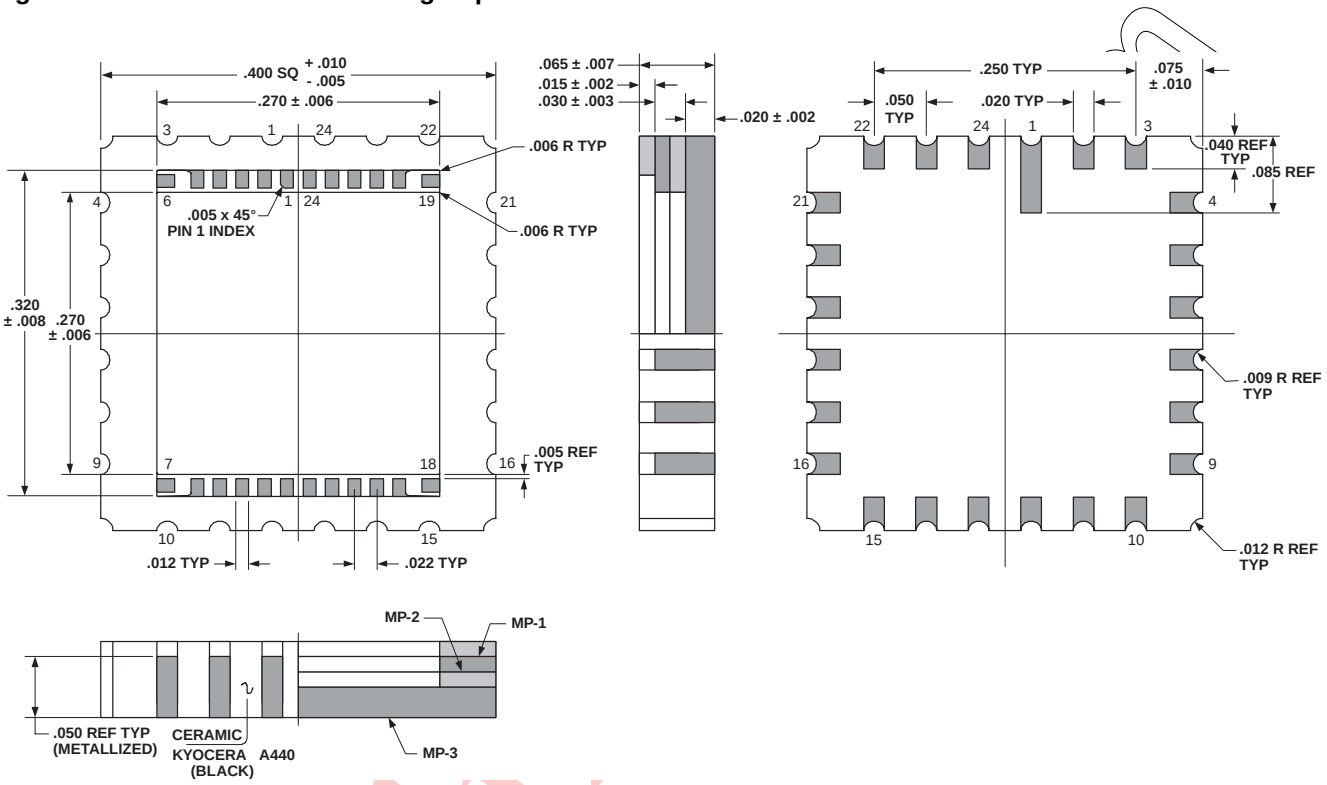
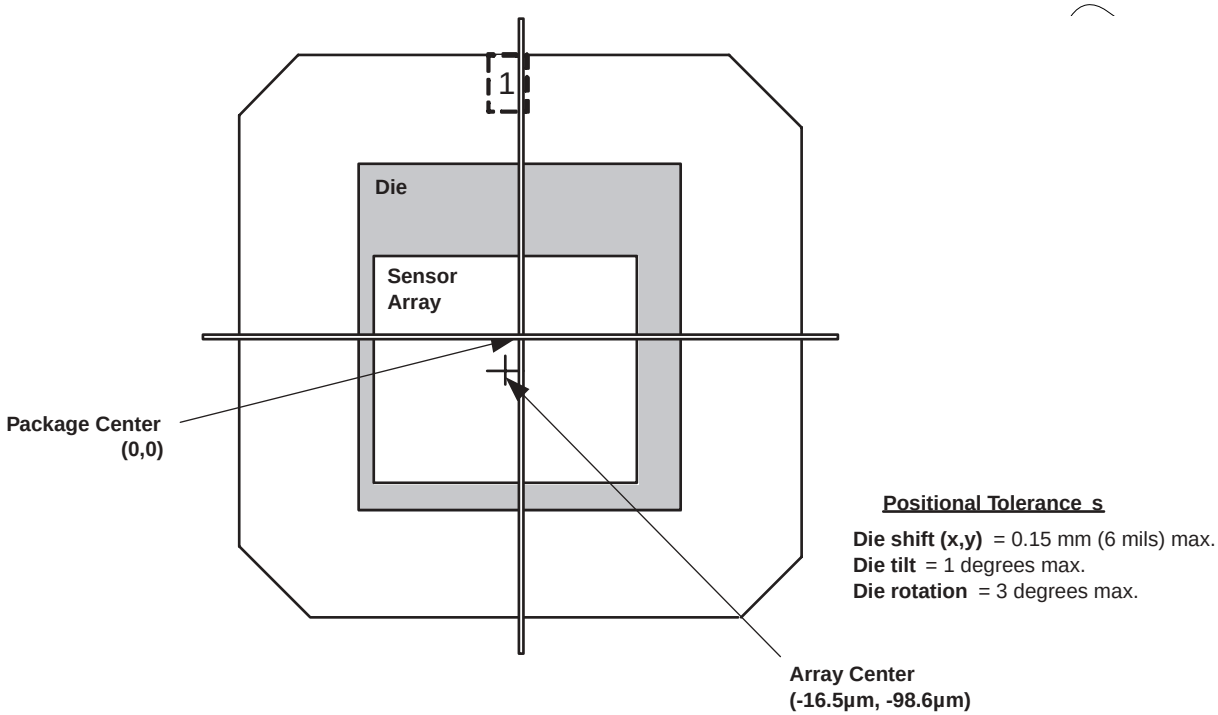


Table 17 OV7635/OV7135 Package Dimensions

Dimensions	Millimeters (mm)	Inches (in.)
Package Size	10.16 + 0.25 / -0.13 SQ	.400 +.01 / -.005 SQ
Package Height	2.24 ± 0.28	.088 ± .011
Substrate Height	0.51 ± 0.05	.020 ± .002
Cavity Size	6.99 ± 0.15 SQ	.275 ± .006 SQ
Castellation Height	1.14 ± 0.13	.045 ± .005
Pin #1 Pad Size	0.51 x 2.16	.020 x .085
Pad Size	0.51 x 1.02	.020 x .04
Pad Pitch	1.27 ± 0.10	.050 ± .004
Package Edge to First Lead Center	1.91 ± 0.25	.075 ± .01
End-to-End Pad Center-Center	6.35 ± 0.13	.250 ± .005
Glass Size	9.50 ± 0.10 SQ	.374 ± .004 SQ
Glass Height	0.55 ± 0.05	.022 ± .002

Sensor Array Center

Figure 21 OV7635/OV7135 Sensor Array Center



NOTES: 1. This drawing is not to scale and is for reference only.

2. As most optical assemblies invert and mirror the image, the chip is typically mounted with pin one oriented down on the PCB.

Note:

- *All information shown herein is current as of the revision and publication date. Please refer to the OmniVision web site (http://www.ovt.com) to obtain the current versions of all documentation.*

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