NEC

MOS INTEGRATED CIRCUIT

μPD789022,789024,789025,789026

8-BIT SINGLE-CHIP MICROCONTROLLER

DESCRIPTION

The μPD789022, μPD789024, μPD789025, and μPD789026 are μPD789026 Subseries products (compact general-purpose devices) of the 78K/0S Series.

These microcontrollers feature an 8-bit CPU, I/O ports, timers, a serial interface, and interrupt control circuits.

In addition, a flash memory product (μPD78F9026) that can operate within the same voltage range as the mask ROM versions, and a wide range of related development tools are available.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

μPD789026 Subseries User's Manual: U11919E
78K/0S Series User's Manual — Instruction: U11047E

FEATURES

- ROM and RAM capacity

Item / Product Name	Program Memory (ROM)	Data Memory (Internal High-Speed RAM)	Package
μPD789022	4 Kbytes	256 bytes	44-pin plastic QFP (10 × 10 mm, resin thickness: 2.7 mm) 44-pin plastic LQFP (10 × 10 mm, resin thickness: 1.4 mm)
μPD789024	8 Kbytes		
μPD789025	12 Kbytes	512 bytes	42-pin plastic shrink DIP (600 mils) 44-pin plastic QFP (10 × 10 mm, resin thickness: 2.7 mm) 44-pin plastic LQFP (10 × 10 mm, resin thickness: 1.4 mm)
μPD789026	16 Kbytes		

- Minimum instruction execution time can be changed from high-speed (0.4 μs) to low-speed (1.6 μs) (@ 5.0-MHz operation with system clock)
- I/O ports: 34
- Serial interface: 1 channel
  3-wire serial I/O mode/UART mode can be selected
- Timer: 3 channels
  - 16-bit timer counter: 1 channel
  - 8-bit timer/event counter: 1 channel
  - Watchdog timer: 1 channel
- Power supply voltage: V_{DD} = 1.8 to 5.5 V

APPLICATIONS

Compact household appliances, car accessories, air conditioners, games, etc.

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Printed in Japan

The mark ★ shows major revised points.

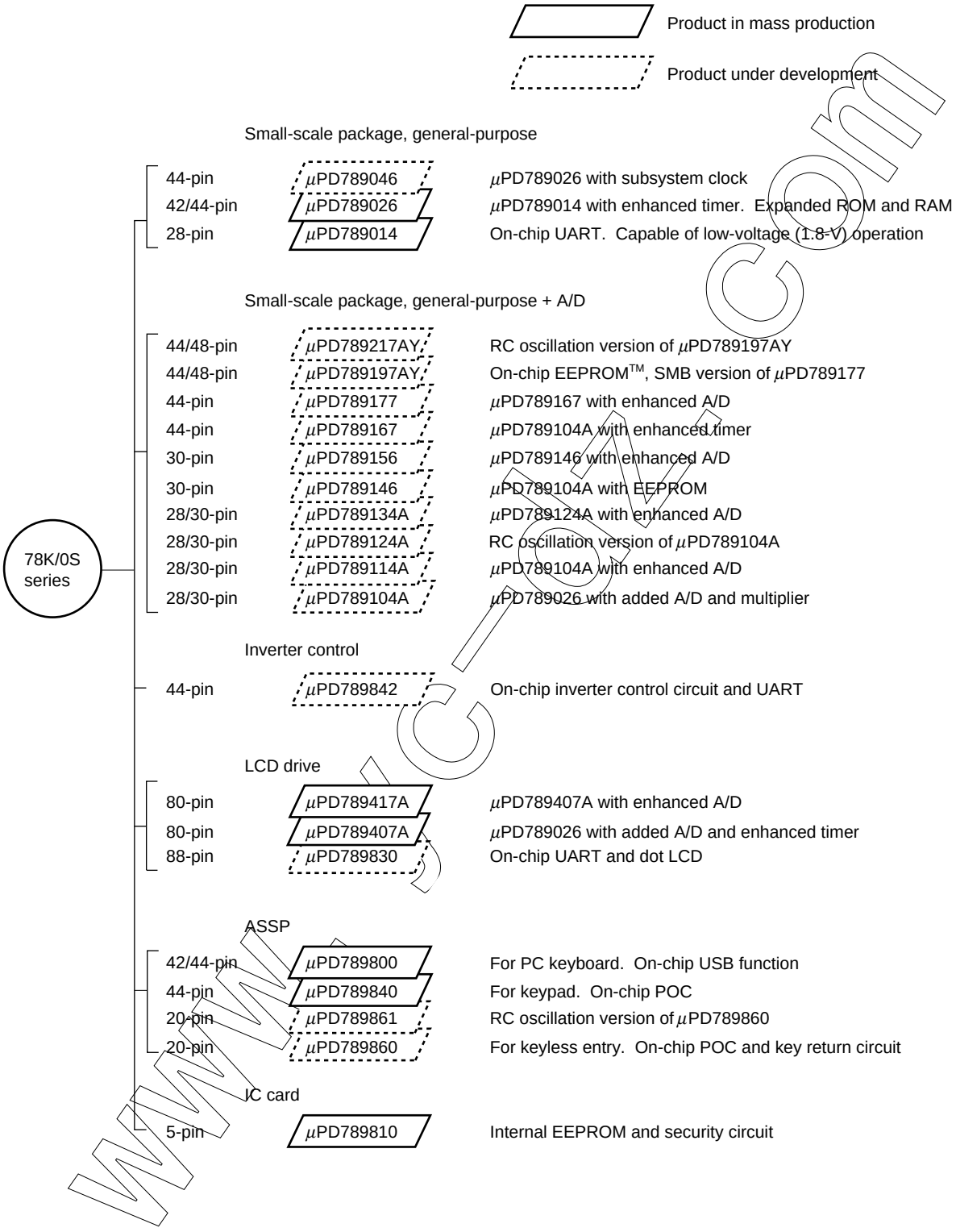
★ ORDERING INFORMATION

Part Number	Package
μPD789022GB-×××-3BS-MTX	44-pin plastic QFP (10 × 10 mm, resin thickness: 2.7 mm)
μPD789022GB-×××-8ES	44-pin plastic LQFP (10 × 10 mm, resin thickness: 1.4 mm)
μPD789024GB-×××-3BS-MTX	44-pin plastic QFP (10 × 10 mm, resin thickness: 2.7 mm)
μPD789024GB-×××-8ES	44-pin plastic LQFP (10 × 10 mm, resin thickness: 1.4 mm)
μPD789025CU-×××	42-pin plastic shrink DIP (600 mils)
μPD789025GB-×××-3BS-MTX	44-pin plastic QFP (10 × 10 mm, resin thickness: 2.7 mm)
μPD789025GB-×××-8ES	44-pin plastic LQFP (10 × 10 mm, resin thickness: 1.4 mm)
μPD789026CU-×××	42-pin plastic shrink DIP (600 mils)
μPD789026GB-×××-3BS-MTX	44-pin plastic QFP (10 × 10 mm, resin thickness: 2.7 mm)
μPD789026GB-×××-8ES	44-pin plastic LQFP (10 × 10 mm, resin thickness: 1.4 mm)

Remark ××× indicates ROM code suffix.

⋆ 78K/0S SERIES LINEUP

The products in the 78K/0S Series are listed below. The names enclosed in boxes are subseries names.



The major functional differences among the subseries are listed below.

Subseries Name \ Function		ROM Capacity	Timer				8-bit A/D	10-bit A/D	Serial Interface	I/O	V_{DD} MIN Value	Remark
			8-bit	16-bit	Watch	WDT						
Small-scale package, general-purpose	μPD789046	16 K	1 ch	1 ch	1 ch	1 ch	—	—	1 ch (UART:1 ch)	34	1.8 V	—
	μPD789026	4 K to 16 K			—							
	μPD789014	2 K to 4 K	2 ch	—						22		
Small-scale package, general-purpose + A/D	μPD789217AY	16 K to 24 K	3 ch	1 ch	1 ch	1 ch	—	8 ch	2 ch (UART: 1 ch, SMB: 1 ch)	31	1.8 V	RC oscillation version, internal EEPROM
	μPD789197AY											Internal EEPROM
	μPD789177								1 ch (UART: 1 ch)			—
	μPD789167						8 ch	—				
	μPD789156	8 K to 16 K	1 ch		—		—	4 ch		20		Internal EEPROM
	μPD789146						4 ch	—				
	μPD789134A	2 K to 8 K					—	4 ch				RC oscillation version
	μPD789124A						4 ch	—				
	μPD789114A						—	4 ch				—
	μPD789104A						4 ch	—				
Inverter control	μPD789842	8 K to 16 K	3 ch	**Note**	1 ch	1 ch	8 ch	—	1 ch (UART: 1 ch)	30	4.0 V	—
LCD drive	μPD789417A	12 K to 24 K	3 ch	1 ch	1 ch	1 ch	—	7 ch	1 ch (UART: 1 ch)	43	1.8 V	—
	μPD789407A						7 ch	—				
	μPD789830	24 K	1 ch				—			30	2.7 V	
ASSP	μPD789800	8 K	2 ch	1 ch	—	1 ch	—	—	2 ch (USB: 1 ch)	31	4.0 V	—
	μPD789840						4 ch		1 ch	29	2.8 V	
	μPD789861	4 K		—			—		—	14	1.8 V	RC oscillation version
	μPD789860											—
IC card	μPD789810	6 K	—		—	1 ch	—	—	—	1	2.7 V	Internal EEPROM

Note 10-bit timer: 1 channel

OVERVIEW OF FUNCTIONS

Item		μPD789022	μPD789024	μPD789025	μPD789026
Internal memory	ROM	4 Kbytes	8 Kbytes	12 Kbytes	16 Kbytes
	High-speed RAM	256 bytes		512 bytes	
Minimum instruction execution time		0.4 μs/1.6 μs (@ 5.0-MHz operation with system clock)			
General-purpose registers		8 bits × 8 registers			
Instruction set		• 16-bit operation • Bit manipulation (set, reset, test), etc.			
I/O ports		Total: 34 • CMOS input/output: 34			
Serial interface		• 3-wire serial I/O mode/UART mode selectable: 1 channel			
Timer		• 16-bit timer counter: 1 channel • 8-bit timer/event counter: 1 channel • Watchdog timer: 1 channel			
Timer outputs		2 outputs			
Vectored interrupt sources	Maskable interrupts	Internal: 5, External: 4			
	Non-maskable interrupt	Internal: 1			
Power supply voltage		V_{DD} = 1.8 to 5.5 V			
Operating ambient temperature		T_A = –40 to +85°C			
★ Packages		• 44-pin plastic QFP (10 × 10 mm, resin thickness 2.7 mm) • 44-pin plastic LQFP (10 × 10 mm, resin thickness 1.4 mm)		• 42-pin plastic shrink DIP (600 mils) • 44-pin plastic QFP (10 × 10 mm, resin thickness 2.7 mm) • 44-pin plastic LQFP (10 × 10 mm, resin thickness 1.4 mm)	

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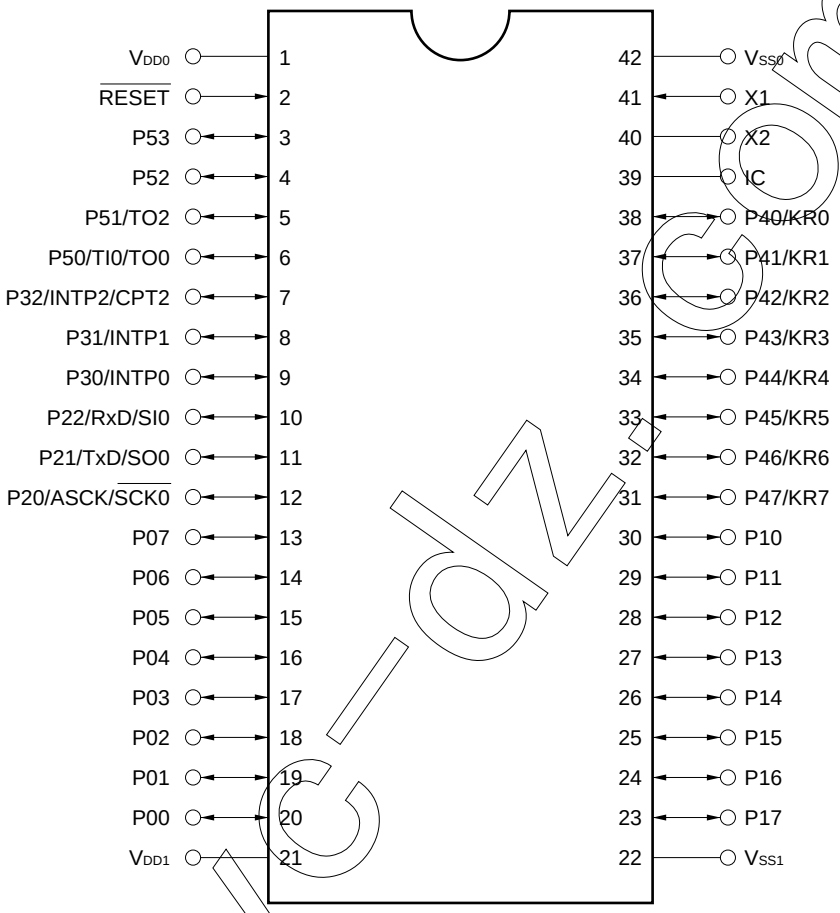
1. PIN CONFIGURATION (TOP VIEW)

- **42-pin plastic shrink DIP (600 mils)**
  μPD789025CU-×××
  μPD789026CU-×××

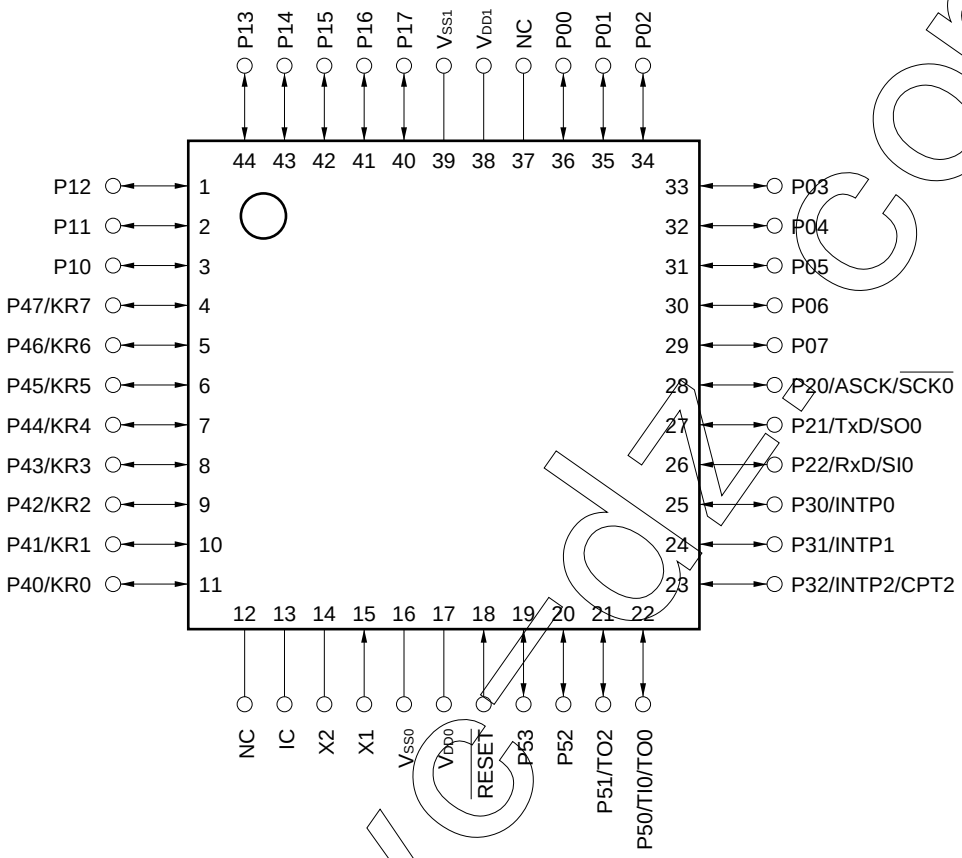


Caution Connect the IC (internally connected) pin directly to V_{SS0} or V_{SS1}.

★ • **44-pin plastic QFP**
(10 × 10 mm, resin thickness 2.7 mm)
μPD789022GB-×××-3BS-MTX
μPD789024GB-×××-3BS-MTX
μPD789025GB-×××-3BS-MTX
μPD789026GB-×××-3BS-MTX

• **44-pin plastic LQFP**
(10 × 10 mm, resin thickness 1.4 mm)
μPD789022GB-×××-8ES
μPD789024GB-×××-8ES
μPD789025GB-×××-8ES
μPD789026GB-×××-8ES

★



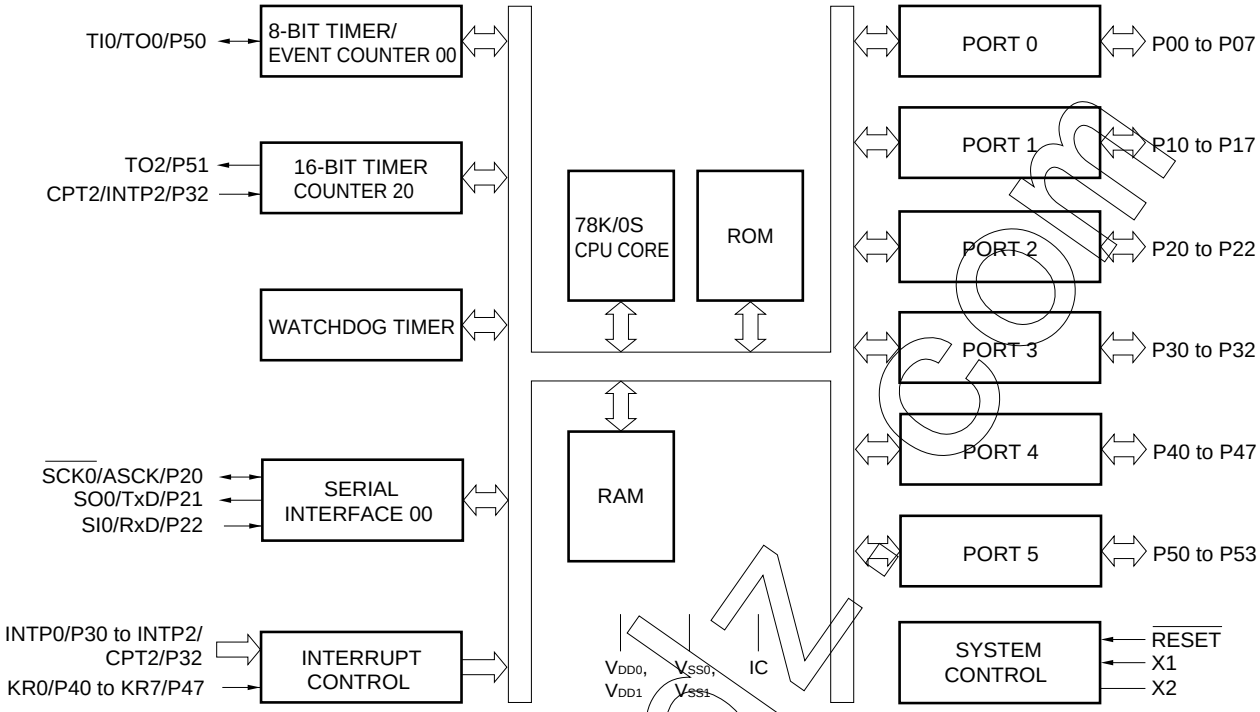
★

Caution Connect the IC (internally connected) pin directly to V_{SS0} or V_{SS1}.

ASCK:	Asynchronous Serial Clock
CPT2:	Capture Trigger Input
IC:	Internally Connected
INTP0 to INTP2:	Interrupt from Peripherals
KR0 to KR7:	Key Return
NC:	Non-connection
P00 to P07:	Port 0
P10 to P17:	Port 1
P20 to P22:	Port 2
P30 to P32:	Port 3
P40 to P47:	Port 4
P50 to P53:	Port 5

$\overline{\text{RESET}}$:	Reset
RxD:	Receive Data
$\overline{\text{SCK0}}$:	Serial Clock
SI0:	Serial Input
SO0:	Serial Output
TI0:	Timer Input
TO0, TO2:	Timer Output
TxD:	Transmit Data
V_{DD0}, V_{DD1}:	Power Supply
V_{SS0}, V_{SS1}:	Ground
X1, X2:	Crystal

2. BLOCK DIAGRAM



Remark The internal ROM and high-speed RAM capacities vary depending on the product.

3. PIN FUNCTIONS

3.1 Port Pins

Pin Name	I/O	Function	After Reset	Alternate Function
P00 to P07	I/O	Port 0 8-bit input/output port Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software. LEDs can be driven directly.	Input	—
P10 to P17	I/O	Port 1 8-bit input/output port Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software. LEDs can be driven directly.	Input	—
P20	I/O	Port 2 3-bit input/output port Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software. LEDs can be driven directly.	Input	ASCK/ $\overline{\text{SCK0}}$
P21				TxD/SO0
P22				RxD/SI0
P30	I/O	Port 3 3-bit input/output port Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software. LEDs can be driven directly.	Input	INTP0
P31				INTP1
P32				INTP2/CPT2
P40 to P47	I/O	Port 4 8-bit input/output port Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software. LEDs can be driven directly.	Input	KR0 to KR7
P50	I/O	Port 5 4-bit input/output port Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software. LEDs can be driven directly.	Input	TI0/TO0
P51				TO2
P52, P53				—

3.2 Non-Port Pins

Pin Name	I/O	Function	After Reset	Alternate Function
INTP0	Input	External interrupt input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified	Input	P30
INTP1				P31
INTP2				P32/CPT2
SI0	Input	Serial interface serial data input	Input	P22/RxD
SO0	Output	Serial interface serial data output	Input	P21/TxD
$\overline{SCK0}$	I/O	Serial interface serial clock input/output	Input	P20/ASCK
RxD	Input	Asynchronous serial interface serial data input	Input	P22/SI0
TxD	Output	Asynchronous serial interface serial data output	Input	P21/SO0
ASCK	Input	Asynchronous serial interface serial clock input	Input	P20/ $\overline{SCK0}$
TI0	Input	External count clock input to 8-bit timer (TM00)	Input	P50/TO0
TO0	Output	8-bit timer (TM00) output	Input	P50/TI0
TO2	Output	16-bit timer (TM20) output	Input	P51
CPT2	Input	Capture edge input pin	Input	P32/INTP2
KR0 to KR7	Input	Key return signal detection pin	Input	P40 to P47
$\overline{RESET}$	Input	System reset input	Input	—
X1	Input	Connecting crystal resonator for system clock oscillation	—	—
X2	—		—	—
★ V_{DD0}	—	Positive power supply of ports	—	—
★ V_{DD1}	—	Positive power supply (except ports)	—	—
IC	—	Internally connected. Connect directly to V_{SS0} or V_{SS1}.	—	—
NC	—	Not internally connected. Leave open.	—	—
★ V_{SS0}	—	Ground potential of ports	—	—
★ V_{SS1}	—	Ground potential (except ports)	—	—

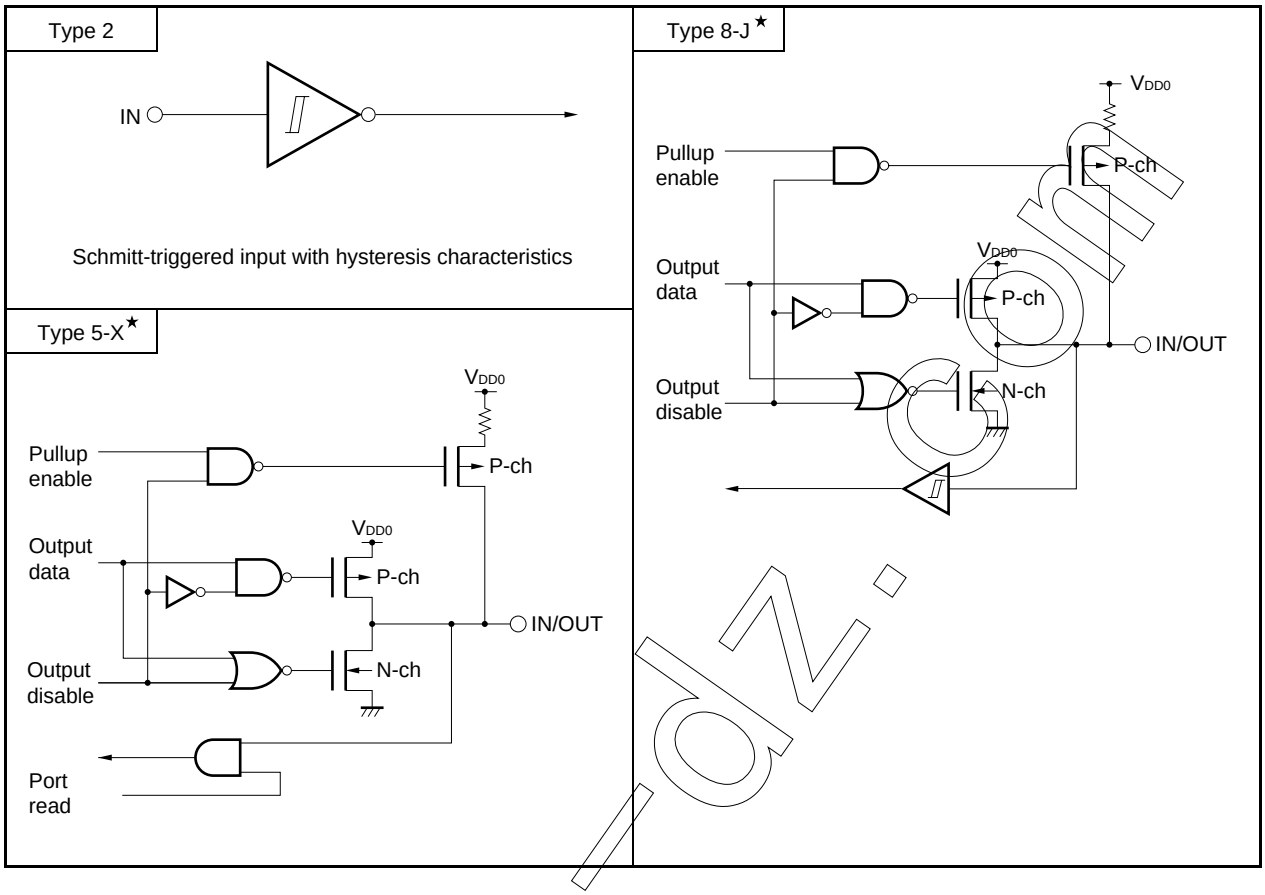
3.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The input/output circuit type of each pin and recommended connection of unused pins are shown in Table 3-1.
For the input/output circuit configuration of each type, refer to Figure 3-1.

★ **Table 3-1. Types of Input/Output Circuits and Recommended Connection of Unused Pins**

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P00 to P07	5-X	I/O	Input: Independently connect to V_{DD0} or V_{DD1}, or V_{SS0} or V_{SS1} via a resistor. Output: Leave open.
P10 to P17			
P20/ASCK/$\overline{SCK0}$	8-J		
P21/TxD/SO0	5-X		
P22/RxD/SI0	8-J		
P30/INTP0			
P31/INTP1			
P32/INTP2/CPT2			
P40/KR0 to P47/KR7			
P50/TI0/TO0			
P51/TO2	5-X		
P52, P53			
$\overline{RESET}$	2	Input	—
NC	—	—	Leave open.
IC			Connect directly to V_{SS0} or V_{SS1}.

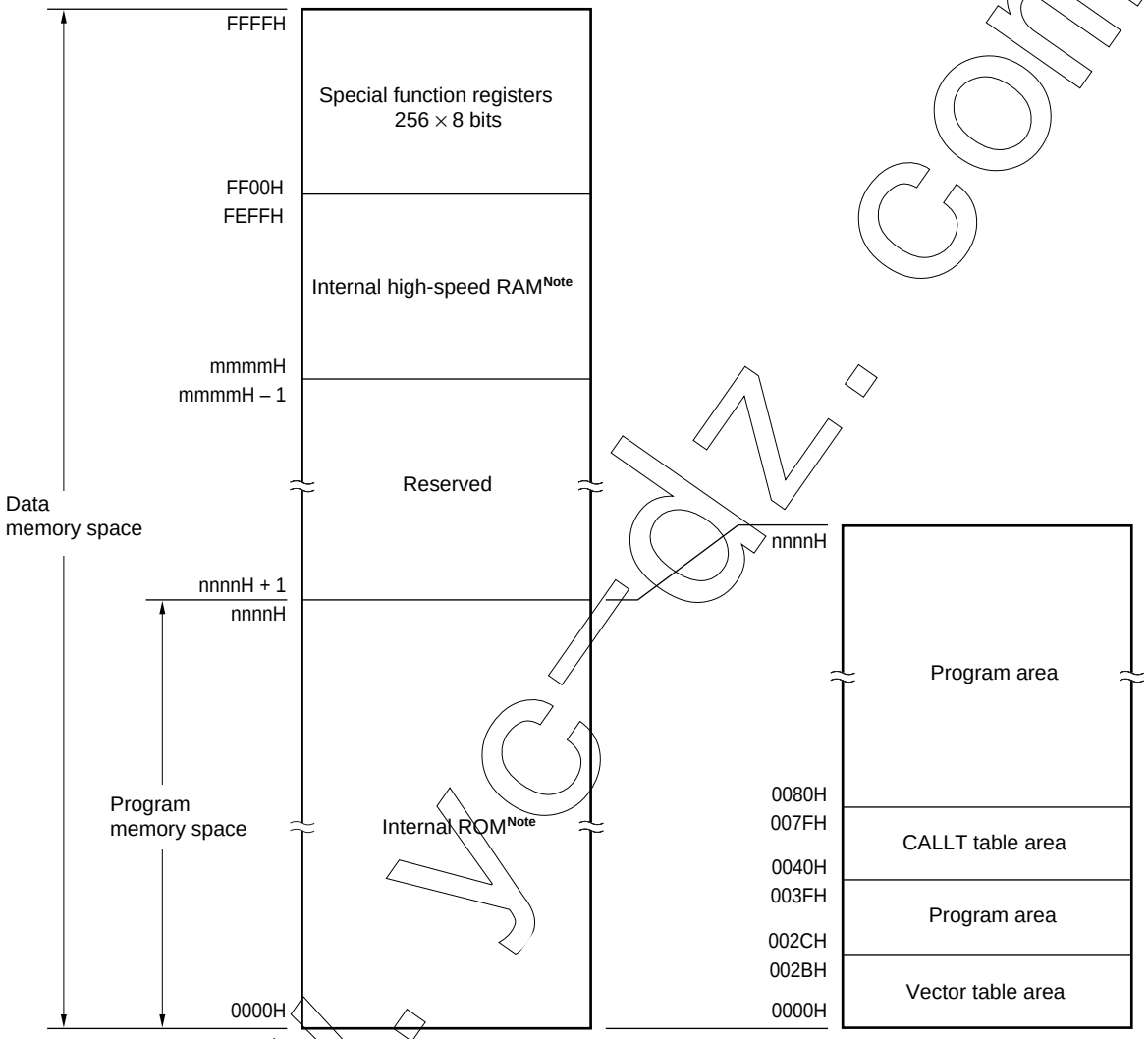
Figure 3-1. Pin Input/Output Circuits



4. MEMORY SPACE

The μPD789022, μPD789024, μPD789025, and μPD789026 can each access up to 64 Kbytes of memory space. Figure 4-1 shows the memory map.

Figure 4-1. Memory Map



Note The internal ROM and high-speed RAM capacities vary depending on the product (See the following table).

Part Number	Last Address of Internal ROM nnnnH	Start Address of Internal High-Speed RAM mmmmH
μPD789022	0FFFH	FE00H
μPD789024	1FFFH	
μPD789025	2FFFH	FD00H
μPD789026	3FFFH	

5. PERIPHERAL HARDWARE FUNCTIONS

5.1 Ports

The μPD789022, μPD789024, μPD789025, and μPD789026 are provided with the ports shown below. These ports are used to enable several types of control.

Table 5-1. Port Functions

Port Name	Pin Name	Function
Port 0	P00 to P07	I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software. LEDs can be driven directly.
Port 1	P10 to P17	I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software. LEDs can be driven directly.
Port 2	P20 to P22	I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software. LEDs can be driven directly.
Port 3	P30 to P32	I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software. LEDs can be driven directly.
Port 4	P40 to P47	I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software. LEDs can be driven directly.
Port 5	P50 to P53	I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software. LEDs can be driven directly.

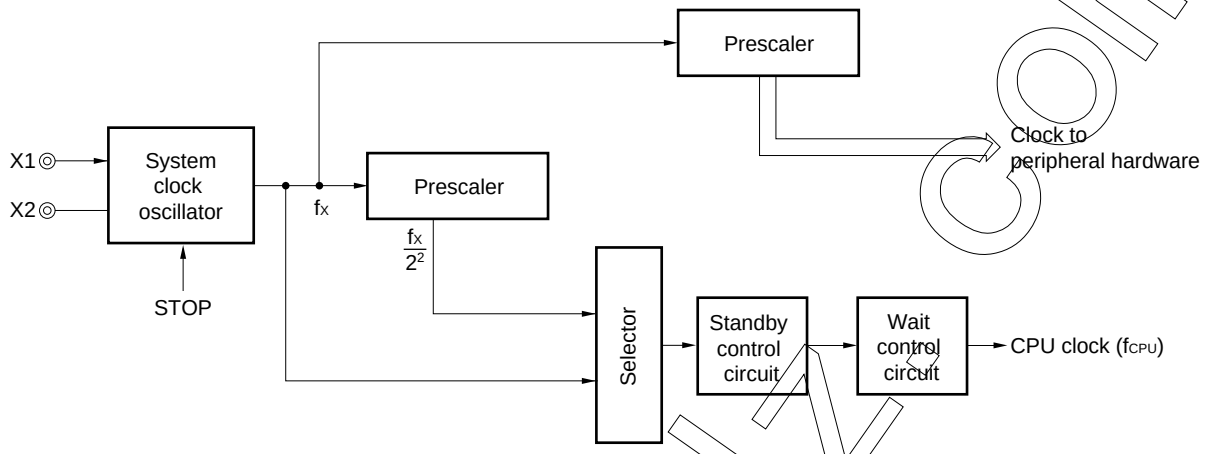
5.2 Clock Generator

An on-chip system-clock generator is provided.

The minimum instruction execution time can be changed.

- 0.4 μs/1.6 μs (@ 5.0-MHz operation with system clock)

Figure 5-1. Clock Generator Block Diagram



5.3 Timer

Three timer channels are incorporated.

- 16-bit timer counter 20: 1 channel
- 8-bit timer/event counter 00: 1 channel
- Watchdog timer: 1 channel

Table 5-2. Timer Operation

		16-Bit Timer Counter 20	8-Bit Timer/ Event Counter 00	Watchdog Timer
Operation mode	Interval timer	1 channel	1 channel	1 channel
	External event counter	—	1 channel	—
Function	Timer output	1 output	1 output	—
	Capture	1 input	—	—
	Square wave output	—	1 output	—
	Interrupt request	1	1	1

Figure 5-2. Block Diagram of 16-Bit Timer Counter 20 (TM20)

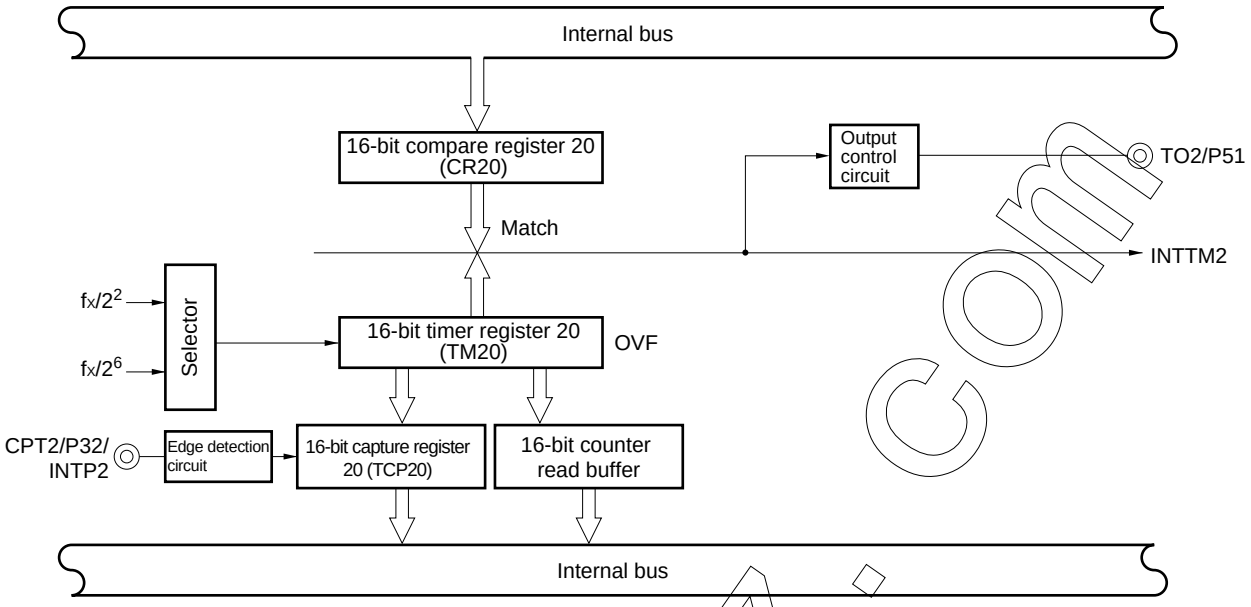


Figure 5-3. Block Diagram of 8-Bit Timer/Event Counter 00 (TM00)

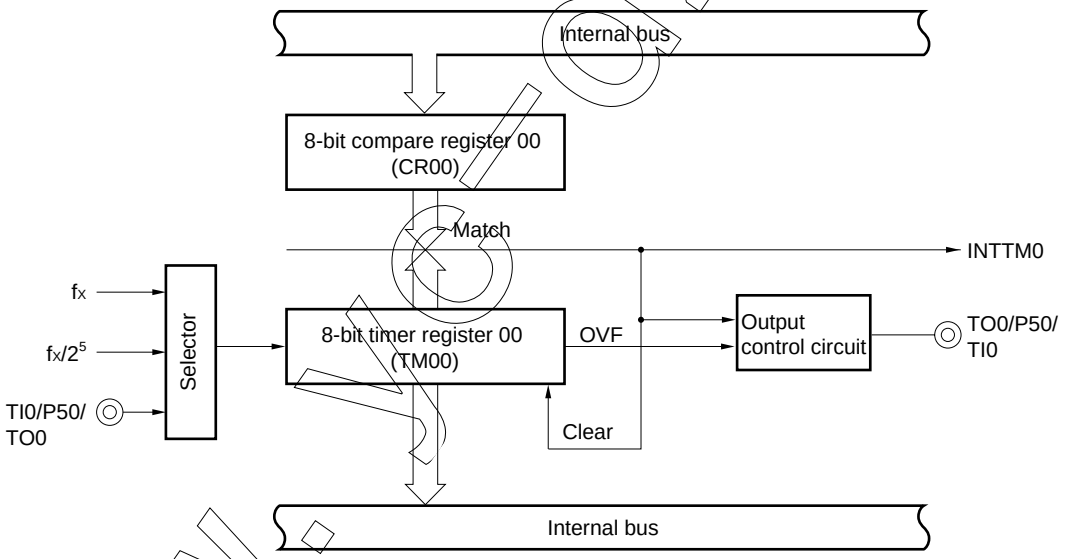
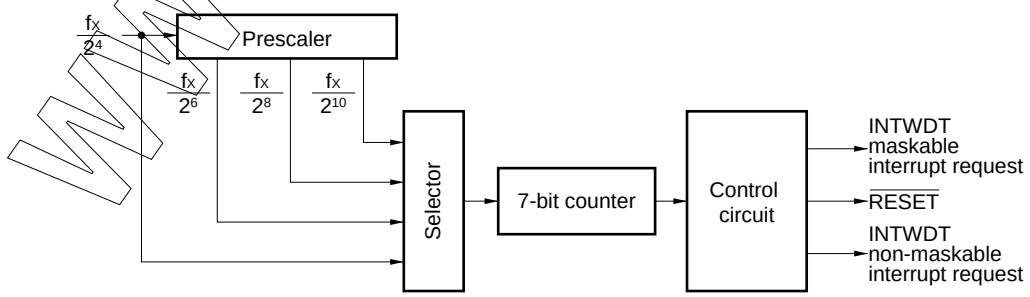


Figure 5-4. Watchdog Timer Block Diagram



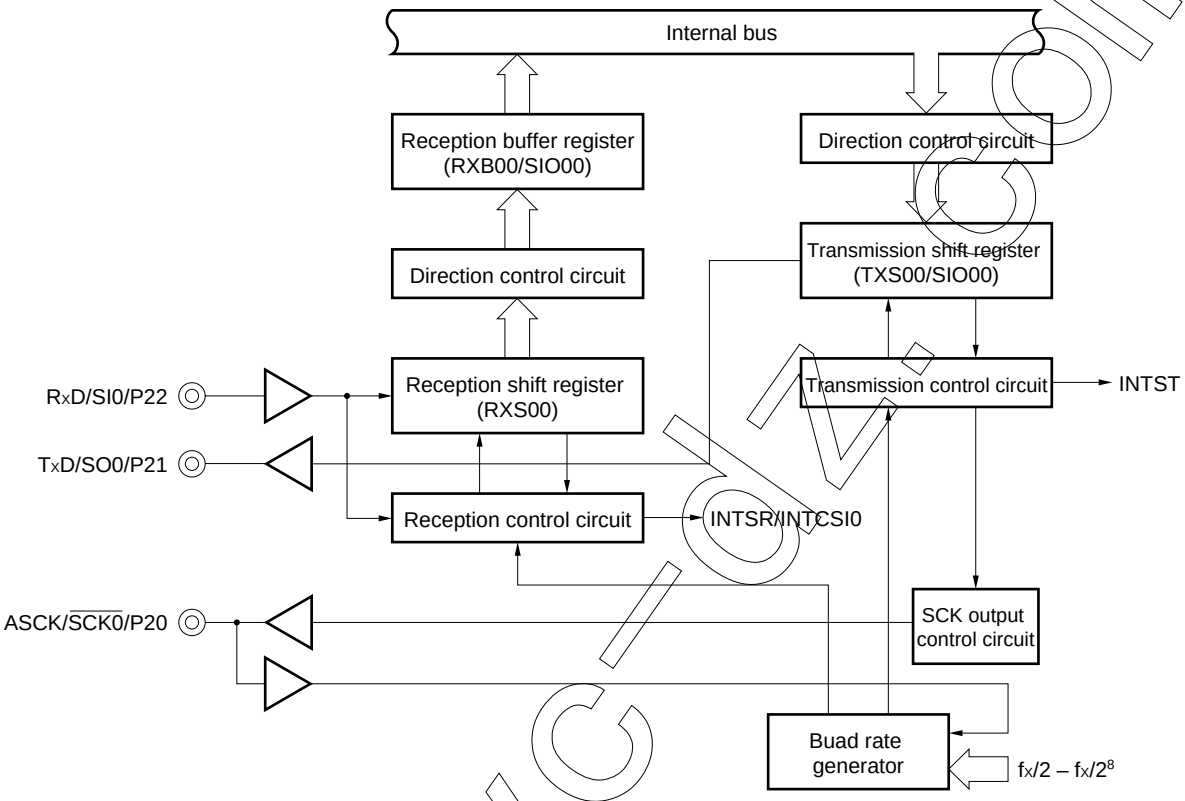
5.4 Serial Interface

One-channel serial interface is incorporated.

Serial interface 00 supports the following two modes:

- 3-wire serial I/O mode: MSB-first or LSB-first switching possible
- Asynchronous serial interface (UART) mode: On-chip dedicated baud rate generator provided

Figure 5-5. Block Diagram of Serial Interface 00



6. INTERRUPT FUNCTION

A total of 10 interrupt sources are provided, divided into the following two types.

- Non-maskable interrupts: 1 source
- Maskable interrupts: 9 sources

Table 6-1. List of Interrupt Sources

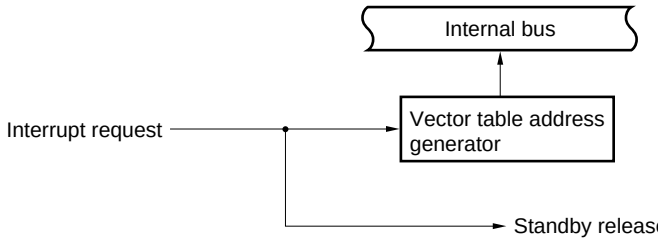
Interrupt Type	Priority[Note 1]	Interrupt Source		Internal/External	Vector Table Address	Basic Configuration Type[Note 2]
		Name	Trigger			
Non-maskable	—	INTWDT	Watchdog timer overflow (with watchdog timer mode 1 selected)	Internal	0004H	(A)
Maskable	0	INTWDT	Watchdog timer overflow (with interval timer mode selected)			(B)
	1	INTP0	Pin input edge detection	External	0006H	(C)
	2	INTP1			0008H	
	3	INTP2			000AH	
	4	INTSR	End of serial interface 00 UART reception	Internal	000CH	(B)
		INTCSI0	End of serial interface 00 3-wire SIO transfer reception			
	5	INTST	End of serial interface 00 UART transmission		000EH	
	6	INTTM0	Generation of matching signal of 8-bit timer/event counter 00		0010H	
	7	INTTM2	Generation of matching signal of 16-bit timer 20		0014H	
	8	INTKR	Key return signal detection	External	002AH	(C)

Notes 1. Default priority is the priority order when two or more maskable interrupt requests are generated at the same time. 0 is the highest order and 20 is the lowest order.

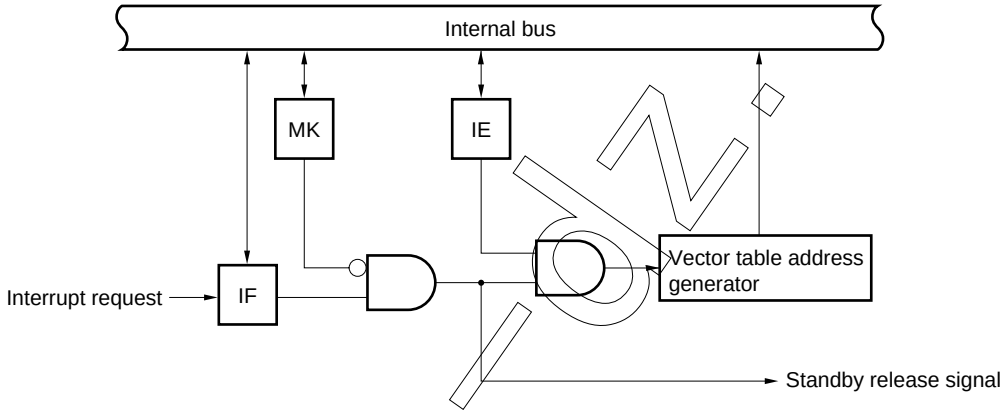
2. Basic configuration types (A), (B), and (C) correspond to (A), (B), and (C) in Figure 6-1.

Figure 6-1. Basic Configuration of Interrupt Function

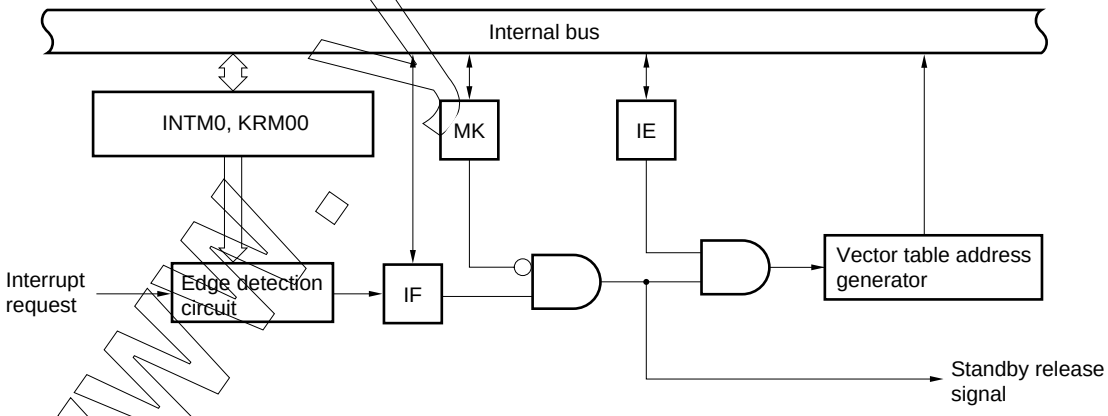
(A) Internal non-maskable interrupt



(B) Internal maskable interrupt



(C) External maskable interrupt



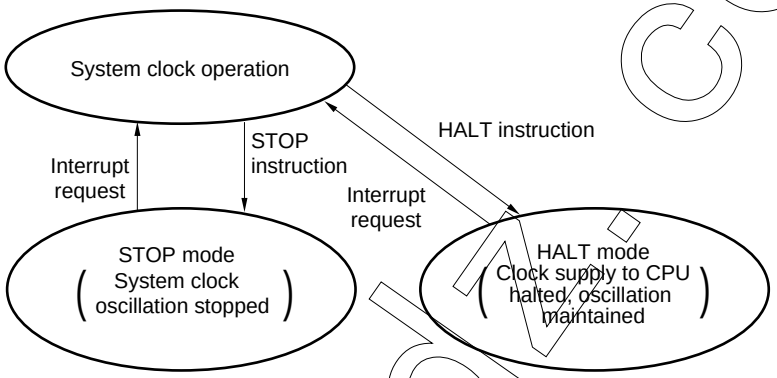
IF: Interrupt request flag
IE: Interrupt enable flag
MK: Interrupt mask flag
INTM0: External interrupt mode register 0
KRM00: Key return mode register 00

7. STANDBY FUNCTION

The following two standby modes are available for further reduction of system current consumption.

- HALT mode: In this mode, the CPU operation clock is stopped. The average current consumption can be reduced by intermittent operation by combining this mode with the normal operation.
- STOP mode: In this mode, oscillation of the system clock is stopped. All operations performed on the system clock are suspended resulting in extremely small power consumption.

Figure 7-1. Standby Function



8. RESET FUNCTION

The following two reset methods are available.

- External reset by $\overline{\text{RESET}}$ signal input
- Internal reset by watchdog timer runaway time detection

9. INSTRUCTION SET OVERVIEW

The instruction set for the μPD789022, μPD789024, μPD789025, and μPD789026 is listed later in this section.

9.1 Conventions

9.1.1 Operand formats and descriptions

The description made in the operand field of each instruction conforms to the operand format for the instructions listed below (the details conform to the assembly specification). If more than one operand format is listed for an instruction, one is selected. Uppercase letters, #, !, $, and [ ] are used to specify keywords, which must be written exactly as they appear. The meanings of these special characters are as follows:

- #: Immediate data specification
- $: Relative address specification
- !: Absolute address specification
- [ ]: Indirect address specification

Immediate data should be described using appropriate values or labels. The specification of values and labels must be accompanied by #, !, $, or [ ].

Operand registers, expressed as r or rp in the formats, can be described using both functional names (X, A, C, etc.) and absolute names (R0, R1, R2, and other names listed inside the parentheses in Table 9-1).

Table 9-1. Operand Formats and Descriptions

Format	Description
r	X (R0), A (R1), C (R2), B (R3), E (R4), D (R5), L (R6), H (R7)
rp	AX (RP0), BC (RP1), DE (RP2), HL (RP3)
sfr	Special function register symbol
saddr	FE20H to FF1FH: Immediate data or label
saddrp	FE20H to FF1FH: Immediate data or label (even addresses only)
addr16	0000H to FFFFH: Immediate data or label (only even address for 16-bit data transfer instructions)
addr5	0040H to 007FH: Immediate data or label (even addresses only)
word	16-bit immediate data or label
byte	8-bit immediate data or label
bit	3-bit immediate data or label

9.1.2 Descriptions of the operation field

A: A register (8-bit accumulator)
X: X register
B: B register
C: C register
D: D register
E: E register
H: H register
L: L register
AX: AX register pair (16-bit accumulator)
BC: BC register pair
DE: DE register pair
HL: HL register pair
PC: Program counter
SP: Stack pointer
PSW: Program status word
CY: Carry flag
AC: Auxiliary carry flag
Z: Zero flag
IE: Interrupt request enable flag
NMIS: Flag to indicate that a non-maskable interrupt is being handled
(): Contents of a memory location indicated by a parenthesized address or register name
X_H, X_L: Upper and lower 8 bits of a 16-bit register
∧: Logical product (AND)
∨: Logical sum (OR)
∀: Exclusive OR
—: Inverted data
addr16: 16-bit immediate data or label
jdisp8: Signed 8-bit data (displacement value)

9.1.3 Description of the flag operation field

(blank): No change
0: To be cleared to 0
1: To be set to 1
×: To be set or cleared according to the result
R: To be restored to the previous value

9.2 Operations

Mnemonic	Operand	Byte	Clock	Operation	Flag		
					Z	AC	CY
MOV	r, #byte	3	6	r ← byte			
	saddr, #byte	3	6	(saddr) ← byte			
	sfr, #byte	3	6	sfr ← byte			
	A, r Note 1	2	4	A ← r			
	r, A Note 1	2	4	r ← A			
	A, saddr	2	4	A ← (saddr)			
	saddr, A	2	4	(saddr) ← A			
	A, sfr	2	4	A ← sfr			
	sfr, A	2	4	sfr ← A			
	A, !addr16	3	8	A ← (addr16)			
	!addr16, A	3	8	(addr16) ← A			
	PSW, #byte	3	6	PSW ← byte	×	×	×
	A, PSW	2	4	A ← PSW			
	PSW, A	2	4	PSW ← A	×	×	×
	A, [DE]	1	6	A ← (DE)			
	[DE], A	1	6	(DE) ← A			
	A, [HL]	1	6	A ← (HL)			
	[HL], A	1	6	(HL) ← A			
	A, [HL + byte]	2	6	A ← (HL + byte)			
	[HL + byte], A	2	6	(HL + byte) ← A			
XCH	A, X	1	4	A ↔ X			
	A, r Note 2	2	6	A ↔ r			
	A, saddr	2	6	A ↔ (saddr)			
	A, sfr	2	6	A ↔ (sfr)			
	A, [DE]	1	8	A ↔ (DE)			
	A, [HL]	1	8	A ↔ (HL)			
	A, [HL + byte]	2	8	A ↔ (HL + byte)			
MOVW	rp, #word	3	6	rp ← word			
	AX, saddrp	2	6	AX ← (saddrp)			
	saddrp, AX	2	8	(saddrp) ← AX			
	AX, rp Note 3	1	4	AX ← rp			
	rp, AX Note 3	1	4	rp ← AX			

Notes 1. Except when r = A.

2. Except when r = A or X.

3. Only when rp = BC, DE, or HL.

Remark The instruction clock cycle is based on the CPU clock (f_{CPU}), specified by the processor clock control register (PCC).

Mnemonic	Operand	Byte	Clock	Operation	Flag		
					Z	AC	CY
XCHW	AX, rp Note	1	8	AX ↔ rp			
ADD	A, #byte	2	4	A, CY ← A + byte	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) + byte	×	×	×
	A, r	2	4	A, CY ← A + r	×	×	×
	A, saddr	2	4	A, CY ← A + (saddr)	×	×	×
	A, !addr16	3	8	A, CY ← A + (addr16)	×	×	×
	A, [HL]	1	6	A, CY ← A + (HL)	×	×	×
	A, [HL + byte]	2	6	A, CY ← A + (HL + byte)	×	×	×
ADDC	A, #byte	2	4	A, CY ← A + byte + CY	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) + byte + CY	×	×	×
	A, r	2	4	A, CY ← A + r + CY	×	×	×
	A, saddr	2	4	A, CY ← A + (saddr) + CY	×	×	×
	A, !addr16	3	8	A, CY ← A + (addr16) + CY	×	×	×
	A, [HL]	1	6	A, CY ← A + (HL) + CY	×	×	×
	A, [HL + byte]	2	6	A, CY ← A + (HL + byte) + CY	×	×	×
SUB	A, #byte	2	4	A, CY ← A – byte	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) – byte	×	×	×
	A, r	2	4	A, CY ← A – r	×	×	×
	A, saddr	2	4	A, CY ← A – (saddr)	×	×	×
	A, !addr16	3	8	A, CY ← A – (addr16)	×	×	×
	A, [HL]	1	6	A, CY ← A – (HL)	×	×	×
	A, [HL + byte]	2	6	A, CY ← A – (HL + byte)	×	×	×
SUBC	A, #byte	2	4	A, CY ← A – byte – CY	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) – byte – CY	×	×	×
	A, r	2	4	A, CY ← A – r – CY	×	×	×
	A, saddr	2	4	A, CY ← A – (saddr) – CY	×	×	×
	A, !addr16	3	8	A, CY ← A – (addr16) – CY	×	×	×
	A, [HL]	1	6	A, CY ← A – (HL) – CY	×	×	×
	A, [HL + byte]	2	6	A, CY ← A – (HL + byte) – CY	×	×	×
AND	A, #byte	2	4	A ← A ∧ byte	×		
	saddr, #byte	3	6	(saddr) ← (saddr) ∧ byte	×		
	A, r	2	4	A ← A ∧ r	×		
	A, saddr	2	4	A ← A ∧ (saddr)	×		
	A, !addr16	3	8	A ← A ∧ (addr16)	×		
	A, [HL]	1	6	A ← A ∧ (HL)	×		
	A, [HL + byte]	2	6	A ← A ∧ (HL + byte)	×		

Note Only when rp = BC, DE, or HL.

Remark The instruction clock cycle is based on the CPU clock (f_{CPU}), specified by the processor clock control register (PCC).

Mnemonic	Operand	Byte	Clock	Operation	Flag		
					Z	AC	CY
OR	A, #byte	2	4	A ← A ∨ byte	×		
	saddr, #byte	3	6	(saddr) ← (saddr) ∨ byte	×		
	A, r	2	4	A ← A ∨ r	×		
	A, saddr	2	4	A ← A ∨ (saddr)	×		
	A, !addr16	3	8	A ← A ∨ (addr16)	×		
	A, [HL]	1	6	A ← A ∨ (HL)	×		
	A, [HL + byte]	2	6	A ← A ∨ (HL + byte)	×		
XOR	A, #byte	2	4	A ← A ⊻ byte	×		
	saddr, #byte	3	6	(saddr) ← (saddr) ⊻ byte	×		
	A, r	2	4	A ← A ⊻ r	×		
	A, saddr	2	4	A ← A ⊻ (saddr)	×		
	A, !addr16	3	8	A ← A ⊻ (addr16)	×		
	A, [HL]	1	6	A ← A ⊻ (HL)	×		
	A, [HL + byte]	2	6	A ← A ⊻ (HL + byte)	×		
CMP	A, #byte	2	4	A – byte	×	×	×
	saddr, #byte	3	6	(saddr) – byte	×	×	×
	A, r	2	4	A – r	×	×	×
	A, saddr	2	4	A – (saddr)	×	×	×
	A, !addr16	3	8	A – (addr16)	×	×	×
	A, [HL]	1	6	A – (HL)	×	×	×
	A, [HL + byte]	2	6	A – (HL + byte)	×	×	×
ADDW	AX, #word	3	6	AX, CY ← AX + word	×	×	×
SUBW	AX, #word	3	6	AX, CY ← AX – word	×	×	×
CMPW	AX, #word	3	6	AX – word	×	×	×
INC	r	2	4	r ← r + 1	×	×	
	saddr	2	4	(saddr) ← (saddr) + 1	×	×	
DEC	r	2	4	r ← r – 1	×	×	
	saddr	2	4	(saddr) ← (saddr) – 1	×	×	
INCW	rp	1	4	rp ← rp + 1			
DECW	rp	1	4	rp ← rp – 1			
ROR	A, 1	1	2	(CY, A_7 ← A_0, A_{m-1} ← A_m) × 1			×
ROL	A, 1	1	2	(CY, A_0 ← A_7, A_{m+1} ← A_m) × 1			×
RORC	A, 1	1	2	(CY ← A_0, A_7 ← CY, A_{m-1} ← A_m) × 1			×
ROLC	A, 1	1	2	(CY ← A_7, A_0 ← CY, A_{m+1} ← A_m) × 1			×

Remark The instruction clock cycle is based on the CPU clock (f_{CPU}), specified by the processor clock control register (PCC).

Mnemonic	Operand	Byte	Clock	Operation	Flag		
					Z	AC	CY
SET1	saddr. bit	3	6	(saddr. bit) ← 1			
	sfr. bit	3	6	sfr. bit ← 1			
	A. bit	2	4	A. bit ← 1			
	PSW. bit	3	6	PSW. bit ← 1	×	×	×
	[HL]. bit	2	10	(HL). bit ← 1			
CLR1	saddr. bit	3	6	(saddr. bit) ← 0			
	sfr. bit	3	6	sfr. bit ← 0			
	A. bit	2	4	A. bit ← 0			
	PSW. bit	3	6	PSW. bit ← 0	×	×	×
	[HL]. bit	2	10	(HL). bit ← 0			
SET1	CY	1	2	CY ← 1			1
CLR1	CY	1	2	CY ← 0			0
NOT1	CY	1	2	CY ← $\overline{CY}$			×
CALL	!addr16	3	6	(SP – 1) ← $(PC + 3)_H$, (SP – 2) ← $(PC + 3)_L$, PC ← addr16, SP ← SP – 2			
CALLT	[addr5]	1	8	(SP – 1) ← $(PC + 1)_H$, (SP – 2) ← $(PC + 1)_L$, PC_H ← (00000000, addr5 + 1), PC_L ← (00000000, addr5), SP ← SP – 2			
RET		1	6	PC_H ← (SP + 1), PC_L ← (SP), SP ← SP + 2			
RETI		1	8	PC_H ← (SP + 1), PC_L ← (SP), PSW ← (SP + 2), SP ← SP + 3, NMIS ← 0	R	R	R
PUSH	PSW	1	2	(SP – 1) ← PSW, SP ← SP – 1			
	rp	1	4	(SP – 1) ← rp_H, (SP – 2) ← rp_L, SP ← SP – 2			
POP	PSW	1	4	PSW ← (SP), SP ← SP + 1	R	R	R
	rp	1	6	rp_H ← (SP + 1), rp_L ← (SP), SP ← SP + 2			
MOVW	SP, AX	2	8	SP ← AX			
	AX, SP	2	6	AX ← SP			
BR	!addr16	3	6	PC ← addr16			
	$addr16	2	6	PC ← PC + 2 + jdisp8			
	AX	1	6	PC_H ← A, PC_L ← X			

Remark The instruction clock cycle is based on the CPU clock (f_{CPU}), specified by the processor clock control register (PCC).

Mnemonic	Operand	Byte	Clock	Operation	Flag
					Z AC CY
BC	$addr16	2	6	PC ← PC + 2 + jdisp8 if CY = 1	
BNC	$addr16	2	6	PC ← PC + 2 + jdisp8 if CY = 0	
BZ	$addr16	2	6	PC ← PC + 2 + jdisp8 if Z = 1	
BNZ	$addr16	2	6	PC ← PC + 2 + jdisp8 if Z = 0	
BT	saddr. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if (saddr. bit) = 1	
	sfr. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if sfr. bit = 1	
	A. bit, $addr16	3	8	PC ← PC + 3 + jdisp8 if A. bit = 1	
	PSW. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if PSW. bit = 1	
BF	saddr. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if (saddr. bit) = 0	
	sfr. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if sfr. bit = 0	
	A. bit, $addr16	3	8	PC ← PC + 3 + jdisp8 if A. bit = 0	
	PSW. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if PSW. bit = 0	
DBNZ	B, $addr16	2	6	B ← B – 1, then PC ← PC + 2 + jdisp8 if B ≠ 0	
	C, $addr16	2	6	C ← C – 1, then PC ← PC + 2 + jdisp8 if C ≠ 0	
	saddr, $addr16	3	8	(saddr) ← (saddr) – 1, then PC ← PC + 3 + jdisp8 if (saddr) ≠ 0	
NOP		1	2	No Operation	
EI		3	6	IE ← 1 (Enable Interrupt)	
DI		3	6	IE ← 0 (Disable Interrupt)	
HALT		1	2	Set HALT Mode	
STOP		1	2	Set STOP Mode	

Remark The instruction clock cycle is based on the CPU clock (f_{CPU}), specified by the processor clock control register (PCC).

10. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}		–0.3 to +6.5	V
Input voltage	V_I		–0.3 to V_{DD} + 0.3	V
Output voltage	V_O		–0.3 to V_{DD} + 0.3	V
Output current, high	I_{OH}	Per pin	–10	mA
		Total for all pins	–30	mA
Output current, low	I_{OL}	Per pin	30	mA
		Total for all pins	160	mA
Operating ambient temperature	T_A		–40 to +85	°C
Storage temperature	T_{stg}		–65 to +150	°C

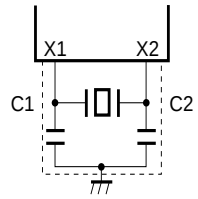
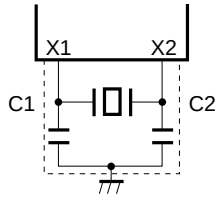
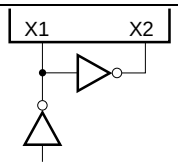
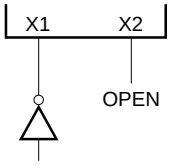
Caution Product quality may suffer if the maximum absolute ratings exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Capacitance (T_A = 25°C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz			15	pF
Output capacitance	C_{OUT}	Unmeasured pins returned to 0 V			15	pF
Input/output capacitance	C_{IO}				15	pF

System Clock Oscillator Characteristics (T_A = –40°C to +85°C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X)[Note 1]	V_{DD} = Oscillation voltage range	1.0		5.0	MHz
		Oscillation stabilization time[Note 2]	After V_{DD} reaches the oscillation voltage range MIN.			4	ms
Crystal resonator		Oscillation frequency (f_X)[Note 1]		1.0		5.0	MHz
		Oscillation stabilization time[Note 2]	V_{DD} = 4.5 to 5.5 V			10	ms
						30	
External clock		X1 input frequency (f_X)[Note 1]		1.0		5.0	MHz
★		X1 input high-/low-level width (t_{XH}, t_{XL})		85		500	ns
		X1 input frequency (f_X)[Note 1]	V_{DD} = 2.7 to 5.5 V	1.0		5.0	MHz
★		X1 input high-/low-level width (t_{XH}, t_{XL})	V_{DD} = 2.7 to 5.5 V	85		500	ns

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after reset or STOP mode release

Caution When using the system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

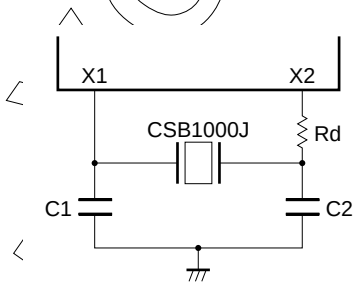
- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS0}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

Recommended Oscillator Constant

Ceramic resonator (T_A = –40°C to +85°C)

Manufacturer	Part Number	Frequency (MHz)	Recommended Circuit Constant (pF)		Oscillation Voltage Range (V_{DD})		Remarks
			C1	C2	MIN.	MAX.	
Murata Mfg. Co., Ltd.	CSB1000J[Note]	1.0	100	100	2.2	5.5	Rd = 4.7 kΩ
	CSA2.00MG040	2.0	100	100	1.8	5.5	
	CST2.00MG040		—	—			On-chip capacitor
	CSA4.19MG	4.19	100	100	1.8	5.5	
	CST4.19MGW		—	—			On-chip capacitor
	CSA5.00MG	5.0	30	30	2.0	5.5	
	CST5.00MGW		—	—			On-chip capacitor
	CSA5.00MGU		30	30	1.8	5.5	
	CST5.00MGWU		—	—			On-chip capacitor
TDK	CCR4.19MC3	4.19	—	—	2.0	5.5	On-chip capacitor
	FCR4.19MC5		—	—			On-chip capacitor
	CCR5.0MC3	5.0	—	—	2.0	5.5	On-chip capacitor
	FCR5.0MC5		—	—			On-chip capacitor

Note When the CSB1000J (1.0 MHz) manufactured by Murata Mfg. Co., Ltd. is used, a limiting resistor (Rd = 4.7 kΩ) is necessary (see the following figure). When one of other resonators is used, no limiting resistor is required.



Caution The oscillator constant and oscillation voltage range indicate conditions of stable oscillation. Oscillation frequency precision is not guaranteed. For applications requiring oscillation frequency precision, the oscillation frequency must be adjusted on the implementation circuit. For details, please contact directly the manufacturer of the resonator you will use.

DC Characteristics (T_A = –40°C to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high	I_{OH}	Per pin				–1	mA
		Total for all pins				–15	mA
Output current, low	I_{OL}	Per pin				10	mA
		Total for all pins				80	mA
Input voltage, high	V_{IH1}	P00 to P07, P10 to P17, P21, P51 to 53	V_{DD} = 2.7 to 5.5 V	0.7V_{DD}		V_{DD}	V
				0.9V_{DD}		V_{DD}	V
	V_{IH2}	P20, P22, P30 to P32, P40 to P47, P50, RESET	V_{DD} = 2.7 to 5.5 V	0.8V_{DD}		V_{DD}	V
				0.9V_{DD}		V_{DD}	V
	V_{IH3}	X1, X2		V_{DD} – 0.1		V_{DD}	V
Input voltage, low	V_{IL1}	P00 to P07, P10 to P17, P21, P51 to P53	V_{DD} = 2.7 to 5.5 V	0		0.3V_{DD}	V
				0		0.1V_{DD}	V
	V_{IL2}	P20, P22, P30 to P32, P40 to P47, P50, RESET	V_{DD} = 2.7 to 5.5 V	0		0.2V_{DD}	V
				0		0.1V_{DD}	V
	V_{IL3}	X1, X2		0		0.1	V
Output voltage, high	V_{OH}	V_{DD} = 4.5 to 5.5 V, I_{OH} = –1 mA		V_{DD} – 0.1			V
		I_{OH} = –100 μA		V_{DD} – 0.5			V
Output voltage, low	V_{OL}	V_{DD} = 4.5 to 5.5 V, I_{OL} = 10 mA				1.0	V
		I_{OL} = 400 μA				0.5	V
Input leakage current, high	I_{LIH1}	V_{IN} = V_{DD}	Pins other than X1 and X2			3	μA
	I_{LIH2}		X1, X2			20	μA
Input leakage current, low	I_{LIL1}	V_{IN} = 0 V	Pins other than X1 and X2			–3	μA
	I_{LIL2}		X1, X2			–20	μA
Output leakage current, high	I_{LOH}	V_{OUT} = V_{DD}				3	μA
Output leakage current, low	I_{LOL}	V_{OUT} = 0 V				–3	μA
Software pull-up resistor	R	V_{IN} = 0 V		50	100	200	kΩ
Supply current[Note 1]	I_{DD1}	5.0-MHz crystal oscillation operating mode	V_{DD} = 5.0 V±10%[Note 2]		1.3	2.5	mA
			V_{DD} = 3.0 V±10%[Note 3]		0.26	0.45	mA
			V_{DD} = 2.0 V±10%[Note 3]		0.14	0.30	mA
	I_{DD2}	5.0-MHz crystal oscillation HALT mode	V_{DD} = 5.0 V±10%[Note 2]		0.41	0.85	mA
			V_{DD} = 3.0 V±10%[Note 3]		0.16	0.35	mA
			V_{DD} = 2.0 V±10%[Note 3]		0.07	0.15	mA
	I_{DD3}	STOP mode	V_{DD} = 5.0 V±10%		0.1	10	μA
			V_{DD} = 3.0 V±10%		0.05	5.0	μA
			T_A = 25°C		0.05	3.0	μA
			V_{DD} = 2.0 V±10%		0.05	3.0	μA

Notes 1. The current flowing to the ports (including the current flowing through the on-chip pull-up resistors) is not included.

2. High-speed mode operation (when the processor clock control register (PCC) is set to 00H)

3. Low-speed mode operation (when PCC is set to 02H)

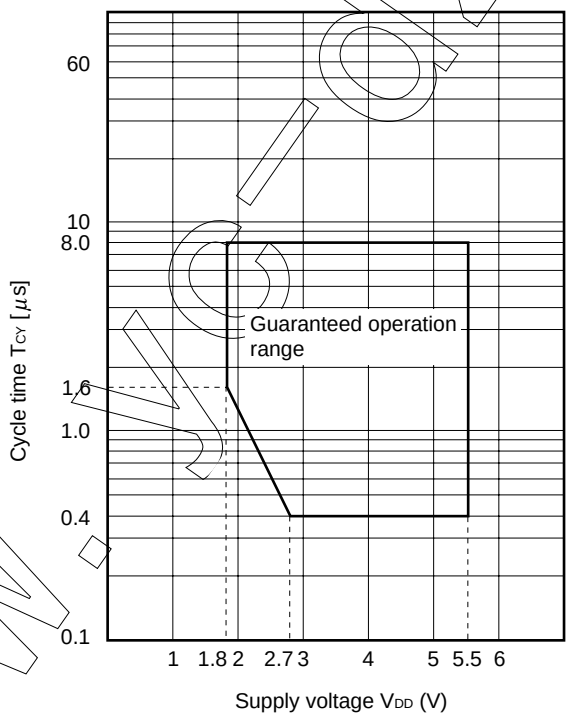
Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

AC Characteristics

(1) Basic operation (T_A = –40°C to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T_{CY}	V_{DD} = 2.7 to 5.5 V	0.4		8	μs
			1.6		8	μs
TI0 input high-/low-level width	t_{TIH}, t_{TIL}	V_{DD} = 2.7 to 5.5 V	0.1			μs
			1.8			μs
TI0 input frequency	f_{TI}	V_{DD} = 2.7 to 5.5 V	0		4	MHz
			0		275	kHz
Interrupt input high-/low-level width	t_{INTH}, t_{INTL}	INTP0 to INTP2	10			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}		10			μs

T_{CY} vs V_{DD} (system clock)



(2) Serial interface 00 (T_A = –40°C to +85°C, V_{DD} = 1.8 to 5.5 V)

(i) 3-wire serial I/O mode ($\overline{SCK0}$...Internal clock output)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY1}	V_{DD} = 2.7 to 5.5 V		800			ns
				3200			ns
$\overline{SCK0}$ high-/low-level width	t_{KH1}, t_{KL1}	V_{DD} = 2.7 to 5.5 V		t_{KCY1}/2 – 50			ns
				t_{KCY1}/2 – 150			ns
SI0 setup time (to $\overline{SCK0}$↑)	t_{SIK1}	V_{DD} = 2.7 to 5.5 V		150			ns
				500			ns
SI0 hold time (from $\overline{SCK0}$↑)	t_{KSI1}	V_{DD} = 2.7 to 5.5 V		400			ns
				600			ns
SO0 output delay time from $\overline{SCK0}$↓	t_{KSO1}	R = 1 kΩ, C =100 pF[Note]	V_{DD} = 2.7 to 5.5 V	0		250	ns
				0		1000	ns

Note R and C are the load resistance and load capacitance of the SO0 output line, respectively.

(ii) 3-wire serial I/O mode ($\overline{SCK0}$...External clock input)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
★ $\overline{SCK0}$ cycle time	t_{KCY2}	V_{DD} = 2.7 to 5.5 V		900			ns
★				3500			ns
$\overline{SCK0}$ high-/low-level width	t_{KH2}, t_{KL2}	V_{DD} = 2.7 to 5.5 V		400			ns
				1600			ns
SI0 setup time (to $\overline{SCK0}$↑)	t_{SIK2}	V_{DD} = 2.7 to 5.5 V		100			ns
				150			ns
SI0 hold time (from $\overline{SCK0}$↑)	t_{KSI2}	V_{DD} = 2.7 to 5.5 V		400			ns
				600			ns
SO0 output delay time from $\overline{SCK0}$↓	t_{KSO2}	R = 1 kΩ, C =100 pF[Note]	V_{DD} = 2.7 to 5.5 V	0		300	ns
				0		1000	ns

Note R and C are the load resistance and load capacitance of the SO0 output line, respectively.

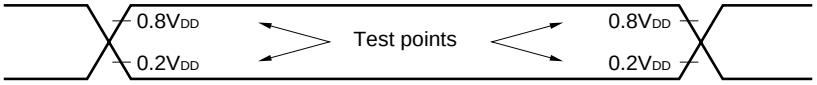
(iii) UART mode (Dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		V_{DD} = 2.7 to 5.5 V			78125	bps
					19531	bps

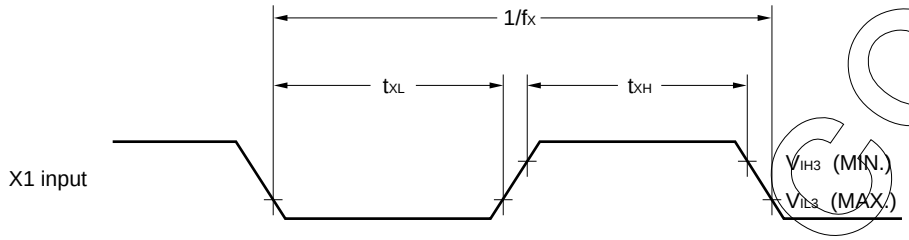
(iv) UART mode (External clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
★ ASCK cycle time	t_{KCY3}	V_{DD} = 2.7 to 5.5 V	900			ns
★			3500			ns
ASCK high-/low-level width	t_{KH3}, t_{KL3}	V_{DD} = 2.7 to 5.5 V	400			ns
			1600			ns
Transfer rate		V_{DD} = 2.7 to 5.5 V			39063	bps
					9766	bps
ASCK rise/fall time	t_R, t_F				1	μs

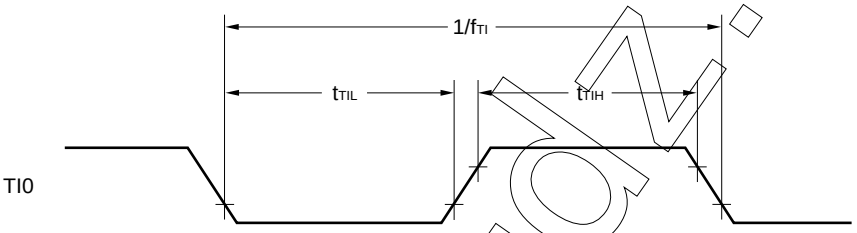
AC Timing Test Points (except the X1 input)



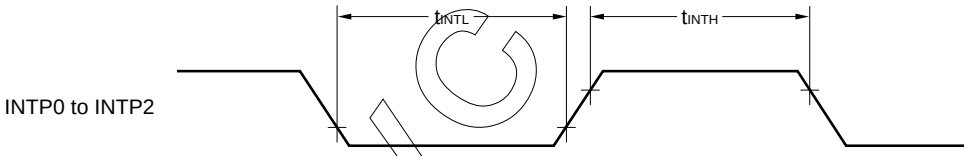
Clock Timing



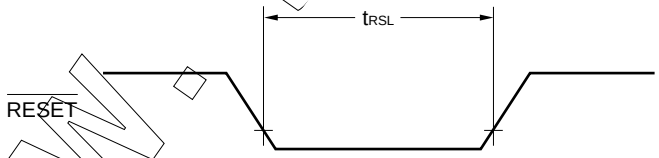
TI Timing



Interrupt Input Timing

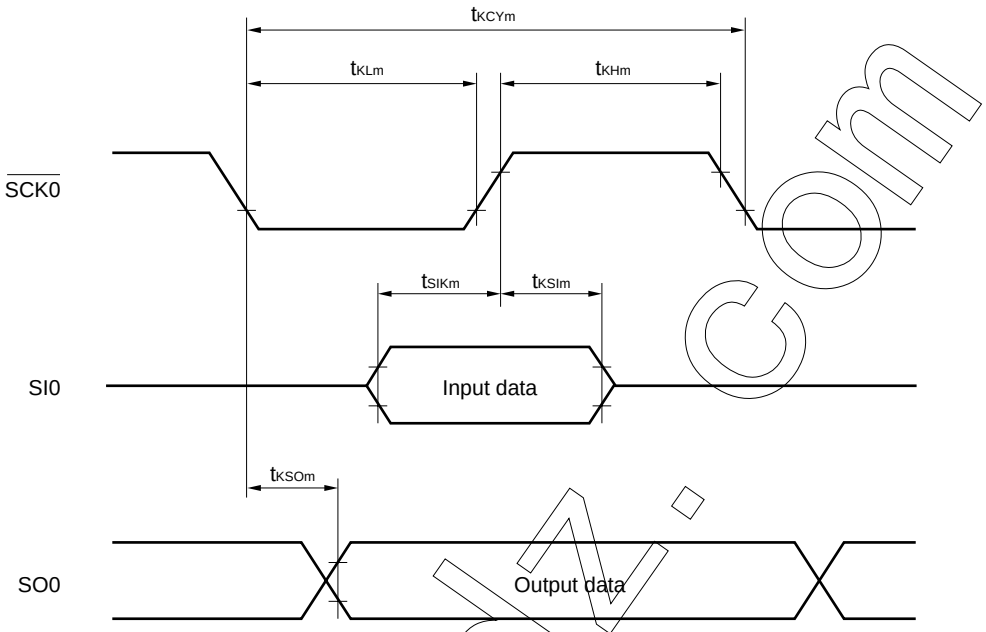


$\overline{\text{RESET}}$ Input Timing



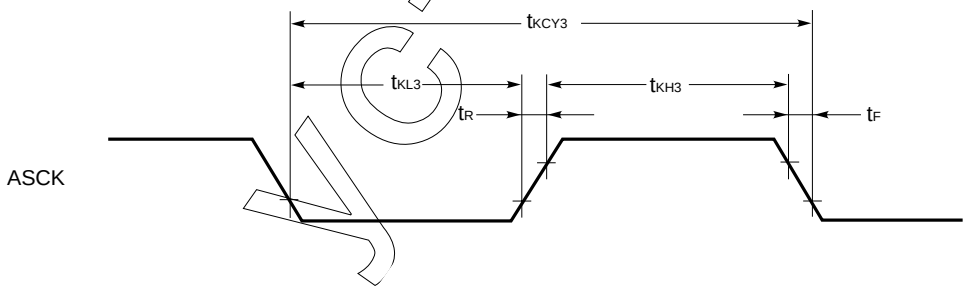
Serial Transfer Timing

3-wire serial I/O mode:



m = 1, 2

UART mode (external clock input):



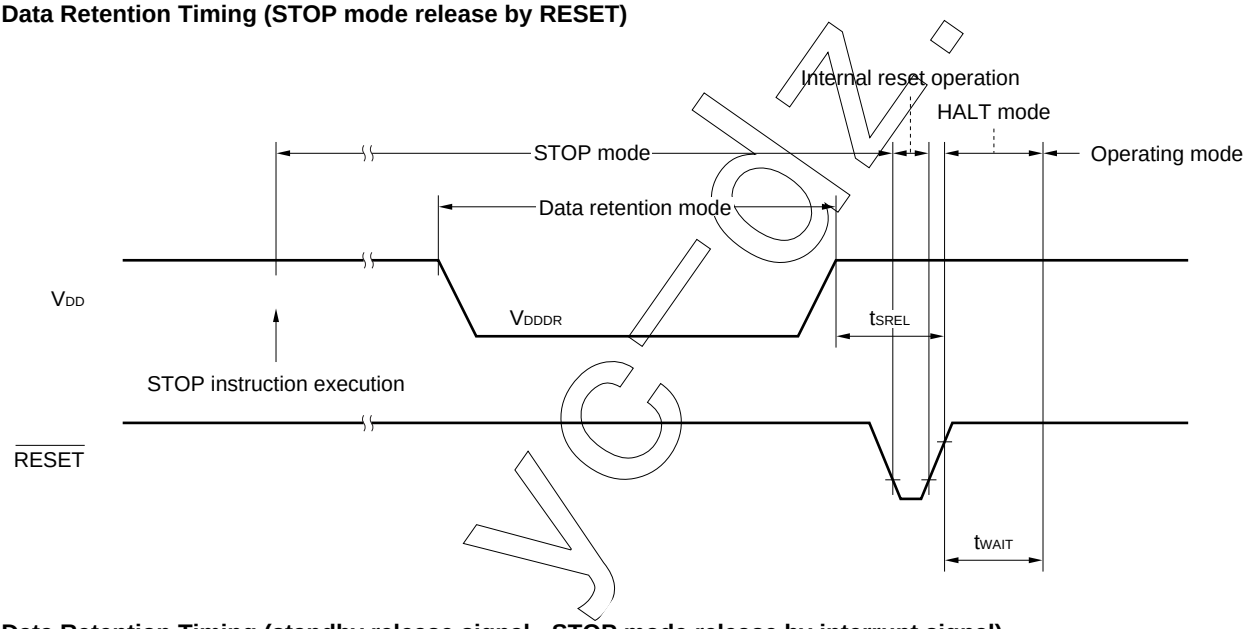
Data Memory Stop Mode Low Supply Voltage Data Retention Characteristics (T_A = –40°C to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.8		5.5	V
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time	t_{WAIT}	Release by $\overline{\text{RESET}}$		$2^{15}/f_X$		ms
		Release by interrupt		**Note**		ms

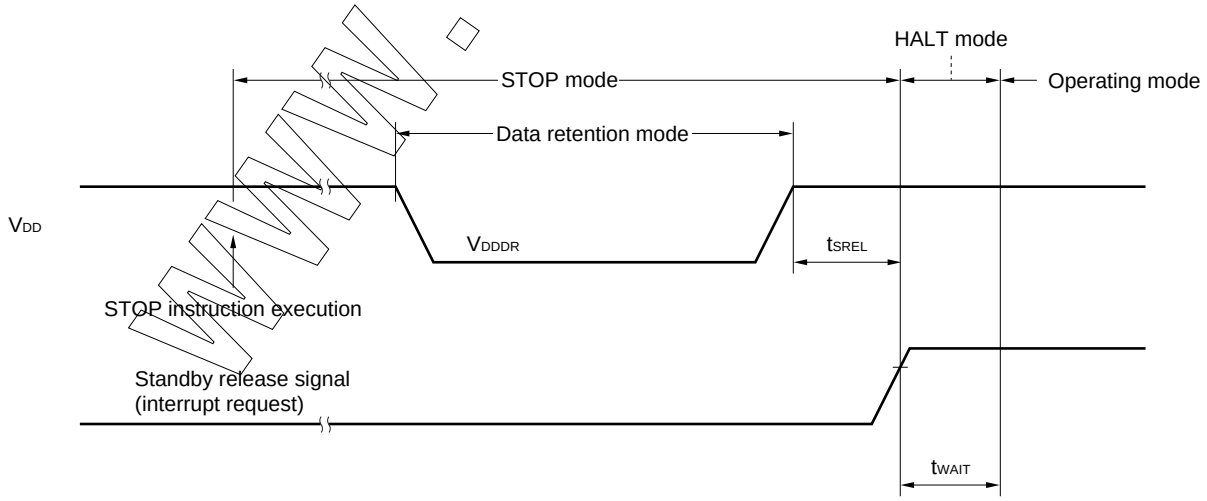
Note $2^{12}/f_X$, $2^{15}/f_X$, or $2^{17}/f_X$ can be selected according to the setting of bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time selection register.

Remark f_X: System clock oscillation frequency

Data Retention Timing (STOP mode release by $\overline{\text{RESET}}$)

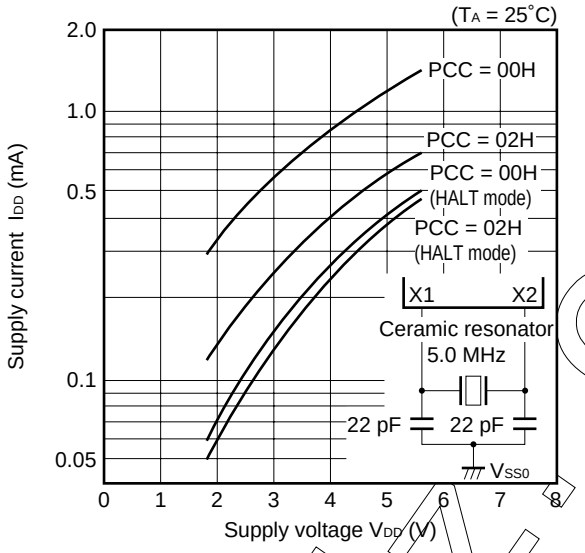


Data Retention Timing (standby release signal: STOP mode release by interrupt signal)

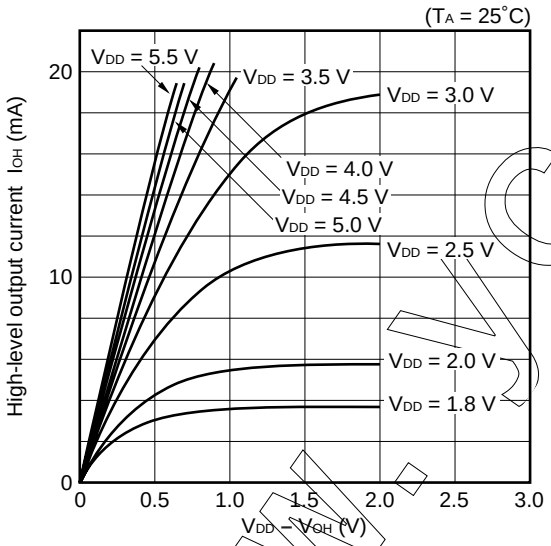


11. CHARACTERISTICS CURVES

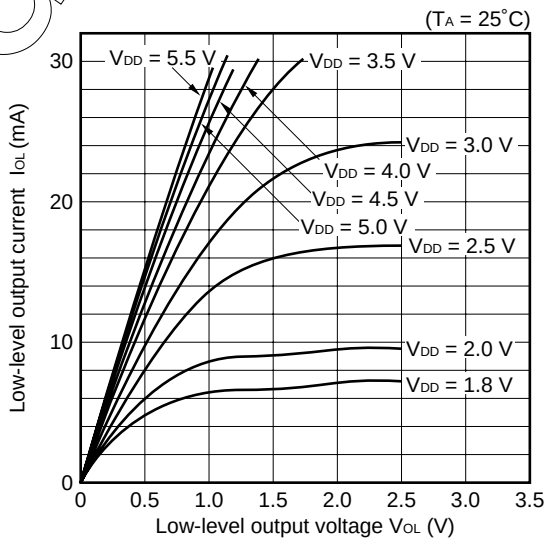
I_{DD} vs V_{DD} (system clock: 5.0 MHz, crystal resonator)



I_{OH} vs $V_{DD} - V_{OH}$

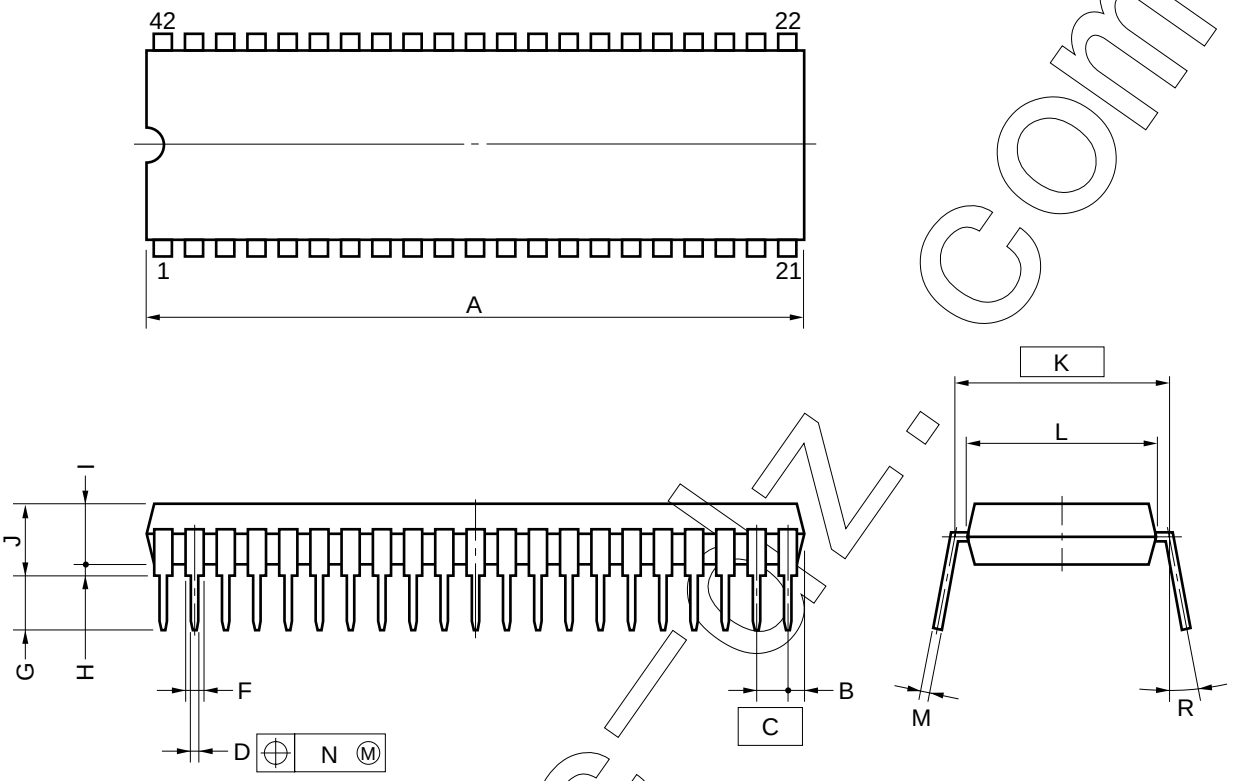


I_{OL} vs V_{OL}



12. PACKAGE DRAWINGS

42PIN PLASTIC SHRINK DIP (600 mil)



NOTES

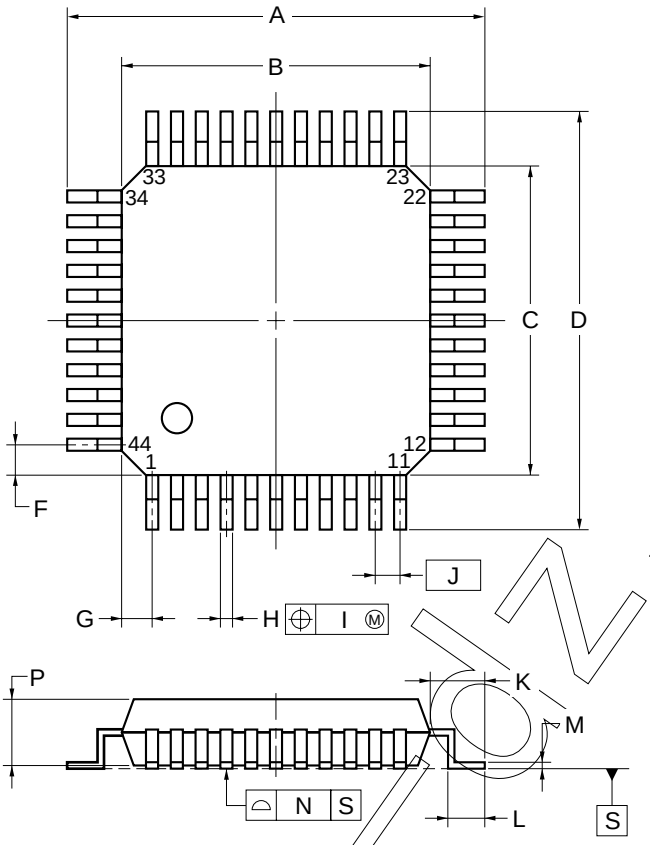
1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

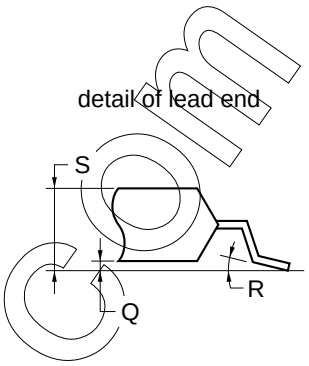
2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	39.13 MAX.	1.541 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50 ± 0.10	$0.020^{+0.004}_{-0.005}$
F	0.9 MIN.	0.035 MIN.
G	3.2 ± 0.3	0.126 ± 0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	15.24 (T.P.)	0.600 (T.P.)
L	13.2	0.520
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007
R	0~15°	0~15°

P42C-70-600A-1

44 PIN PLASTIC QFP (□10)





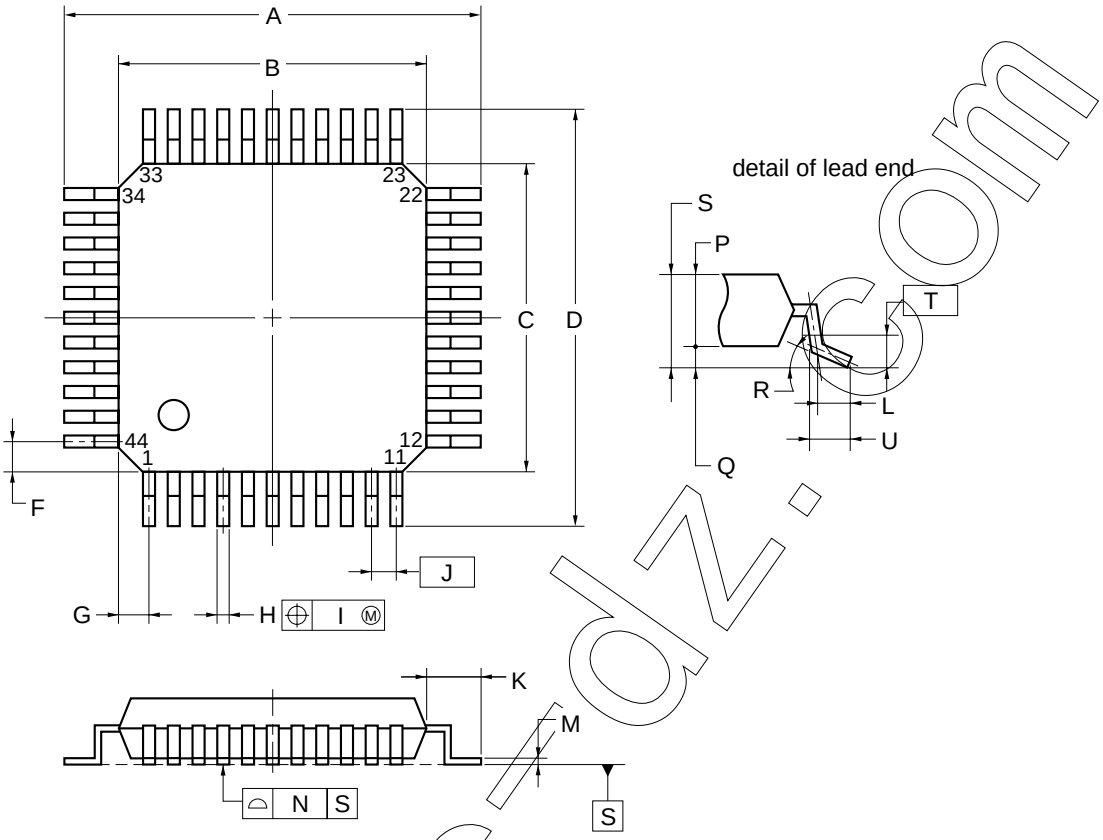
NOTE

1. Controlling dimension —— millimeter.
2. Each lead centerline is located within 0.16 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	13.2±0.2	$0.520^{+0.008}_{-0.009}$
B	10.0±0.2	$0.394^{+0.008}_{-0.009}$
C	10.0±0.2	$0.394^{+0.008}_{-0.009}$
D	13.2±0.2	$0.520^{+0.008}_{-0.009}$
F	1.0	0.039
G	1.0	0.039
H	$0.37^{+0.08}_{-0.07}$	$0.015^{+0.003}_{-0.004}$
I	0.16	0.007
J	0.8 (T.P.)	0.031 (T.P.)
K	1.6±0.2	0.063±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.17^{+0.06}_{-0.05}$	$0.007^{+0.002}_{-0.003}$
N	0.10	0.004
P	2.7±0.1	$0.106^{+0.005}_{-0.004}$
Q	0.125±0.075	0.005±0.003
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	3.0 MAX.	0.119 MAX.

S44GB-80-3BS-1

⋆ 44 PIN PLASTIC QFP (10x10)



NOTE

Each lead centerline is located within 0.16 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	12.0±0.2
B	10.0±0.2
C	10.0±0.2
D	12.0±0.2
F	1.0
G	1.0
H	$0.37^{+0.08}_{-0.07}$
I	0.2
J	0.8 (T.P.)
K	1.0±0.2
L	0.5
M	$0.17^{+0.03}_{-0.06}$
N	0.10
P	1.4±0.05
Q	0.1±0.05
R	$3^{\circ}{}^{+4^{\circ}}_{-3^{\circ}}$
S	1.6 MAX.
U	0.6±0.15

S44GB-80-8ES-1

13. RECOMMENDED SOLDERING CONDITIONS

The μPD789022, 789024, 789025, and μPD789026 should be soldered and mounted under the following recommended conditions.

For the details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

★ **Table 13-1. Surface Mounting Type Soldering Conditions**

μPD789022GB-×××-3BS-MTX: 44-pin plastic QFP (10 × 10 mm, resin thickness 2.7 mm)
μPD789024GB-×××-3BS-MTX: 44-pin plastic QFP (10 × 10 mm, resin thickness 2.7 mm)
μPD789025GB-×××-3BS-MTX: 44-pin plastic QFP (10 × 10 mm, resin thickness 2.7 mm)
μPD789026GB-×××-3BS-MTX: 44-pin plastic QFP (10 × 10 mm, resin thickness 2.7 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 sec. Max. (at 210°C or higher), Count: three times or less	IR35-00-3
VPS	Package peak temperature: 215°C, Time: 40 sec. Max. (at 200°C or higher), Count: three times or less	VP15-00-3
Wave soldering	Solder bath temperature: 260°C Max., Time: 10 sec. Max., Count: Once, Preheating temperature: 120°C Max. (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300°C Max. Time: 3 sec. Max. (per pin row)	—

Caution Do not use different soldering method together (except for partial heating).

μPD789022GB-×××-8ES: 44-pin plastic LQFP (10 × 10 mm, resin thickness 1.4 mm)
μPD789024GB-×××-8ES: 44-pin plastic LQFP (10 × 10 mm, resin thickness 1.4 mm)
μPD789025GB-×××-8ES: 44-pin plastic LQFP (10 × 10 mm, resin thickness 1.4 mm)
μPD789026GB-×××-8ES: 44-pin plastic LQFP (10 × 10 mm, resin thickness 1.4 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 sec. Max. (at 210°C or higher), Count: two times or less	IR35-00-2
VPS	Package peak temperature: 215°C, Time: 40 sec. Max. (at 200°C or higher), Count: two times or less	VP15-00-2
Wave soldering	Solder bath temperature: 260°C Max., Time: 10 sec. Max., Count: Once, Preheating temperature: 120°C Max. (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300°C Max. Time: 3 sec. Max. (per pin row)	—

Caution Do not use different soldering method together (except for partial heating).

Table 13-2. Insertion Type Soldering Conditions

μPD789025CU-xxx: 42-pin plastic shrink DIP (600 mils)
μPD789026CU-xxx: 42-pin plastic shrink DIP (600 mils)

Soldering Method	Soldering Conditions
Wave soldering (pin only)	Solder bath temperature: 260°C Max., Time: 10 sec. Max.
Partial heating	Terminal temperature: 300°C Max., Time: 3 sec. Max. (for each pin)

Caution Apply wave soldering only to the pins and be careful not to bring solder into direct contact with the package.

APPENDIX A DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD789022, μPD789024, μPD789025, and μPD789026.

Language Processing Software

RA78K0S[Notes 1, 2, 3]	Assembler package common to 78K/0S Series
CC78K0S[Notes 1, 2, 3]	C compiler package common to 78K/0S Series
DF789026[Notes 1, 2, 3]	Device file for the μPD789026 Subseries
CC78K0S-L[Notes 1, 2, 3]	C compiler library source file common to 78K/0S Series

★ Flash Memory Writing Tools

Flashpro lll (FL-PR3[Note 4], PG-FP3)	Dedicated flash programmer for microcontrollers incorporating flash memory
FA-42CU[Note 4]	Flash memory writing adapter for 42-pin plastic shrink DIP (CU type)
FA-44GB[Note 4]	Flash memory writing adapter for 44-pin plastic QFP (GB-3BS type)
FA-44GB-8ES[Note 4]	Flash memory writing adapter for 44-pin plastic LQFP (GB-8ES type)

★ Debugging Tools

IE-78K0S-NS In-circuit emulator	In-circuit emulator for debugging the hardware and software of the application system using the 78K/0S series. Supports the integrated debugger (ID78K0S-NS). Used with an AC adapter, emulation probe, and interface adapter that connects the host machine.
IE-70000-MC-PS-B AC adapter	Adapter that distributes power supply from an AC100 to 240-V outlet.
IE-70000-98-IF-C Interface adapter	Adapter when using a PC-9800 series PC (except notebook type) as the host machine of the IE-78K0S-NS (C bus supported).
IE-70000-CD-IF-A PC card interface	PC card and interface cable when using a notebook type PC as the host machine of the IE-78K0S-NS (PCMCIA socket supported).
IE-70000-PC-IF-C Interface adapter	Adapter when using an IBM PC/AT™ or compatibles as the host machine of the IE-78K0S-NS (ISA bus supported).
IE-70000-PCI-IF Interface adapter	Adapter when using a PC with PCI bus as the host machine of the IE-78K0S-NS.
IE-789026-NS-EM1 Emulation board	Board for emulating device-specific peripheral hardware. Used with an in-circuit emulator.
NP-42CU[Note 4]	Board connecting an in-circuit emulator and target system. For 42-pin plastic shrink DIP (CU type).
NP-44GB[Note 4] NP-44GB-TQ[Note 4]	Board connecting an in-circuit emulator and target system. For 44-pin plastic QFP (GB-3BS type) and 44-pin plastic LQFP (GB-8ES type).
SM78K0S[Notes 1,2]	System simulator common to 78K/0S Series
ID78K0S-NS[Notes 1,2]	Integrated debugger common to 78K/0S Series
DF789026[Notes 1,2]	Device file for μPD789026 Subseries

Real-Time OS

MX78K0S[Notes 1, 2]	OS for 78K/0S Series

Notes 1. Based on the PC-9800 series (MS-DOS™ + Windows™)

2. Based on the IBM PC/AT and compatibles (Japanese/English Windows)

3. Based on the HP9000 series 700™ (HP-UX™), SPARCstation™ (SunOS™, Solaris™), and NEWS™ (NEWS-OS™)

4. Products manufactured by Naito Densei Machida Mfg. Co., Ltd. (+81-44-822-3813).

Remark The RA78K0S, CC78K0S, and SM78K0S can be used in combination with the DF789026.

APPENDIX B RELATED DOCUMENTS

Documents Related to Devices

Document Name	Document No.	
	English	Japanese
μPD789022, 789024, 789025, 789026 Data Sheet	This manual	U11715J
μPD78F9026 Data Sheet	U11858E	U11858J
μPD789026 Subseries User's Manual	U11919E	U11919J
78K/0S Series User's Manual — Instruction	U11047E	U11047J

Documents Related to Development Tools (User's Manuals)

Document Name		Document No.	
		English	Japanese
RA78K0S Assembler Package	Operation	U11622E	U11622J
	Assembly Language	U11599E	U11599J
	Structured Assembly Language	U11623E	U11623J
CC78K/0S C Compiler	Operation	U11816E	U11816J
	Language	U11817E	U11817J
SM78K0S System Simulator Windows Based	Reference	U11489E	U11489J
SM78K Series System Simulator	External Parts User Open Interface Specifications	U10092E	U10092J
ID78K0S-NS Integrated Debugger Windows Based	Reference	U12901E	U12901J
★ IE-78K0S-NS In-Circuit Emulator		U13549E	U13549J
IE-789026-NS-EM1 Emulation Board		To be prepared	To be prepared

Documents Related to Embedded Software (User's Manual)

Document Name	Document No.	
	English	Japanese
78K/0S Series OS MX78K0S	U12938E	U12938J

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

Other Related Documents

Document Name	Document No.	
	English	Japanese
★ SEMICONDUCTOR SELECTION GUIDE Products & Packages (CD-ROM)	X13769X	
Semiconductor Device Mounting Technology Manual	C10535E	C10535J
Quality Grades on NEC Semiconductor Device	C11531E	C11531J
NEC Semiconductor Device Reliability/Quality Control System	C10983E	C10983J
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E	C11892J
Guide to Microcomputer-Related Products by Third Party	—	U11416J

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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