凌陽科技
SUNPLUS

SPCA501A
PC CAMERA CHIPSET

GENERAL DESCRIPTION

The SPCA501A provides a single chip solution to the PC camera application. It includes all the control, image processing, image compression and data transaction units needed by a PC camera. The compressed data is transferred to the PC side via the USB bus. The embedded USB controller is a hard-wired state machine. There is no need to use external microprocessors. However, an optional microprocessor may be added to control image processor for AE (auto exposure) and AWB (auto white balance). Furthermore, the SPCA501A has a built-in timing generator that supports both Sharp and Sony CCD sensor.

FEATURES

- 10 bits CCD raw data input
- Support RGB mosaic CFA(Color Filter Array) and Frame Transfer type CCD image sensor such as Sony ICX098AK, Sharp LZ24BP
- Provide window image's white balance measurement and gain parameter control
- Provide window image's exposure and sharpness measurement
- 3.3 Volt power supply
- USB Suspend mode available
- Support YUV422, YUV411, Raw Data 8 bit and Raw data 10 bit format when using 2M-bytes DRAM
- Support YUV411 and Raw Data 8 bit format when using 512K-byte DRAM
- Adjustable compression rate
- USB Vendor ID selectable via a serial EEPROM
- 100 pins QFP packages

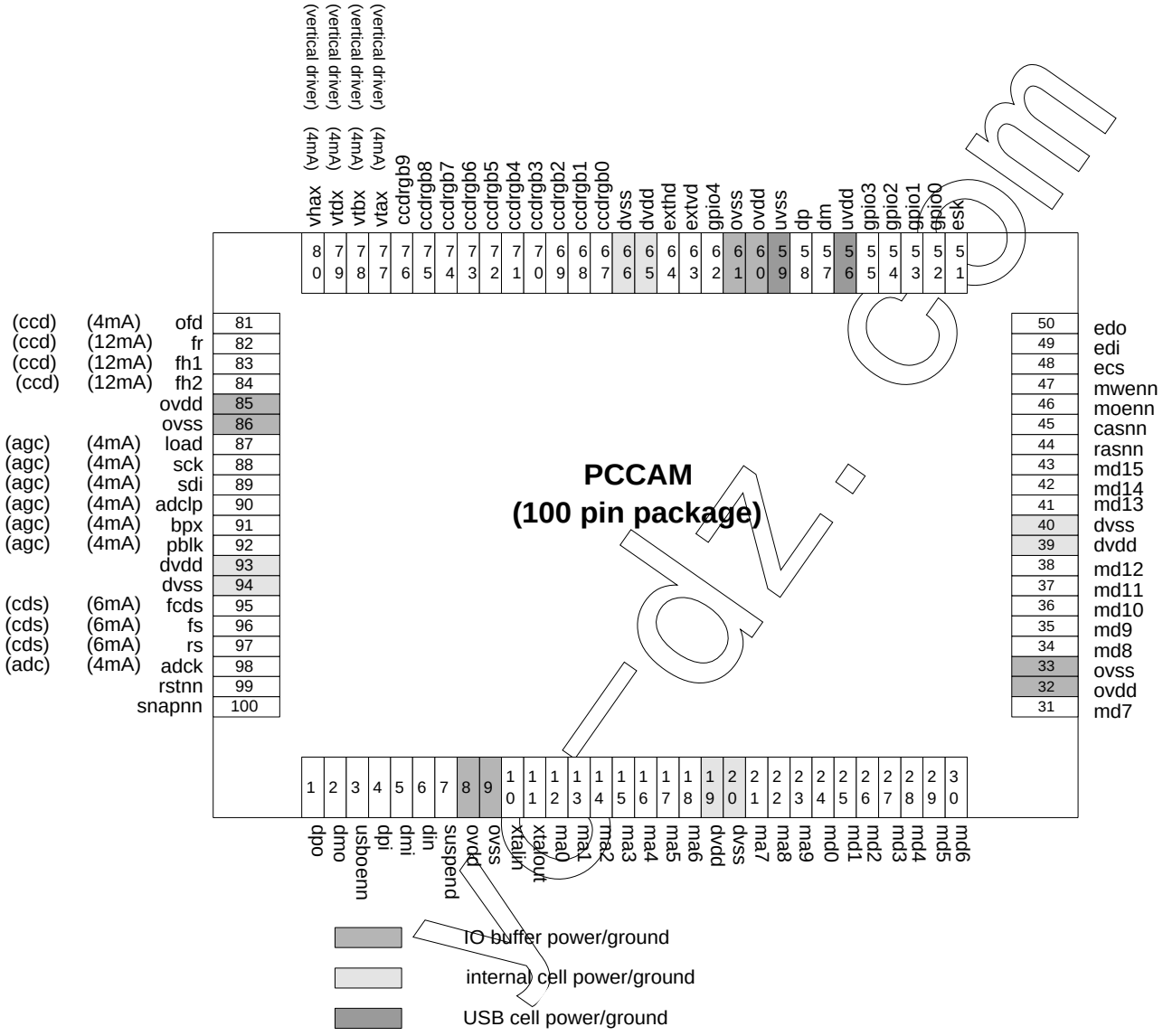
PIN DESCRIPTION

Mnemonic	PIN No.	Type	Description	Memo
dpo	1	O	USB data output to external transceiver	
dmo	2	O	USB data output to external transceiver	
usboenn	3	O	USB data output enable	active low
dpi	4	I	USB data single ended data input from external USB transceiver	pull-up inside the chip
dmi	5	I	USB data single ended data input from external USB transceiver	pull-down inside the chip
din	6	I	USB differential data input from external USB transceiver	pull-down inside the chip
suspend	7	O	USB suspend signal	
ovdd	8	PWR	power for IO	
ovss	9	GND	ground for IO	
xtalin	10	I	crystal pad	
xtalout	11	O	crystal pad	
ma0	12	B	DRAM address	IO trap pins
ma1	13	O		
ma2	14	O		
ma3	15	B		IO trap pins
ma4	16	O		
ma5	17	O		
ma6	18	O		
dvdd	19	PWR	Power for internal cell	
dvss	20	GND	ground for internal cell	
ma7	21	O		
ma8	22	O		
ma9	23	O		
md0	24	B	DRAM data	
md1	25	B		
md2	26	B		
md3	27	B		
md4	28	B		
md5	29	B		
md6	30	B		
md7	31	B		

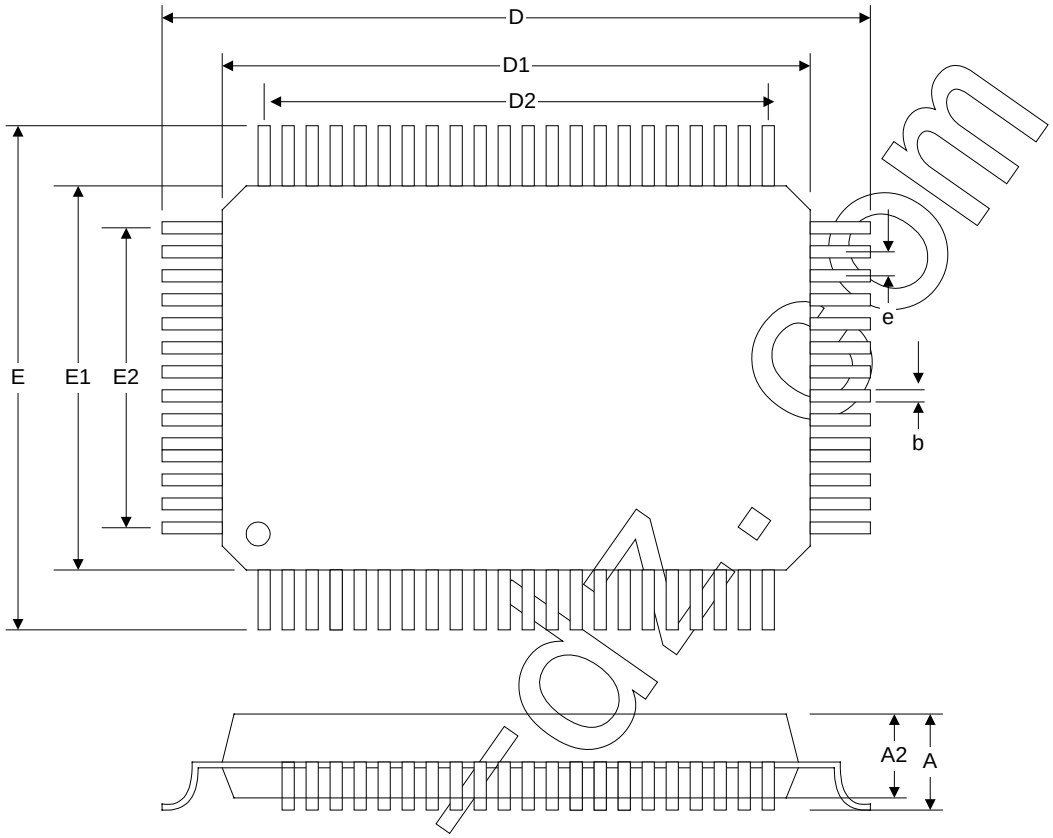
Mnemonic	PIN No.	Type	Description	Memo
ovdd	32	PWR	power for IO	
ovss	33	GND	ground for IO	
md8	34	B		
md9	35	B		
md10	36	B		
md11	37	B		
md12	38	B		
dvdd	39	PWR	power for internal cells	
dvss	40	GND	ground for internal cells	
md13	41	B		
md14	42	B		
md15	43	B		
rasnn	44	O	DRAM row address strobe	
casnn	45	O	DRAM column address strobe	
moenn	46	O	DRAM data output enable	
mwenn	47	O	DRAM data write enable	
ecs	48	O	EPROM chip select	
edi	49	B	EPROM data input	
edo	50	I	EPROM data output	pull-down inside the chip
esk	51	O	EPROM clock	
gpio0	52	O	general purpose output port	
gpio1	53	O		
gpio2	54	O		
gpio3	55	O		
uvdd	56	PWR	power for internal USB transceiver	
dm	57	B	USB data	
dp	58	B		
uvss	59	GND	ground for internal USB transceiver	
ovdd	60	PWR	power for IO	
ovss	61	GND	ground for IO	
gpio4	62	O		
extvd	63	I	external VD	pull-down inside the chip
exthd	64	I	external HD	pull-down inside the chip
dvdd	65	PWR	power for internal cells	
dvss	66	GND	ground for internal cells	

Mnemonic	PIN No.	Type	Description	Memo
ccdrgb0	67	I	CCD module raw data inputs	pull-down inside the chip
ccdrgb1	68	I		ref. to pin 67
ccdrgb2	69	I		ref. to pin 67
ccdrgb3	70	I		ref. to pin 67
ccdrgb4	71	I		ref. to pin 67
ccdrgb5	72	I		ref. to pin 67
ccdrgb6	73	I		ref. to pin 67
ccdrgb7	74	I		ref. to pin 67
ccdrgb8	75	I		ref. to pin 67
ccdrgb9	76	I		ref. to pin 67
vtax	77	O	CCD vertical shift clock	
vtbx	78	O	CCD vertical shift clock	
vtdx	79	O	CCD vertical shift clock	
vhax	80	O	CCD vertical shift clock	
ofd	81	O	CCD over flow drain	
fr	82	O	CCD reset gate	
fh1	83	O	CCD horizontal shift clock	
fh2	84	O	CCD horizontal shift clock	
ovdd	85	PWR	power for IO (pin 77 to pin 98)	
ovss	86	GND	ground for IO (pin 77 to pin 98)	
load	87	O	CDS/AGC register programming chip select	For Hitachi chip HD49322BF
sck	88	O	CDS/AGC register programming clock	
sdi	89	O	CDS/AGC register programming data	
adclp	90	O	CCD dummy output clamp pulse	
Dvdd	91	PWR	power for internal cells	
dvss	92	GND	ground for internal cells	
bpx	93	O	optical black clamp pulse	
pblk	94	O	pre-blanking pulse	
fcds	95	O	CDS S/H pulse	
fs	96	O	CDS S/H pulse	
rs	97	O	CDS S/H pulse	
adck	98	O	ADC S/H pulse	
rstnn	99	I	global reset signal to the chip	active low
snapnn	100	I	snapshot signal	active low

PIN ASSIGNMENT



PACKAGE DIMENSION



CONTROL DIMENSIONS ARE IN MILLIMETERS

Symbol	Min.	Nom.	Max.
A	-	-	3.4
A2	2.5	2.72	2.9
E	17.20	17.20	17.20
E1	14.00	14.00	14.00
E2	12.35	12.35	12.35
D	23.20	23.20	23.20
D1	20.00	20.00	20.00
D2	18.85	18.85	18.85
e	0.65	0.65	0.65
b	0.20	0.30	0.38

Unit: millimeter

NOTE: SUNPLUS TECHNOLOGY CO., LTD reserves the right to make changes at any time without notice in order to improve the design and performance and to supply the best possible product.

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