Integrating Mixed-Signal Solutions

PRELIMINARY DATA SHEET

STAC9461/63

Two and Six-Channel, 24-Bit, 192 kHz Audio DAC

PRELIMINARY INFORMATION 1/24/02

2-9461-D1-2.0-0102

STAC9461/63

Two and Six-Channel, 24-Bit, 192 kHz Audio DAC

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STAC9461/63

Two and Six-Channel, 24-Bit, 192 kHz Audio DAC

2. PRODUCT BRIEF

SigmaTel's STAC9461/63 are six and two-channel general-purpose 24-bit, audio DACs for use in consumer applications. The STAC9461/63 incorporate SigmaTel's proprietary Sigma-Delta technology to achieve DAC SNRs in excess of 100 dB. There are three audio I^2S inputs. The STAC9461/63 communicates via a standard two-wire serial interface providing simplicity in the audio system design. Packaged in a 28-pin SSOP, the STAC9461 and STAC9463 require minimal PCB space for implementation. The STAC9461 and STAC9463 DACs are pin compatible with the STAC9460 and STAC9462 audio codecs with integrated ADCs for recording.

The STAC9461 provides variable sample rate D-A converter, as well as analog processing. Supported DAC audio sample rates include 32 kHz, 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, 176.4 kHz and 192 kHz. The digital data interface communicates via a standard I^2C® compatible serial control interface and I^2S digital audio interface. All DAC's operate at 24-bit resolution with the sample rate based on the MCLK and programmable registers.

The STAC9461/63 supports I^2S digital audio inputs. These digital I/O options provide for a number of advanced architectural implementations, with volume controls and mute capabilities built directly into the codec for each individual channel. The output volume ranges from 0 dB to -95 dB with .75 dB steps. The STAC9461 also supports a single-line format.

The STAC9461/63 is designed primarily to support 6-channel audio. True AC-3 playback can be achieved for 6-speaker applications by taking advantage of the STAC9461 architecture and combining it with the appropriate processing. This product is ideal for home theatre, DVD, karaoke, and set-top-box applications.

2.1. FEATURES

- High performance ΣΔ technology
- Two or six DAC channels with independent volume controls
- Master Volume Control for all DACs
- 24-bit full duplex stereo DACs
- 32, 44.1, 48, 88.2, 96, 176.4 and 192 kHz DAC sample rates
- Standard I^2C® compatible and I^2S serial interfaces
- Digital de-emphasis capability
- DAC SNR >104 dB normal 1V RMS mode
- AudioUltra™ Mode SNR 107dB with +3dBV output
- 28-pin SSOP package
- Energy saving dynamic power modes
- 5V Analog with 3.3V or 5V Digital capability

2.2. Ordering Information

PART NUMBER	CHANNELS	PACKAGE	TEMPERATURE RANGE	SUPPLY RANGE
STAC9461S	6 DAC	28-pin SSOP	0 °C to +70 °C	AVdd = 5V, DVdd = 3.3V or 5V
STAC9463S	2 DAC	28-pin SSOP	0 °C to +70 °C	AVdd = 5V, DVdd = 3.3V or 5V
STEEBAC9460B (Evaluation Board): please send email request to apps@sigmatel.com				

Note: SigmaTel reserves the right to change specifications without notice.

2.3. Block Diagrams

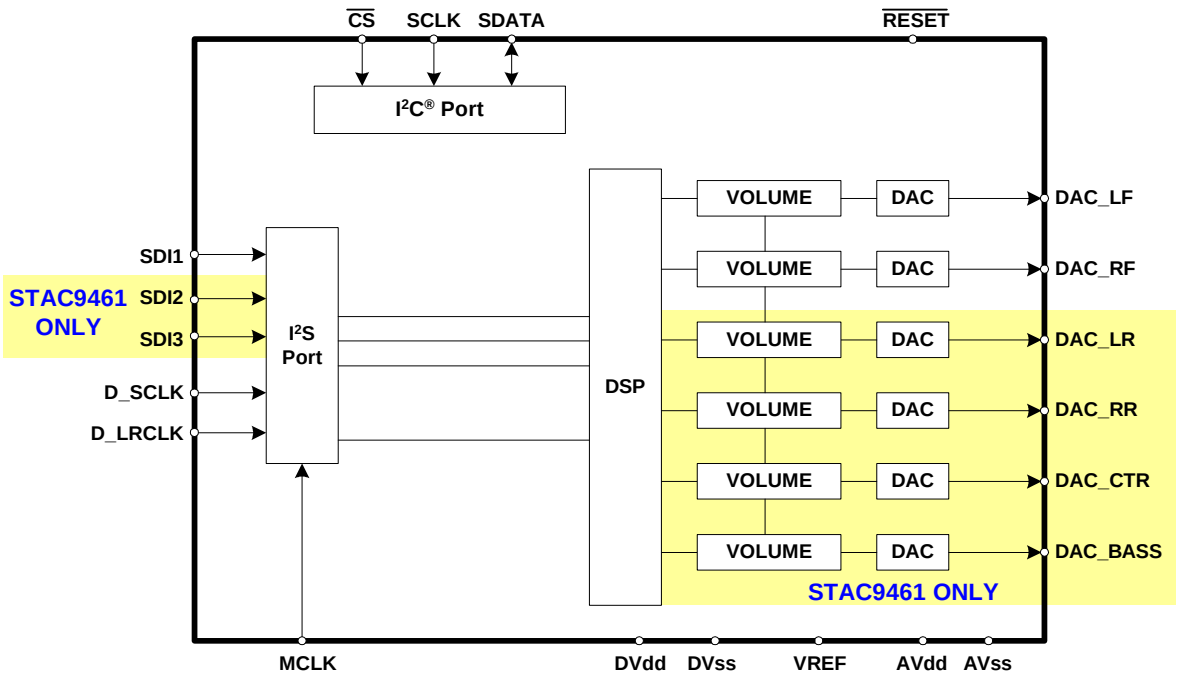


Figure 1. STAC9461 & STAC9463 Block Diagram

2.4. Related Materials

- Product Brief
- Evaluation Boards
- Reference Designs

2.5. Additional Support

Additional product and company information can be obtained by going to the SigmaTel website at: ***www.sigmatel.com***

3. CHARACTERISTICS AND SPECIFICATIONS

3.1. Absolute Maximum Ratings

Voltage on any pin relative to Ground	Vss - 0.3 V TO Vdd + 0.3 V
Operating Temperature	0 ºC TO 70 ºC
Storage Temperature	-55 ºC TO +125 ºC
Soldering Temperature	260 ºC FOR 10 SECONDS
Output Current per Pin	± 4 mA

3.2. Recommended Operating Conditions

PARAMETER		MIN	TYP	MAX	UNITS
Power Supplies	+ 3.3 V Digital	3.135	3.3	3.435	V
	+ 5 V Digital	4.75	5	5.25	V
	+ 5 V Analog	4.75	5	5.25	V
Ambient Temperature		0	-	70	ºC

3.3. Power Consumption

PARAMETER		MIN	TYP	MAX	UNITS
Digital Supply Current	+ 5 V Digital	-	50	-	mA
	+ 3.3 V Digital	-	30	-	mA
Analog Supply Current	+ 5 V Analog	-	70	-	mA

3.4. Static Digital Specifications

($T_{ambient}$ = 25 ºC, DVdd = 5.0 V or 3.3 V ± 5%, AVss=DVss=0 V; 50pF external load)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Input Voltage Range	Vin	-0.30		DVdd + 0.30	V
Low level input range	Vil	-	-	0.30xDVdd	V
High level input voltage	Vih	0.65xDVdd	-	-	V
High level output voltage	Voh	0.90xDVdd	-	-	V
Low level output voltage	Vol	-	-	0.2xDVdd	V
Input Leakage Current (Digital inputs)	-	-10	-	10	uA
Output Leakage Current (Digital outputs)	-	-10	-	10	uA
Output buffer drive current	-	-	4	-	mA

3.5. STAC9461 Analog Performance Characteristics

($T_{ambient}$ = 25 °C, AVdd = 5.0V ± 5%, DVdd = 5.0V ± 5%, AVss=DVss=0V; 1 kHz input sine wave; Sample Frequency = 48 kHz; 0 dB = 1 Vrms, 10 KΩ/50 pF load, Testbench Characterization BW: 20 Hz – 20 kHz, 0 dB settings on all gain stages)

PARAMETER	MIN	TYP	MAX	UNITS
Full Scale Input Voltage:				
Differential Inputs	-	1.0	-	Vrms
Mic Inputs	-	1.0	-	Vrms
Full Scale Output Voltage: Line Output 5V	-	1.0	-	Vrms
Analog Frequency Response (Note 1)	20	-	20,000	Hz
Digital S/N (Note 2)				
D/A 5V	-	104	-	dB
A/D 5V	-	100	-	dB
Total Harmonic Distortion: Line Output (Note 3)	-	90	-	dB
D/A Frequency Response (Note 4)	20	-	20,000	Hz
Transition Band(Note 6)	19,200	-	28,800	Hz
Stop Band(Note 6)	28,800	-	-	Hz
Deviation from Linear Phase (Note 6)	-	-	1	degree
Stop Band Rejection	-85	-	-	dB
Out-of-Band Rejection (Note 7)	-	-40	-	dB
Group Delay	-	-	1	ms
Power Supply Rejection Ratio (1kHz)	-	-40	-	dB
Spurious Tone Rejection	-	-100	-	dB
VREFout	-	0.45 x AVdd	-	V
Interchannel Gain Mismatch DAC	-	-	0.5	dB
Gain Drift	-	100	-	ppm/ºC
DAC Offset Voltage	-	10	50	mV
External Load Impedance	10	-	-	KΩ
Mute Attenuation (Vrms input)	90	96	-	dB

Note:
1. ± 1 dB limits. If the sample rate is greater than or equal to 96 kHz the max frequency response becomes 40 kHz.
2. The ratio of the rms output level with 1 kHz full scale input to the rms output level with all zeros into the digital input. Measured “A weighted” over a 20 Hz to a 20 kHz bandwidth. (AES17-1991 Idle Channel Noise or EIAJ CP-307 Signal-to-noise Ratio).
3. 0 dB gain, 20 kHz BW, 48 kHz Sample Frequency
4. ± 0.25 dB limits. The D/A freq. response becomes 40 kHz with sampling rates > 96 kHz. At ±3dB the response range is from 20-22,500Hz at 48kHz, or 20-20,000Hz @ 44.1kHz or 20-45,000Hz @ 96kHz.
5. Transition band is 40-60% of sample rate. Stop band begins at 60% of sample rate.
6. Digital De-Emphasis OFF.
7. The integrated Out-of-Band noise generated by the DAC process, during normal PCM audio playback, over a bandwidth 28.8 to 100 kHz, with respect to a 1 Vrms DAC output.

4. STAC9461 TYPICAL CONNECTION DIAGRAM

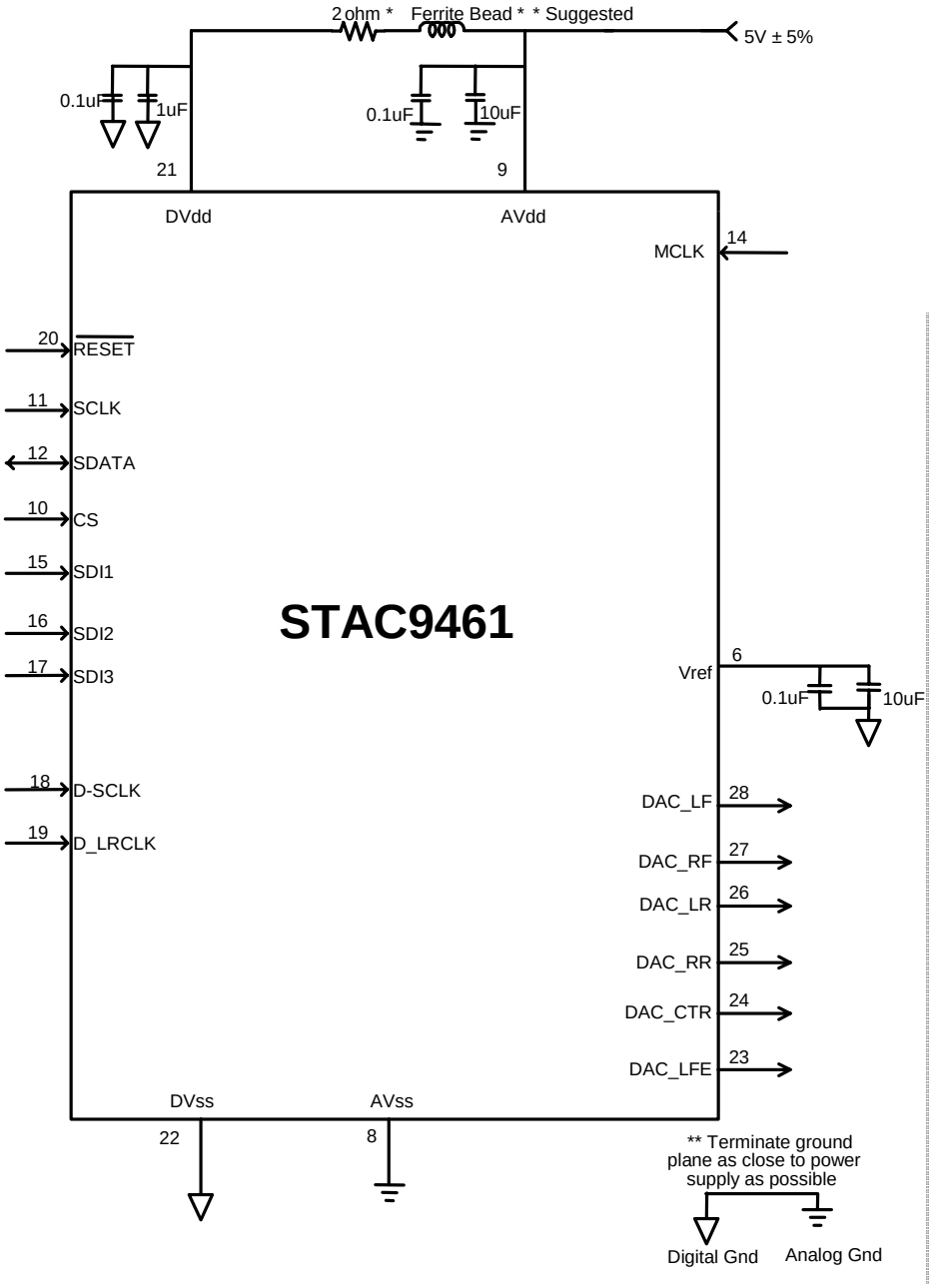


Figure 2. STAC9461 Typical Connection Diagram

Note: Pins 1,2,3,4,5,7,13 are test mode only and must be NO CONNECTS.

5. STAC9463 TYPICAL CONNECTION DIAGRAM

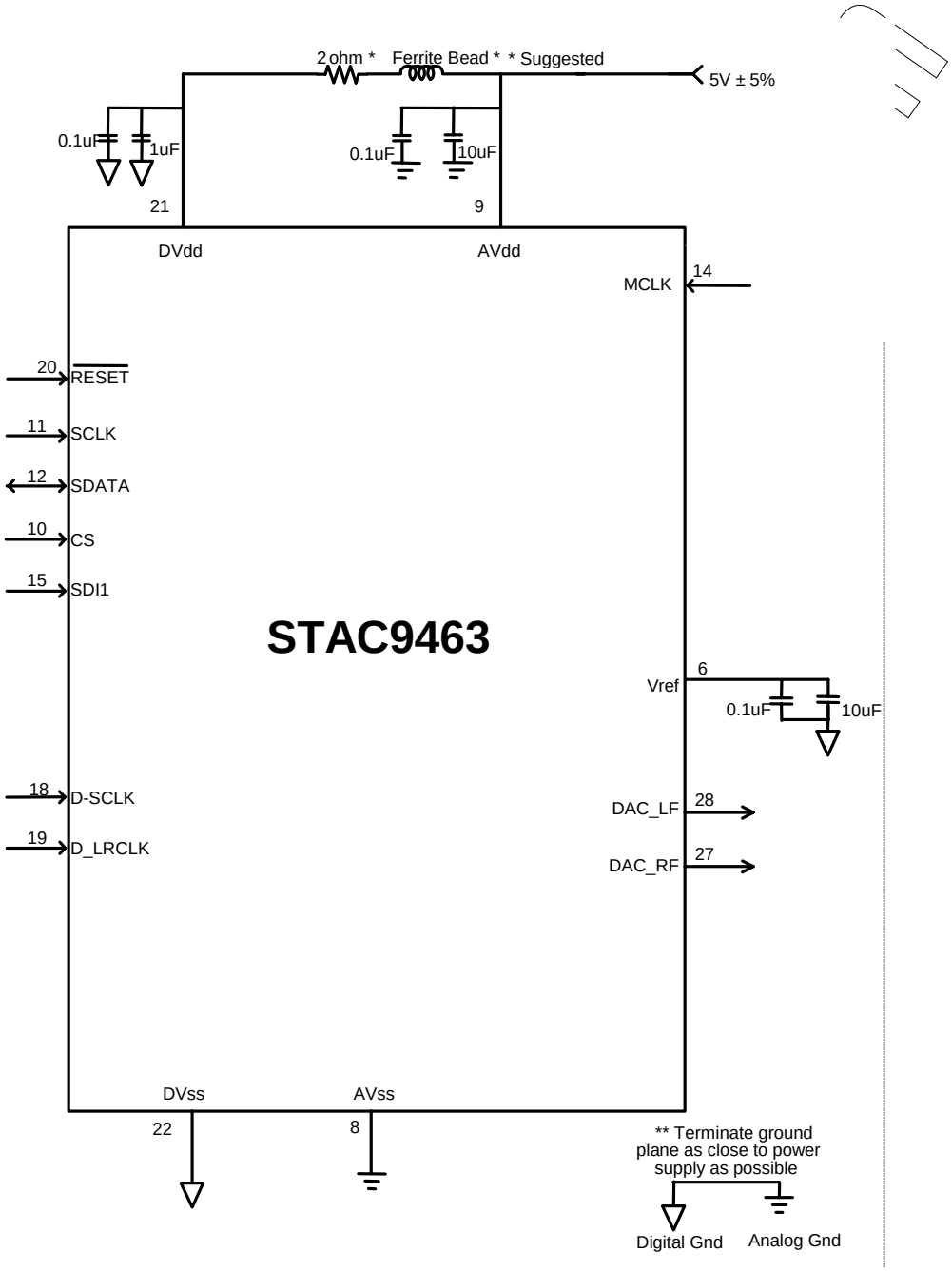


Figure 3. STAC9463 Typical Connection Diagram

Note: Pins 1-5,7,13,16,17, 23-26 are test mode only and must be NO CONNECTS.

6. SERIAL INTERFACE

Below is the figure for the serial interface between the **STAC9461/63** and a µC or µP. All register settings and chip control are performed via this serial interface, except for the address LSB.

Note: This functions as a standard 2-wire I²C compatible interface, however, the CS (chip select) line offers address flexibility and must be either hard wired to ground or tied to Vdd if no other chips are connected to the bus. Refer to Table 8.1.1 on page 15 for additional information.

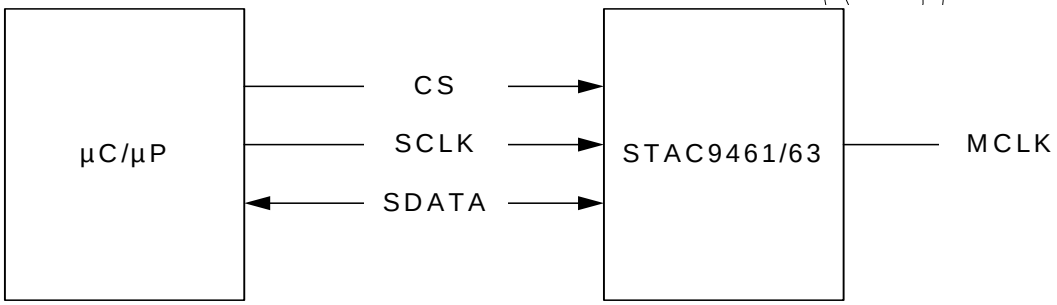


Figure 4. Serial interface to microcontroller or microprocessor

6.1. Clocking

The STAC9461/63 derives its clock from an externally connected clock through the MCLK pin in combination with the Master Clocking Register, which is further explained in section .

6.2. Reset

There are two types of resets as detailed below:

- A hard reset is achieved by driving the reset line low
- A soft reset is achieved by writing to the Reset/Status register (00h)

By writing to the Reset/Status Register (00h) a reset for the Address Control Register will occur. Writing any value to this register performs a register reset, which causes all registers to revert to their default values. This soft reset will also place the I²C state machine in a "stop" condition, and will not continue to auto-increment through the address space. Additional information about the Address Control Register can be found in section 8.1.12.

7. DIGITAL AUDIO INTERFACE

7.1. I²S Serial Interface

The **STAC9461/63** communicates digital audio information through an I²S digital serial interface. The I²S interface can be configured with the standard I²S format, left justified, right justified or one line format. Input signals SDI1, SDI2, and SDI3 interface to the Left and Right Front Channels, Left and Right Rear Channels and the Center and LFE Channels respectively.

I2S LINE	ANALOG CHANNEL	FUNCTION
SDI1	Left & Right Front	I²S data interface to DAC_LF & DAC_RF
SDI2 (9461 only)	Left & Right Rear	I²S data interface to DAC_LR & DAC_RR
SDI3 (9461 only)	Center & LFE	I²S data interface to DAC_CTR & DAC_LFE
Alternate SDI1	All Channels	One line mode for all six channels on STAC9461 One line mode for both channels on STAC9463

Table 1. Digital Audio Interface Configuration

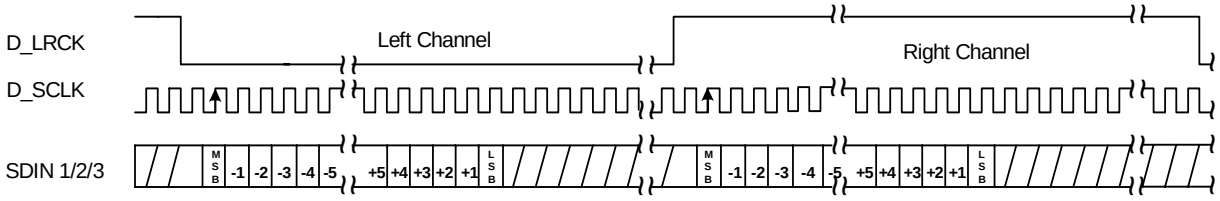


Figure 5. STAC9461/63 I²S Format [1.]

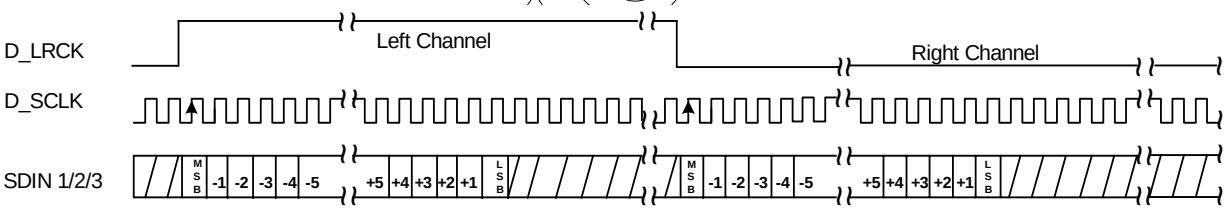


Figure 6. STAC9461/63 I²S Left Justified Format [1.]

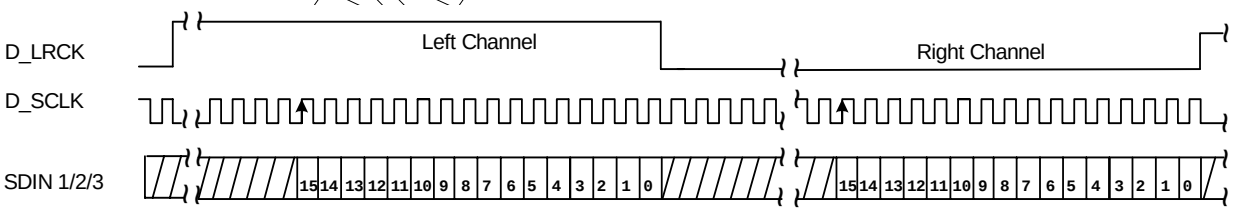


Figure 7. STAC9461/63 I²S Right Justified 16 Bit Format [1.]

Note 1: The STAC9463 uses only SD1 for I²S input.

7.2. Single Line Format

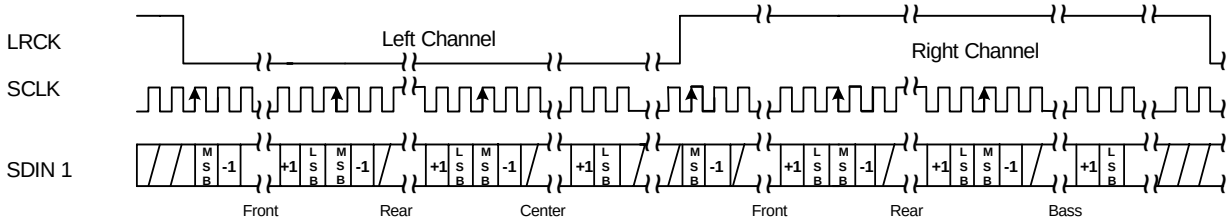


Figure 8. STAC9461 Single Line 20 Bit Data Mode Timing Diagram

Bits/Sample	SCLK Rate	Notes
20	128 Fs	6 inputs, 2 outputs, BRM only

Table 2. Single Line 20 Bit Data Mode, Data Valid on Rising Edge of SCLK

The Single line data mode for the STAC9461 allows data for all six channels to be input to the chip on a single SDATA_IN line, SD1 (Pin 15) and output to all six analog outs (Pins 23-28).

7.3. I²C-Bus Interface

The I²C-Bus of the STAC9461 operates in compliance with the I²C-Bus Interface Specification from Philips Semiconductor. The I²C-Bus for the STAC9461 does include an Auto-Increment feature not identified by the Phillips specification. For Example, a typical write would have the following format: START....Chip Address (8 bits)....Register Address(8 bits)....Data(Register Address 8 bits)....Data (Register Address +1 8 bits)....Data (Register Address +2 8 bits)....STOP. The addresses will increment through the end of the address space or until a "STOP" condition (as per I²C spec) is received by the part. For detailed information relating to the I²C, please reference the I²C-Bus Interface Specification from Philips Semiconductor. Additional information for the Address Registers can be found in section 8.1.12

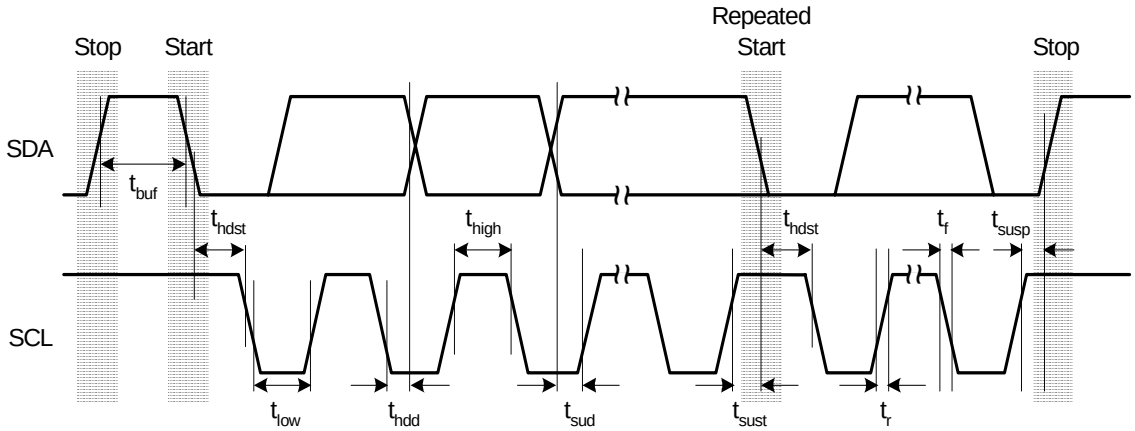


Figure 9. I²C Timing Diagram

PARAMETER	SYMBOL	MIN	MAX	UNITS
I^2C Mode (SDOUT < 47 kΩ to ground) (Note 1)				
SCL Clock Frequency	f_{scl}	-	100	KHz
Buss Free Time Between Transmissions	t_{buf}	4700	-	ns
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	4000	-	ns
Clock Low Time	t_{low}	4700	-	ns
Clock High Time	t_{high}	4000	-	ns
Setup Time for Repeated Start	t_{sust}	4700	-	ns
SDA Hold Time from SCL Falling (Note 2)	t_{hdd}	300	-	ns
SDA Setup Time to SCL Rising	t_{sud}	250	-	ns
Rise Time of Both SDA and SCL Lines	t_r	-	1000	ns
Fall Time of Both SDA and SCL Lines	t_f	-	300	ns
Setup Time for Stop Condition	t_{susp}	100	4700	ns

Note: 1. I^2C is a registered trademark of Philips Semiconductor and requires a license for use.
2. Data must be held for sufficient time to bridge the 300 ns transition time of SCL

Table 3. I^2C Mode Specifications

8. PROGRAMMABILITY

REG #	NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
00h	Reset/Status	RESERVED					REF	RESERVED		00h
01h	Status	RESERVED		LFE	CTR	RR	LR	RF	LF	00h
02h	Master Volume	MMute	MV6	MV5	MV4	MV3	MV2	MV 1	MV0	80h
03h	LF Volume	Mute LF	LF6	LF5	LF4	LF3	LF2	LF1	LF0	80h
04h	RF Volume	Mute RF	RF6	RF5	RF4	RF3	RF2	RF1	RF0	80h
05h	LR Volume	Mute LR	LR6	LR5	LR4	LR3	LR2	LR1	LR0	80h
06h	RR Volume	Mute RR	RR6	RR5	RR4	RR3	RR2	RR1	RR0	80h
07h	Center Volume	Mute C	C6	C5	C4	C3	C2	C1	C0	80h
08h	LFE Volume	Mute LFE	B6	B5	B4	B3	B2	B1	B0	80h
09h	RESERVED									
0Ah	RESERVED									
0Bh	RESERVED									
0Ch	De-Emphasis	DEM1	DEM0	DEM LFE	DEM CTR	DEMRR	DEMLR	DEMRF	DEMLF	00h
0Dh	RESERVED									
0Eh	Audio Port Control	MSS	RESERVED		ADF4	ADF3	ADF2	ADF1	ADF0	00h
0Fh	Master Clocking	RESERVED			MCM2	MCM1	MCM0	SRM1	SRM0	10h
10h	Powerdown Ctrl	RESERVED					VREF	DIG	RSVD	00h
11h	Powerdown Ctrl	RESERVED		PLFE	PCTR	PRR	PLR	PRF	PLF	00h
12h	Revision Code	0	0	0	0	0	0	0	0	00h
13h	Address Control Register	0	0	0	0	0	0	0	0	00h
14h	Address Register	0	1	0	1	0	1	CS	R/W	56h

Table 4. Programming Registers

1. All registers not shown are reserved.
2. Any bits marked “Reserved” should be written zero for normal operation

8.1. List of Registers

8.1.1. Reset/Status Register (00h)

Writing any value to this register performs a register reset, which causes all registers to revert to their default values. Reading this register returns the corresponding status of the chip section represented by the bits. The bits are defined below:

BIT	NAME	DESCRIPTION
D0:D1	RESERVED	
D2	REF	VREF status
D3-D7	RESERVED	

Table 5. Reset/Status Register

8.1.2. Status Register (01h)

Reading this (read only) register returns the corresponding status of the chip section represented by the bits. The bits are defined below:

BIT	NAME	DESCRIPTION
D0	LF	Left front channel
D1	RF	Right front channel
D2	LR	Left rear channel (STAC9461 only)
D3	RR	Right rear channel (STAC9461 only)
D4	CTR	Center channel (STAC9461 only)
D5	LFE	Low Frequency Effects Channel (STAC9461 only)
D6:D7	RESERVED	

Table 6. Status Register

8.1.3. Master Volume Register (02h)

This register manages the output signal volume for all channels simultaneously and adds to the individual channel volume registers. The DAC range is from 0 to –96 dB with each step equivalent to approximately 0.75 dB. The MSB, bit D7, of the register is the mute bit for all DACs. When this bit is set, the output level is -∞ dB. Bits MV6.. MV0 are used to control the master volume.

MMUTE	MV6…MV0	FUNCTION
0	000 0000	0 dB Attenuation
0	111 1111	96 dB Attenuation
1	xxx xxxx	∞ dB Attenuation

Table 7. Master Volume Register

8.1.4. LF/RF, LR/RR, Center/LFE Output Channel Volume Registers(03h-08h)

These registers determines the output signal volumes ranging from 0 dB to –96 dB with 0.75 dB steps. The MSB of the register is the mute bit for the channel. When this bit is set to 1, the outputlevel for that channel is -∞ dB. Please note the STAC9463 only uses registers 3 and 4 for the Left and Right Front Channels.

D7	D6…D0	FUNCTION
0	000 0000	0 dB Attenuation
0	111 1111	96 dB Attenuation
1	XXX XXXX	∞ dB Attenuation

Table 8. DAC Digital Volume Registers

8.1.5. Reserved Registers (09h-0Bh)

8.1.6. De-Emphasis Register (0Ch)

This register is used to turn de-emphasis on and off for each channel. De-emphasis control bits D5..D0 (DEMLFE .. DEMLF) select whether or not de-emphasis is turned on or off for the given DAC and bits D7-D6 (DEM1 and DEM0) determine which response curve to use.

BIT	FUNCTION
D7	De-emphasis OFF
D6	De-emphasis ON
D5	De-emphasis select for the LFE (STAC9461 only)
D4	De-emphasis select for the CENTER (STAC9461 only)
D3	De-emphasis select fot the RIGHT REAR (STAC9461 only)
D2	De-emphasis select for the LEFT REAR (STAC9461 only)
D1	De-emphasis select for the RIGHT FRONT
D0	De-emphasis select for the LEFT FRONT

Table 9. On/Off De-emphasis Selection for Each Channel

D7 .. D6	FUNCTION
00	32 kHz Response Curve
01	44.1 kHz Response Curve
10	48 kHz Response Curve
11	96 kHz Response Curve

Table 10. De-emphasis Filter Selection

8.1.7. Reserved Register (0Dh)

8.1.8. Audio Port Control (0Eh)

The I^2S port is controlled via the bits contained in this register. Formatting is controlled by the Audio Data Format bits, ADF4..ADF0 (bits D4 .. D0) of the register. The audio formats available are standard I^2S, Left Justified, Right Justified (16, 20, or 24-Bit) and One Line. Master Clocking Register (0Fh)

ADF4..ADF0, D4..D0	AUDIO DATA FORMAT
00000	I^2S
00001	Left Justified
00010	16 bit Right Justified
01010	20 bit Right Justified
10010	24 bit Right Justified
00011	One Line
*	All settings not shown are Reserved

Table 11. Audio Data Format Selection

8.1.9. The Master Clocking Register (0Fh)

The Master Clocking Register is used to set the sampling rate of the converters to one of the three sample rate modes. Base rate, mid rate and high rate are selected with bits D1-D0 of the register. The master clock mode is set by selecting bits D4,D2. The master clock mode is used generate an internal clock of the correct frequency based on the MCLK supplied by the user. For example, in the default mode (MCM=100 and SRM=00), MCLK in 512x, so if the sample rate is 48kHz then MCLK must be at 24.576MHz, which is 512x48kHz. Or with MCM=011 and SRM=01 (Mid Rate Mode) and a sample rate of 96kHz, then MCLK must be at 192x96kHz which is 18.432MHz. The Master Clocking Register should be set before unmuting any DAC channels in register 02h to 0Ah. MCM2 (D4) set is default mode.

SRM1SRM0 - D1,D0	SAMPLE RATE	FUNCTION
00 (default)	SR ≤ 48 kHz	Base Rate Mode
01	48 kHz < SR ≤ 96 kHz	Mid Rate Mode
10	96 kHz < SR ≤ 192kHz	High Rate Mode
11	Reserved	Reserved

Table 12. Sample Rate Mode

MCM2...MCM0 D4,D3,D2	MCLK Mode*		
	BRM	MRM	HRM
000	128x	64x	32x
001	Reserved	Reserved	Reserved
010	256x	128x	64x
011	384x	192x	96x
100 (default)	512x	256x	128x
101	768x	384x	192x
110	Reserved	Reserved	Reserved
111	Reserved	Reserved	Reserved

*Note: MCLK rate is relative to sample rate. (MCM * SR = MCLK). The number of D_SCLKs/D_LRCLK is independant of the MCLK mode for the STAC9461/63, but most controllers will generate D_SCLK at 1/2, 1/4, 1/8, or 1/16 the MCLK rate.

Table 13. MCLK Mode

8.1.10. Powerdown Control Registers (10h-11h)

The **STAC9461/63** is capable of operating at reduced power when no activity is required. The state of power down is controlled by the Powerdown register. There are 11 separate power down commands. The Powerdown options are listed in Table 21. The bits can be used individually or in combination with each other, and control power distribution to the DAC's. If the VREF option is selected it powers down the entire chip. Please note the rear, center, add bass DAC's should be powered down for operation with the STAC9463.

REG 11H	
BIT	**FUNCTION**
D0: PLF	DAC_LF
D1: PRF	DAC_RF
D2: PLR	DAC_LR
D3: PRR	DAC_RR
D4: PCTR	DAC_CTR
D5: PLFE	DAC_LFE
D6:	X
D7:	X

REG 10H	
BIT	**FUNCTION**
D0: DIFF	Differential
D1: DIG	Powers down I^2S and De-emphasis
D2: VREF	Voltage Reference
D3:	X
D4:	X
D5:	X
D6:	X
D7:	X

* Note: Powers down I^2S and De-emphasis
X: denotes reserved

Table 14. Powerdown Control

8.1.11. Revision Code Register (12h)

The device Revision register contains a software readable revision-specific code used to identify performance, architectural, or software differences between various device revisions.

8.1.12. Address Control Register/Address Register (13h-14h)

The address for the chip is defaulted to 55/56 or 54/55 for read and write. The LSB (bit D1) is programmable with the CS, pin 10. The Address Register (14h) can be changed. To change the address, AB must first be written to The Address Control Register (13h). A soft or hard reset will reset the Address Register to its default value with CS representing the LSB (D1).

9. PIN DESCRIPTION

9.1. Six Channel STAC9461 Pin and Signal Description

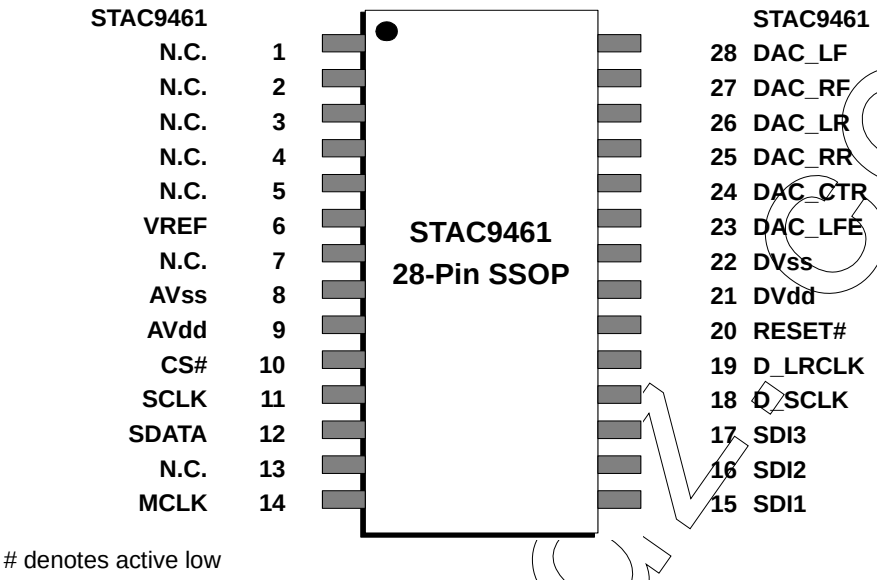


Figure 10. STAC9461 Pin Designation

Note: All N.C. pins are Internal SigmaTel Test Pins and must be left as No Connects.

9.2. Two Channel STAC9463 Pin and Signal Description

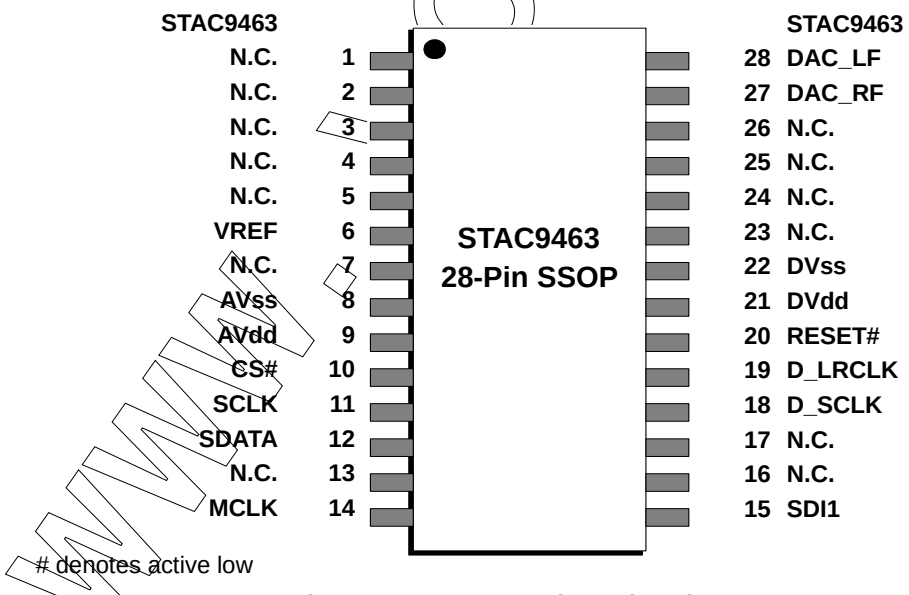


Figure 11. STAC9463 Pin Designation

Note: All N.C. pins are Internal SigmaTel Test Pins and must be left as No Connects.

Note: N.C. is No Connect.

9.3. Digital I/O

These signals connect the **STAC9461/63** to an external µC/µP, DSP, and an external crystal.

SIGNAL NAME	TYPE	DESCRIPTION
RESET #	I	Master Hardware Reset
MCLK	I	See Table 13 on page 17 for details
CS#	I	Chip select
SCLK	I	Serial data clock
SDATA	I/O	Serial data input/output
SDI1	I	I^2S digital data input for LF and RF channels
SDI2	I	I^2S digital data input for LR and RR channels (STAC9461 only, No Connect on STAC9463)
SDI3	I	I^2S digital data input for Center and LFEchannels (STAC9461 only, No Connect on STAC9463)
D_LRCLK	I	I^2S digital data left/right clock
D_SCLK	I	I^2S digital data bit clock

# denotes active low

Table 15. Digital Signal List

9.4. Analog I/O

These signals connect the **STAC9461/63** to analog sources and sinks, including microphones and seakers.

SIGNAL NAME	TYPE	DESCRIPTION
DAC_LF	O	Left front channel (LF)
DAC_RF	O	Right front channel (RF)
DAC_LR	O	Left rear channel (LR) (STAC9461 only, No Connect on STAC9463)
DAC_RR	O	Right rear channel (RR) (STAC9461 only, No Connect on STAC9463)
DAC_CTR	O	Center channel (CTR) (STAC9461 only, No Connect on STAC9463)
DAC_LFE	O	Low Frequency Effects output (LFE) (STAC9461 only, No Connect on STAC9463)

Table 16. Analog Signal List

9.5. Filter/References

SIGNAL NAME	TYPE	DESCRIPTION
VREF	O	Reference Voltage

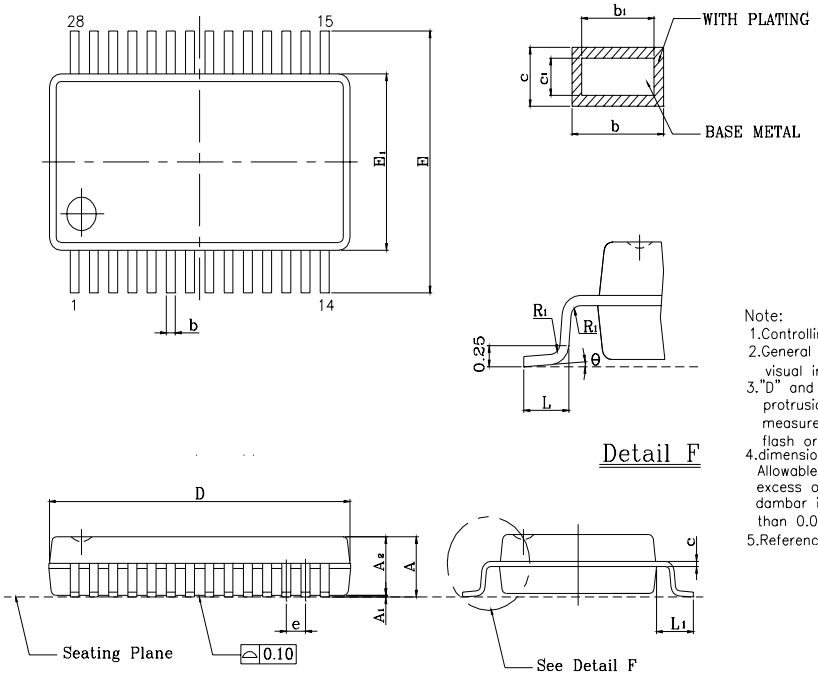
Table 17. Filtering and Voltage References

9.6. Power and Ground Signals

SIGNAL NAME	TYPE	DESCRIPTION
AVdd	I	Analog Vdd = 5.0 V
AVss	I	Analog Gnd
DVdd	I	Digital Vdd = 5.0 V or 3.3 V
DVss	I	Digital Gnd

Table 18. Power Signal List

10. PACKAGE DRAWING



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.079	—	—	2.0
A_1	0.002	—	—	0.05	—	—
A_2	0.065	0.069	0.073	1.65	1.75	1.85
b	0.009	—	0.015	0.22	—	0.38
b_1	0.009	0.012	0.013	0.22	0.30	0.33
c	0.004	—	0.010	0.09	—	0.25
c_1	0.004	0.006	0.008	0.09	0.15	0.21
D	0.390	0.402	0.413	9.90	10.20	10.50
E	0.291	0.307	0.323	7.40	7.80	8.20
E_1	0.197	0.209	0.220	5.00	5.30	5.60
e	0.0256 BSC			0.65 BSC		
L	0.021	0.030	0.037	0.55	0.75	0.95
L_1	0.050 REF			1.25 REF		
R_1	0.004	—	—	0.09	—	—
θ	0°	4°	8°	0°	4°	8°

Note:
1. Controlling dimension: mm
2. General appearance spec should be based on final visual inspection spec.
3. "D" and "E1" dimensions do not include mold flash or protrusions but do include mold mismatch and are measured at datum plane -H- mold parting line. mold flash or protrusion shall not exceed 0.20 mm per side.
4. dimension b does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13mm total in excess of b dimension at maximum material condition. dambar intrusion shall not reduce dimension b by more than 0.07 mm at least material condition.
5. Reference document : JEDEC NO. MO-150AH