I. GENERAL DESCRIPTION

The EM78P451 is an 8-bit microprocessor with low-power and high-speed CMOS technology. Its operation kernel is implemented by RISC-like architecture. The one time programmable(OTP) version is flexible no matter on mass production or engineering test. Users can get any volume with a favorable price. This device is equiped with the function of Serial Peripheral Interface (SPI) and easy-implemented RS-232. These are very suitable for the wire communication. Only 57 instructions need learn. This product is supported by EMC in-circuit emulator, macro assembler and Easy C Compiler.

II. FEATURES

- Operating voltage range: 2.2V~5.5V.
- Available in temperature range: 0°C~70°C.
- Operating frequency range:
  Crystal mode: DC~20MHz at 5V, and DC~8MHz at 3V.
  RC mode: DC~4MHz at 5V, and DC~4MHz at 3V.
- Serial Peripheral Interface (SPI) available.
- 4K x 13 bits on chip ROM (EM78P451).
- 11 special function registers.
- 140 x 8 bits general-purpose registers (SRAM).
- 5 bi-directional I/O ports (35 I/O pins).
- 3 LED direct sinking pins with internal serial resistors.
- Built-in RC oscillator.
- Built-in power-on reset.
- Five stacks for subroutine and interrupt.
- 8-bit real time clock/counter (TCC) with the overflow interrupt.
- Two machine clocks or four machine clocks per instruction cycle.
- Power-down mode.
- Programmable wake-up from sleep circuit on I/O ports.
- Programmable free running on-chip watchdog timer.
- 12 wake-up pins.
- Two open-drain pins.
- Two R-option pins.
- Package :
  (1) 40 pin DIP : EM78P451R.
  (2) 40 pin SOP : EM78P451M.
  (3) 42 pin SHRINK : EM78P451R
  (4) 44 pin QFP : EM78P451AQ.
- Reloadable counter available.
- Four types of interrupts.
  1. Pin changed (/INT).
  2. SPI completed.
  3. TCC over flow.
  4. Reloadable counter match.

III. PIN ASSIGNMENTS

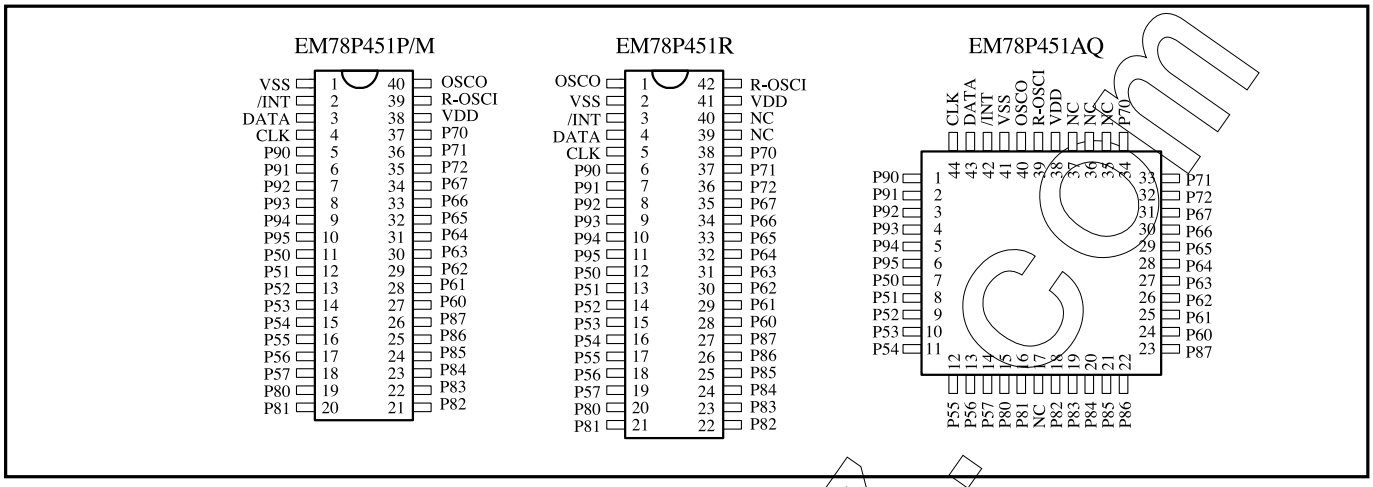


Fig. 1 Pin assignments

IV. FUNCTIONAL BLOCK DIAGRAM

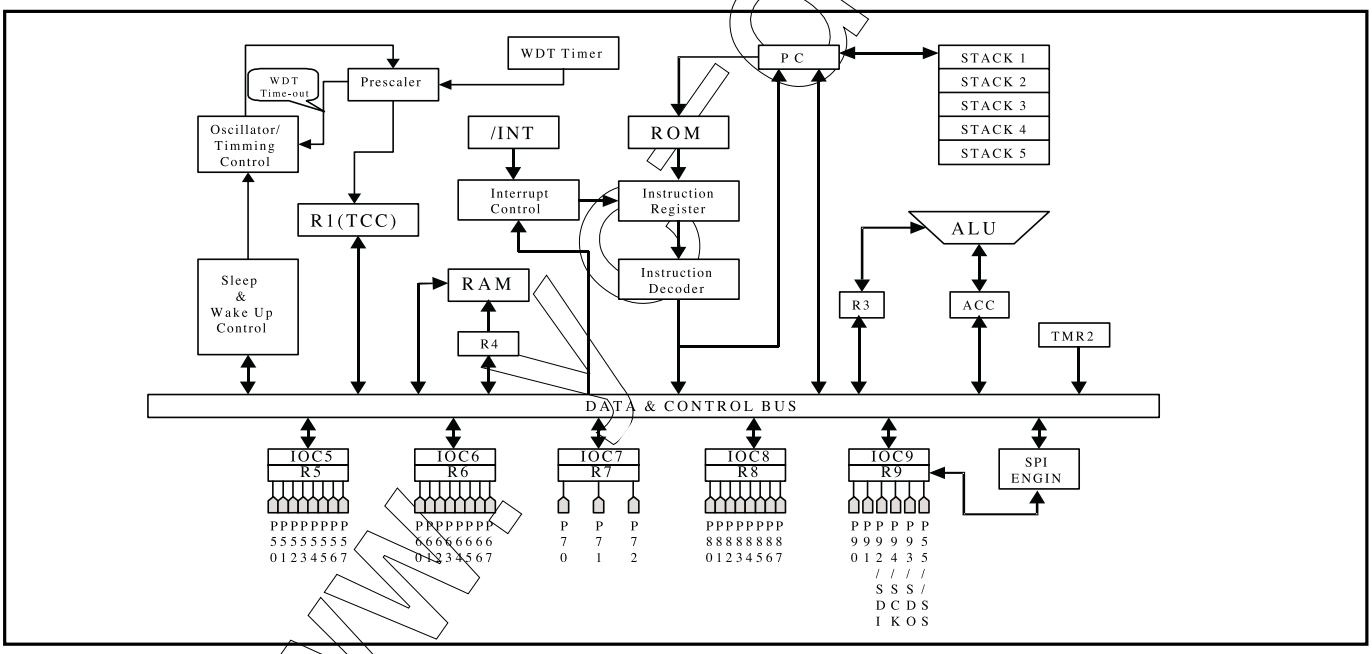


Fig. 2 Functional block diagram

V. PIN DESCRIPTION

Table 1 Pin description-EM78P451

Symbol	Type	Function Description
R-OSCI	I	In XTAL mode: Crystal input; In RC mode: 56 Kohm±5% pull-high to generate 1.8432MHz.
OSCO	O	In XTAL mode: Crystal output; In RC mode: Instruction clock output.
P90~P95	I/O	Port 9 is a 6-bit bi-directional I/O port. All of its pins can be pulled high individually in software.
P80~P87	I/O	Port 8 is an 8-bit bi-directional I/O port. P80 and P81 are also used as the R-option

Symbol	Type	Function Description
P70~P72	I/O	LED direct-driving pin with internal serial resistor as used to be output. Defined in software.
CLK	I/O	By connecting P74 and P76 together. P74 can be pulled high in software. P76 can be defined as an open-drain output.
DATA	I/O	By connecting P75 and P77 together. P75 can be pulled high by software. P77 can be defined as an open-drain output.
P60~P67	I/O	Port 6 is an 8-bit bi-directional port. All of its pins can be pulled high individually in software.
P50~P57	I/O	Port 5 is an 8-bit bi-directional I/O port. All of its pins can be pulled high individually in software.
VDD	-	Power supply pin.
VSS	-	Ground pin.
/INT	I	An interrupt schmitt-triggered pin. The function of interrupt triggers at the falling edge. Users can enable it by software. The internal pull-up resistor is around 50 Kohm.
SDI	I/O	Serial data in.
SDO	I/O	Serial data out.
SCK	I/O	Serial clock.
/SS	I/O	/Slave select.

VI. FUNCTION DESCRIPTION

VI.1 Operational Registers

1. R0 (Indirect Addressing Register)

R0 is not a physically implemented register. It is employed as an indirect addressing pointer. Any instruction using R0 as a register actually accesses the data pointed by the RAM Select Register (R4).

2. R1 (TCC)

- Increased by the instruction cycle clock.
- Written and read by any instruction as any other register.

3. R2 (Program Counter) & Stack

- R2 and the hardware stacks are 12 bits wide.
- The structure is depicted in Fig. 3.
- Generating 4096 x 13 bits on-chip OTP ROM addresses to the relative programming instruction codes. One program page is 1024 words long.
- All the bits of R2 are set "1"s as a RESET condition occurs.
- "JMP" instruction allows the direct loading of the lower 10 program counter bits. Thus, "JMP" allows jump to any location on one page.

- "CALL" instruction loads the lower 10 bits of the PC, and then PC+1 is pushed into the stack. Thus, the subroutine entry address can be any location on one page.
- "RET" ("RETL k", "RETI") instruction loads the program counter with the contents of the top of stack.
- "MOV R2, A" allows the loading of an address from the "A" register to the lower 8 bits of PC, and the ninth and tenth bits (A8~A9) of PC are cleared.
- "ADD R2, A" allows a relative address to be added to the current PC, and the ninth and tenth bits of PC are cleared.
- Any instruction which would change the contents of R2 (e.g. "ADD R2, A", "MOV R2, A", "BC R2,6", ...) (except "TBL") will cause the ninth and tenth bits (A8~A9) of PC to be cleared. Thus, the computed jump is limited to the first 256 locations of any program page.
- "TBL" allows a relative address to be added to the current PC (R2+A→R2), and contents of the ninth and tenth bits (A8~A9) of PC are not changed. Thus, the computed jump can be on the second (or third, 4th) 256 locations on one program page.
- In the case of EM78P451, the two most significant bits (A10 and A11) will be loaded with the contents of bits PS0~PS1 in the status register (R3) upon the execution of a "JMP", "CALL", or any instructions which would change the contents of R2.

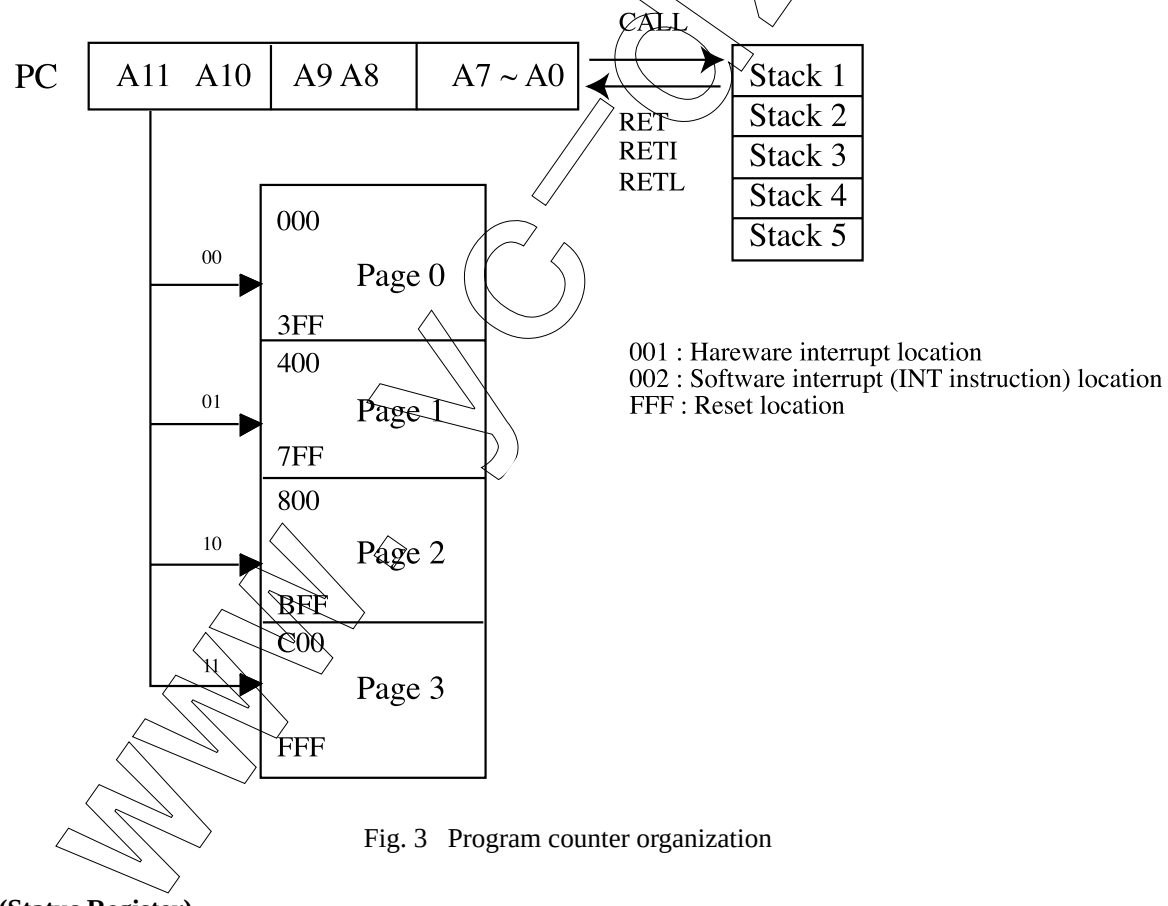


Fig. 3 Program counter organization

4. R3 (Status Register)

7	6	5	4	3	2	1	0
GP	PS1	PS0	T	P	Z	DC	C

- Bit 0 (C) Carry flag
- Bit 1 (DC) Auxiliary carry flag
- Bit 2 (Z) Zero flag. Set to "1" if the result of an arithmetic or logic operation is zero.
- Bit 3 (P) Power-down bit. Set to 1 during power on or by a "WDTC" command and reset to 0 by a "SLEP" command.
- Bit 4 (T) Time-out bit. Set to 1 by the "SLEP" command and the "WDTC" command, or during power-up and reset to 0 by WDT time-out.
- Bits 5 (PS0) ~ 6 (PS1) Page-selecting bits. PS0~PS1 are used to select a program memory page. When executing "JMP", "CALL", or other instructions which cause the program counter to be changed (e.g. MOV R2, A), PS0~PS1 are loaded to the 11th and 12th bits of the program counter which would select one of the available program memory pages. Note that RET, RETL and RETI instructions do not change the PS0~PS1 bits. That is, the return will be always to the page from the place where the subroutine was called, regardless of the current setting of PS0~PS1 bits.

PS1	PS0	Program memory page [Address]
0	0	Page 0 [000-3FF]
0	1	Page 1 [400-7FF]
1	0	Page 2 [800-BFF]
1	1	Page 3 [C00-FFF]

- Bit 7 (GP) General read/write bit.

5. R4 (RAM Select Register)

- Bits 0~5 are used to select the registers (address: 00~3F) in the indirect addressing mode.
- Bits 6~7 determine which bank is activated among the 4 banks.
- If no indirect addressing is used, the RSR can be employed as an 8-bit general-purpose read/write register.
- See the configuration of the data memory in Fig. 4.

6. R5~R8 (Port 5 ~ Port8)

- Four I/O registers
- Both P74 and P76 can read or write data from the DATA pin, and both P75 and P77 can read or write data from the CLK pin .

7. R9 (Port9)

- A 6-bit I/O register. The contents of the upper two most significant bits are read as "0".

8. RA~RF

- Refer to VI.5 Serial Peripheral Interface mode and VI.6 Timer1 .

9. R10~R3E (General-purpose Register)

- R10~R1F and R20~R3E (including Banks 0~3) are general-purpose registers.

10. R3F (Interrupt Status Register)

7	6	5	4	3	2	1	0
-	-	-	-	TM1IF	RBFIF	EXIF	TCIF

- Bit 0 (TCIF) TCC overflowing interrupt flag. Set as TCC overflows, reset by software.
- Bit 1 (EXIF) External interrupt flag. Set by falling edge on the /INT pin, reset by software.
- Bits 4~7 are not used and read as "0".
- "1" means interrupt request, "0" means non-interrupt.
- R3F can be cleared by instruction, but can not be set in software.
- IOCF is the interrupt control register.
- Note that to read R3F will get the result of "logic AND" of R3F and IOCF.

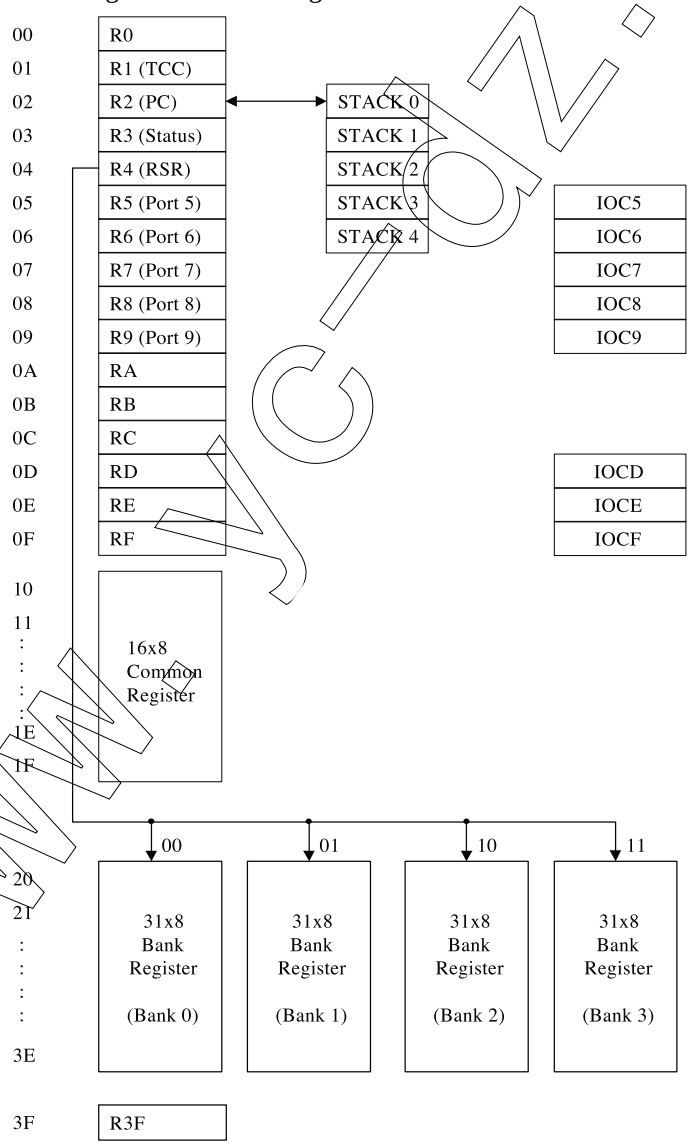


Fig. 4 Data memory configuration

VI.2 Special Purpose Registers

1. A (Accumulator)

- Internal data transfer, or instruction operand holding.
- A non-addressable register.

2. CONT (Control Register)

7	6	5	4	3	2	1	0
/PHEN	/INT	-	-	PAB	PSR2	PSR1	PSR0

- Bit 0 (PSR0) ~ Bit 2 (PSR2) TCC/WDT prescaler bits.

PSR2	PSR1	PSR0	TCC Rate	WDT Rate
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

- Bit 3 (PAB) Prescaler assignment bit.
  0: TCC
  1: WDT
- Bit 6 (/INT) An interrupt enabling flag can not be written by the CONTW instruction.
  0: interrupt masked by the DISI instruction.
  1: interrupt enabled by the ENI or RETI instruction.
- Bit 7 (/PHEN) I/O pin pull-high enable flag.
  0: For P60~P67, P74~P75 and P90~P95, the pull-high function is enabled.
  1: The pull-high function is disabled.
- Bits 4, 5 are not used, and read as "0".
- Bits 0~3 and 7 of the CONT register are readable and writable.

3. IOC5 ~ IOC9 (I/O Port Control Register)

- "1" puts the relative I/O pin into high impedance, while "0" puts the relative I/O pin as output.
- Both P74 and P76 should not be defined as output pins at the same time, and it is the same way for both P75 and P77.

- Only the lower 6 bits of the IOC9 register are used.

4. IOCD (Pull-high Control Register)

7	6	5	4	3	2	1	0
S7	-	-	-	/PU9	/PU8	/PU6	/PU5

- The default values of /PU5, /PU6, /PU8, and /PU9 are “1” which means the pull-high function is disabled.
- /PU6, /PU9 are "AND" gating with /PHEN; that is, each one written "0" will enable the pull high function.
- S7 defines the driving ability of the P70-P72.
  0: Normal output.
  1: Enhance the driving ability for LED.

5. IOCE (WDT Control Register)

7	6	5	4	3	2	1	0
-	ODE	WTE	SLPC	ROC	-	-	/WUE

- Bit 0 (/WUE) Control bit used to enable the wake-up function of P60~P67, P74~P75, and P90~P91.
  0: Enable the wake-up function.
  1: Disable the wake-up function.
  The /WUE bit can be read and written.
- Bit 3 (ROC) ROC is used for the R-option. Setting ROC to "1" will enable the status of R-option pins (P80, P81) to be read by the controller. Clearing ROC will disable the R-option function. Otherwise, the R-option function is introduced. Users must connect the P81 pin or/and P80 pin to VSS by a 560KΩ external resistor (Rex). If Rex is connected/disconnected with VDD, the status of P80 (P81) will be read as "0"/"1". Refer to Fig. 7(b). The ROC bit can be read and written.
- Bit 4 (SLPC) This bit is set by hardware at the falling edge of wake-up signal and is cleared in software. SLPC is used to control the operation of oscillator. The oscillator is disabled (oscillator is stopped, and the controller enters the SLEEP2 mode) on the high-to-low transition and is enabled (the controller is awakened from SLEEP2 mode) on the low-to-high transition. In order to ensure the stable output of the oscillator, once the oscillator is enabled again, there is a delay for approximately 18 ms (oscillator start-up timer, OST) before the next instruction of program being executed. The OST is always activated by wake-up from sleep mode whether the Code Option bit WTC is "0" or not. After waking up, the WDT is enabled if Code Option WTC is "1". The block diagram of SLEEP2 mode and wake-up caused by input triggered are depicted in Fig. 5. The SLPC bit can be read and written.
- Bit 5 (WTE) Control bit used to enable Watchdog Timer.
  The WTE bit is used only if WTC, the CODE option bit, is "1". If the WTC bit is "1", then WDT can be disabled/enabled by the WTE bit.
  0: Disable WDT.
  1: Enable WDT.
  The WTE bit is not used if WTC, the CODE option bit WTC, is "0". That is, if the WTC bit is "0", WDT is always disabled no matter what the WTE bit is.
  The WTE bit can be read and written.

- Bit 6 (ODE) Open-drain control bit.
  0: Both P76 and P77 are normally I/O pins.
  1: Both P76 and P77 pins have the open-drain function inside.
  The ODE bit can be read and written.
- Bits 1~2 and 7 Not used.

6. IOCF (Interrupt Mask Register)

7	6	5	4	3	2	1	0
-	-	-	-	T1IE	SPIIE	EXIE	TCIE

- Bit 0 (TCIE) TCIF interrupt enable bit.
  0: disable TCIF interrupt
  1: enable TCIF interrupt
- Bit 1 (EXIE) EXIF interrupt enable bit.
  0: disable EXIF interrupt
  1: enable EXIF interrupt
- Bit 2 (SPIIE) SPI interrupt enable bit.
  0: disable SPI interrupt
  1: enable SPI interrupt
- Bit 3 (T1IE) T1IE interrupt enable bit.
  0: disable T1IE interrupt
  1: enable T1IE interrupt
- Bits 4~7 Not used.
- Individual interrupt is enabled by setting its associated control bit in IOCF to "1".
- The IOCF register could be read and written.

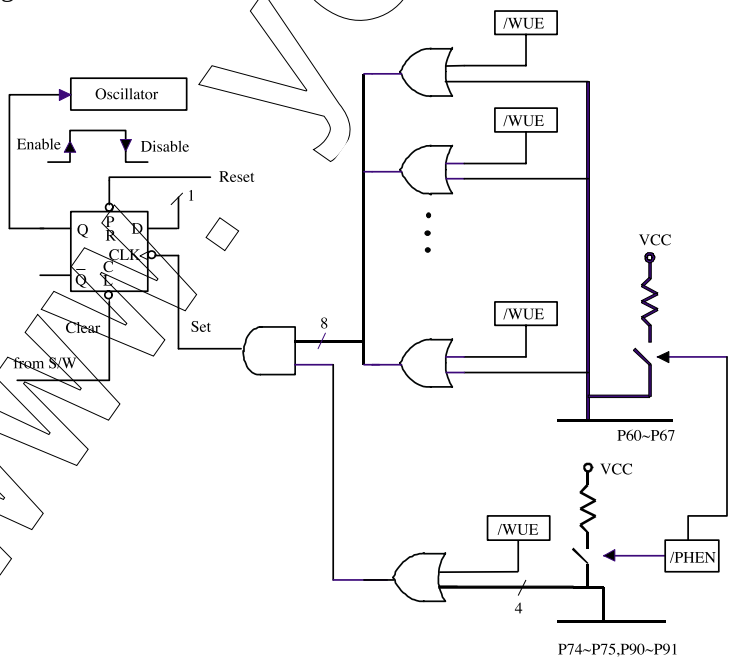


Fig. 5 Block diagram of sleep mode and wake-up circuits on I/O ports

VI.3 TCC/WDT Presacler

There is an 8-bit counter available as prescaler for the TCC or WDT. The prescaler is available only for either the TCC or the WDT at the same time and the PAB bit of the CONT register is used to determine the prescaler assignment. The PSR0~PSR2 bits determine the prescaler ratio. The prescaler will be cleared by instructions which write to TCC each time, when assigned to TCC mode. The WDT and prescaler, if assigned to the WDT mode, will be cleared by the WDTC and SLEP instructions. Fig. 6 depicts the circuit diagram of TCC/WDT.

- R1(TCC) is an 8-bit timer/counter. TCC will increase by one in every instruction cycle (without prescaler).

- The watchdog timer is a free running on-chip RC oscillator. The WDT will keep running even the oscillator driver has been turned off (i.e. in sleep mode). During the normal operation or the sleep mode, a WDT time-out (if enabled) will cause the device to reset. The WDT can be enabled or disabled at any time during the normal mode by software programming (if Code Option bit WTC is "1"). Refer to WTE bit of IOCE register. With no presacler, the WDT time-out period is approximately 18 ms.

VI.4 I/O Ports

The I/O registers, from Port 5 to Port 9, are bi-directional tri-state I/O ports. P60~P67, P74~P75, and P90~P91 have the internal pull-high and wake-up function programmable in software. P76~P77 have open-drain output by software control. P80~P81 are the R-option pins which are enabled by software. While the R-option function is used, to use P80 and P81 as output pins is recommended. During the period of R-option being enabled, P80 and P81 must be programmed as input pins. If an external resistor is connected to P80 (P81) for the R-option function, the current consumption, if necessary, should be aware of being in the power-saving applications.

The I/O ports can be defined as "input" or "output" pins by the I/O control registers (IOC5~IOC9) under program control. The I/O registers and I/O control registers are both readable and writable. The I/O interface circuit is shown in Fig. 7. Note that the reading paths are different between input and output while reading the data from the I/O port.

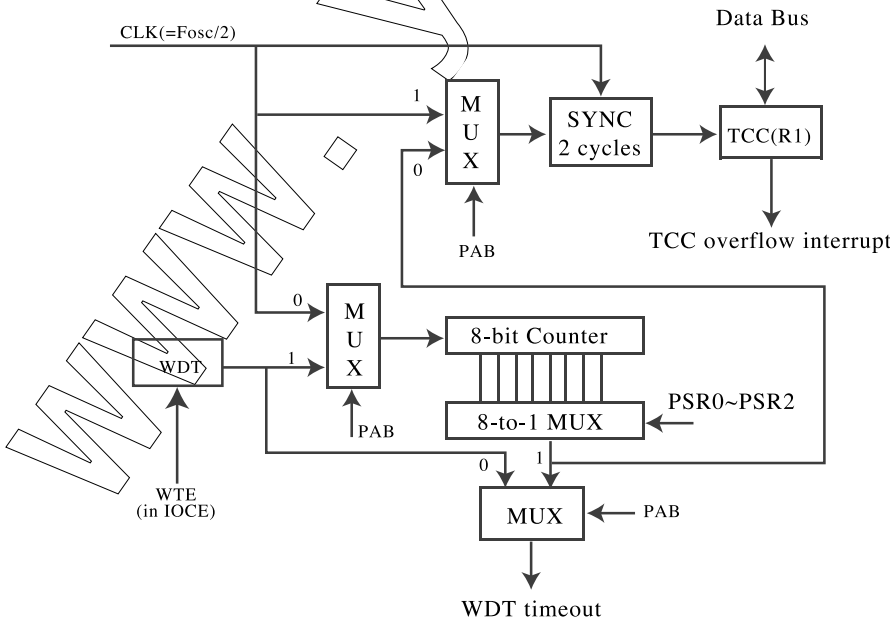


Fig. 6 Block diagram of TCC WDT

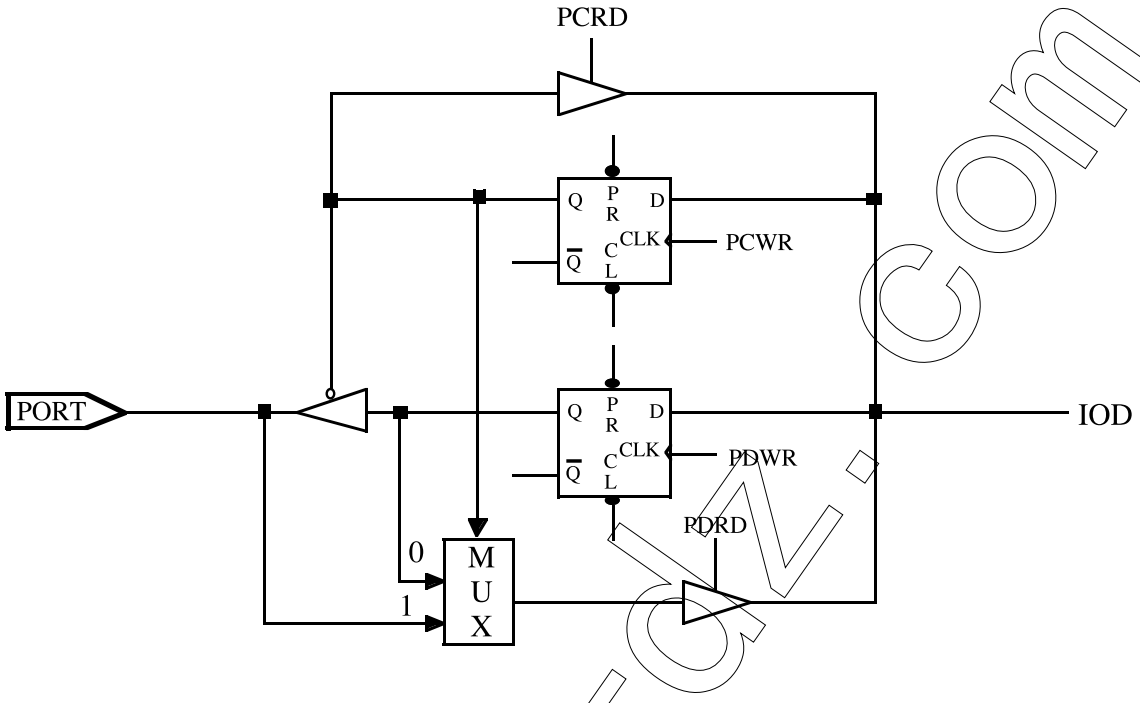


Fig. 7 The circuit of I/O port and I/O control register

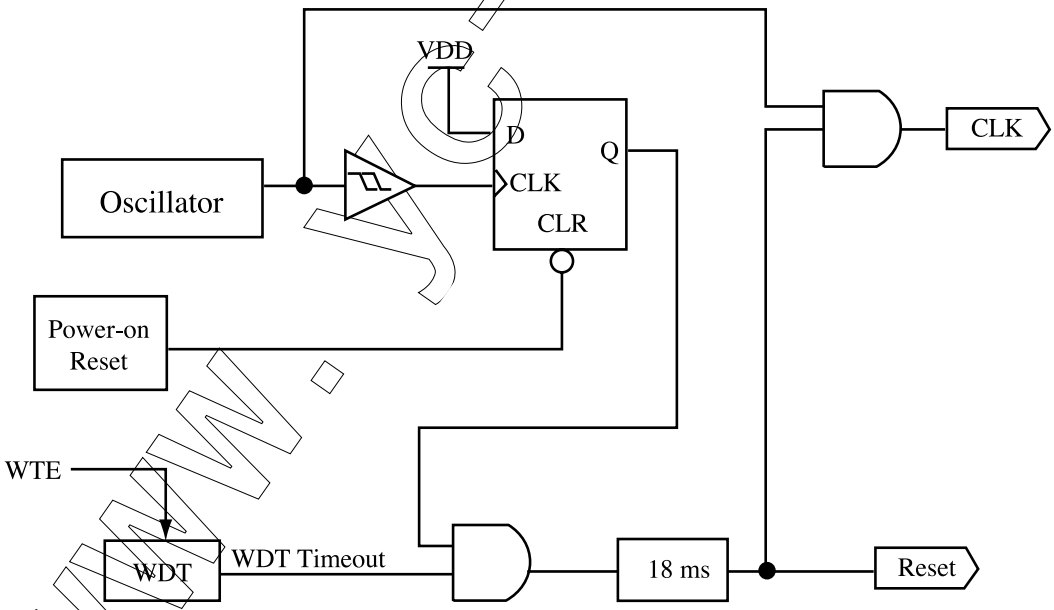


Fig. 8 Block diagram of Reset of controller

VI.5 SERIAL PERIPHERAL INTERFACE MODE

1. Overview & Features

Overview:

Fig. 9, Fig. 10, and Fig. 11 show how EM78P451 to communicate with other devices by SPI module. If EM78P451 is a master controller, it sends clock through the SCK pin. A couple of 8-bit data are transmitted and received at the same time. If EM78P451, however, is defined as a slave, its SCK pin could be programmed as an input pin. Data will continue to be shifted on a basis of both the clock rate and the selected edge.

Features:

- Operation in either Master mode or Slave mode.
- Three-wire or four-wire synchronous communication; that is, full duplex.
- Programmable baud rate of communication.
- Programming clock polarity.
- Interrupt flag available for the read buffer full.
- Up to 8 MHz (maximum) bit frequency.

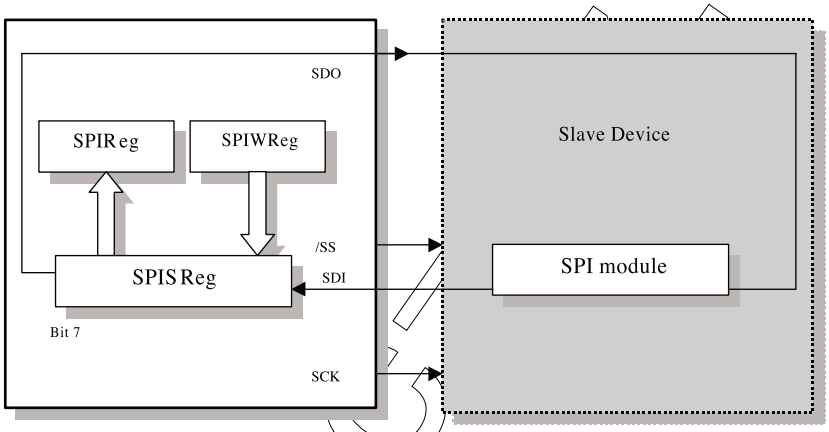


Fig. 9 Single SPI Master / Slave Communication

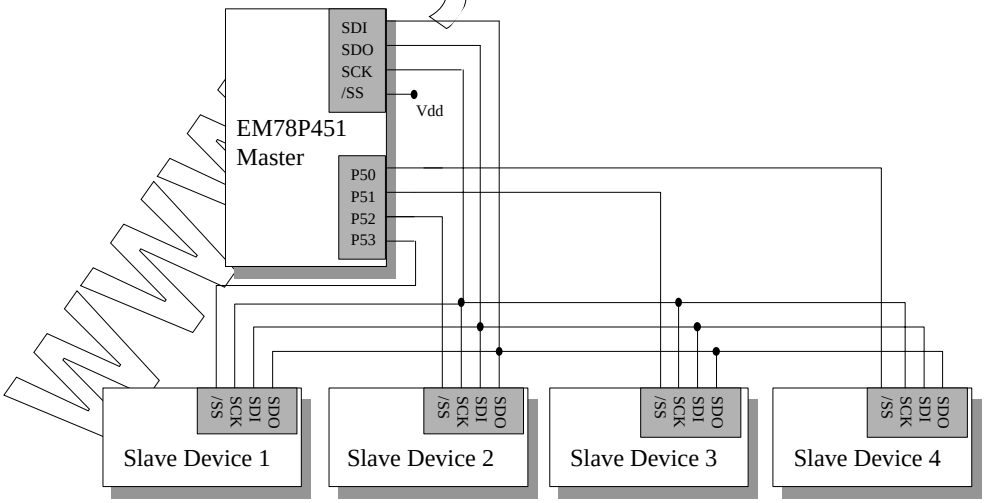


Fig. 10 The SPI configuration of Single-master and Multi-slave

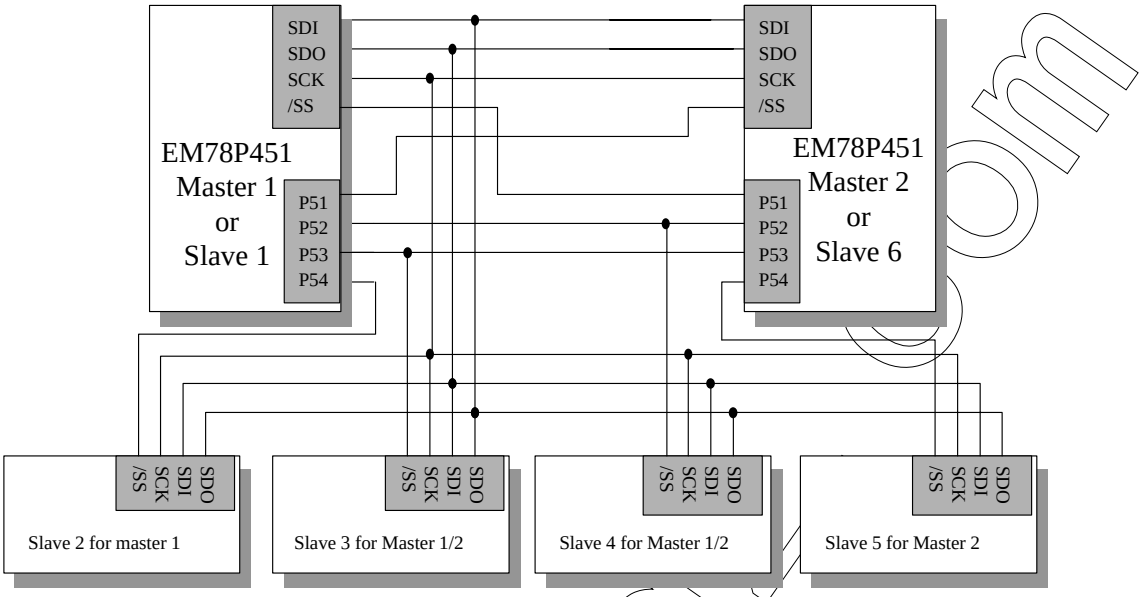


Fig. 11 The SPI configuration of Single-mater and Multi-slave

2. Function Description

The following describes the function of signal how to carry out the SPI communication:

- P93/SDO: Serial Data Out.
- P92/SDI: Serial Data In.
- P94/SCK: Serial ClocK.
- P95//SS: /Slave Select (Option). This pin (/SS) may be required during a slave mode.
- RBF: Set by Buffer Full Detector, and reset in software.
- RBFIF: Set by Buffer Full Detector, and reset in software.
- Buffer Full Detector: Setting to 1, while an 8-bit shift is complete.
- SSE: Loading the data to the SPISW register, and beginning to shift
- SPIS reg.: Shifting byte out and in. The MSB will be shifted first. Both the SPIS register and the SPIW register are loaded at the same time. Once data being written to, SPIS starts transmission / reception. The received data will be moved to the SPIR register, as the shift of the 8-bit data is complete. The RBF (Read Buffer Full) flag and the RBFI (Read Buffer Full Interrupt) flag are set.
- SPIR reg.: Read buffer. The buffer will be updated as the 8-bit shift is complete. The data must be read before the next reception is finished. The RBF flag is cleared as the SPIR register read.
- SPIW reg.: Write buffer. The buffer will deny any write until the 8-bit shift is complete. The SE bit will be kept in 1 if the communication is still under going. This flag must be cleared as the shift is finished. Users can determine if the next write attempt is available.
- SBRS2~SBRS0: Programming the clock frequency/rates and sources.
- Clock Select: Selecting either the internal clock or the external clock as the shifting clock.

- Edge Select: Selecting the appropriate clock edges by programming the ES bit.

3. Signal & Pin Description

The four pins, SDI, SDO, SCK, and /SS, which are shown in Fig. 12, will be explained in detail as follows:

SDI/P92 (Pin 7):
- Serial Data In.
- Receive data serially; Most Significant Bit (MSB) first, Least Significant Bit (LSB) last.
- Defined as high-impedance, if not selected.
- Program the same clock rate and the same clock edge to latch on both the master device and slave device,
- The received byte will update the transmitted byte.
- Both the RBF bit and the RBFI bit (located in Register 0x0D) will be set as the SPI operation is complete.
- Timing is shown in Fig. 12 and Fig. 13 .

SDO/P93 (Pin 8):
- Serial Data Out.
- Transmit data serially; Most Significant Bit (MSB) first, Least Significant Bit (LSB) last.
- Program the same clock rate and the same clock edge to latch on both the master device and slave device.
- The received byte will update the transmitted byte.
- The ES (located in Register 0x0D) bit will be reset as the SPI operation is complete.
- Timing is shown in Fig. 12 and Fig. 13 .

SCK/P94 (Pin 9):
- Serial Clock.
- Generated by a master device.
- Synchronize the data communication on both the SDI pin and the SDO pin.
- The ES (located in Register 0x0D) is used to select the edge to communicate.
- The SBRS0~SBRS2 (located in Register 0x0D) are used to determine the baud rate of communication.
- The ES, SBRS0, SBRS1, and SBRS2 bits have no effect in the slave mode.
- Timing is show in Fig. 12 and Fig. 13.

/SS/P95 (Pin 10):
- Slave Select; negative logic.
- Generated by a master device to signify the slave(s) to receive data.
- Goes low before the first cycle of SCK appears and remains low until the last (eighth) cycle is complete.
- Ignores the data on the SDI and SDO pins while /SS is high, because the SDO is no longer driven.
- Timing is shown in Fig. 12 and Fig. 13 .

4. Programming the related registers

As the SPI mode is defined, the related registers of this operation are shown in Table 2 and Table 3.

Table 2 Related control registers of the SPI mode

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0D	*SPIC/RD	ES/0	SPIE/0	SRO/0	SPISE/0	0/0	SBR2/0	SBR1/0	SBR0/0
0x0F	INTC/IOCF	0	0	0	0	T1IE/0	SPIIE/0	EXIE/0	TCIE/0

<Note>*Bit name/initial valve

Table 3 Related status/data registers of the SPI mode

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X0A	SPIRB/RA	SRB7	SRB6	SRB5	SRB4	SRB3	SRB2	SRB1	SRB0
0x0B	SPIWB/RB	SWB7	SWB6	SWB5	SWB4	SWB3	SWB2	SWB1	SWB0
0x0C	SPIS/RC	0	0	0	T1IF	OD3/0	OD4/0	RBFIF/0	RBF/0

SPIRB: SPI Read Buffer. Once the serial data is received completely, it will load to SPIRB from SPISR, and the RBF bit and the RBFIF bit in the SPIS register will be set also.

SPIWB: SPI Write Buffer. As a transmitted data is loaded, the SPIS register start to shift the data.

SPIC: SPI Control Register. Table 4 shows the initial values at power on reset.

Table 4 Initial values of the SPIC register

SPIC	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	CES	SPIE	SRO	SSE	0	SBRS2	SBRS1	SBRS0
Power-on Reset	0	0	0	0	0	0	0	0

- CES (bit 7): Clock Edge Select bit
  1 = Data shifts out on falling edge, and shifts in on rising edge. Data is held during the high level.
  0 = Data shifts out on rising edge, and shifts in on falling edge. Data is held during the low level.
- SPIE (bit 6): SPI Enable bit
  1= Enable SPI mode
  0= Disable SPI mode
- SRO (bit 5): SPI Read Overflow bit
  1 = A new data is received while the previous data is still being held in the SPIB register. In this situation, the data in SPIS register will be destroyed. To avoid setting this bit, users had better to read SPIRB register even if the transmission is implemented only.
  0 = No overflow.
  <Note>: This can only occur in slave mode.
- SSE (bit 4): SPI Shift Enable bit
  1 = Start to shift and keep on 1 while the current byte is still being transmitted.
  0 = Reset as soon as the shifting is complete, and the next byte is ready to shift.
  <Note>: This bit has to be reset in software.

Table 5 SBRS (bit 2~bit 0): SPI Baud Rate Select bits

SBRS2(Bit 2)	SBRS1(Bit 1)	SBRS0(Bit 0)	ModeBaud	Rate
0	0	0	Master	Fosc/2
0	0	1	Master	Fosc/4
0	1	0	Master	Fosc/8
0	1	1	Master	Fosc/16
1	0	0	Master	Fosc/32
1	0	1	Slave	/SS enable
1	1	0	Slave	/SS disable
1	1	1	Master	TMR1/2

<Note> In master mode, /SS is disabled.

SPIS: SPI Status register

- RBFI (bit 1): Read Buffer Full Interrupt flag
  1 = Received is finished, SPIB is full, and an interrupt occurs if enabled.
  0 = Received is not finished yet, and SPIB is empty.
- RBF (bit 0): Read Buffer Full flag
  1 = Received is finished, and SPIB is full.
  0 = Received is not finished yet, and SPIB is empty.

ODC: Open Drain Control register

- OD3 (bit 3): Open Drain Control bit(P93)
  1 = Open drain enabled for SDO.
  0 = Open drain disabled for SDO.
- OD4 (bit 2): Open Drain Control bit(P94)
  1 = Open drain enabled for SCK.
  0 = Open drain disabled for SCK.

INTC: Interrupt control register

- SPIIE (bit 2): SPI Interrupt Enable Control bit
  1 = SPI Interrupt enabled.
  0 = SPI Interrupt disabled.

5. SPI Mode Timing

The edge of SCK is selected by programming bit, CES. The waveform shown in Fig. 12 can be used no matter EM78P451 is either in a master mode or in a slave mode with /SS disabled. However, the waveform in Fig. 13 can only be implemented in a slave mode with /SS enabled.

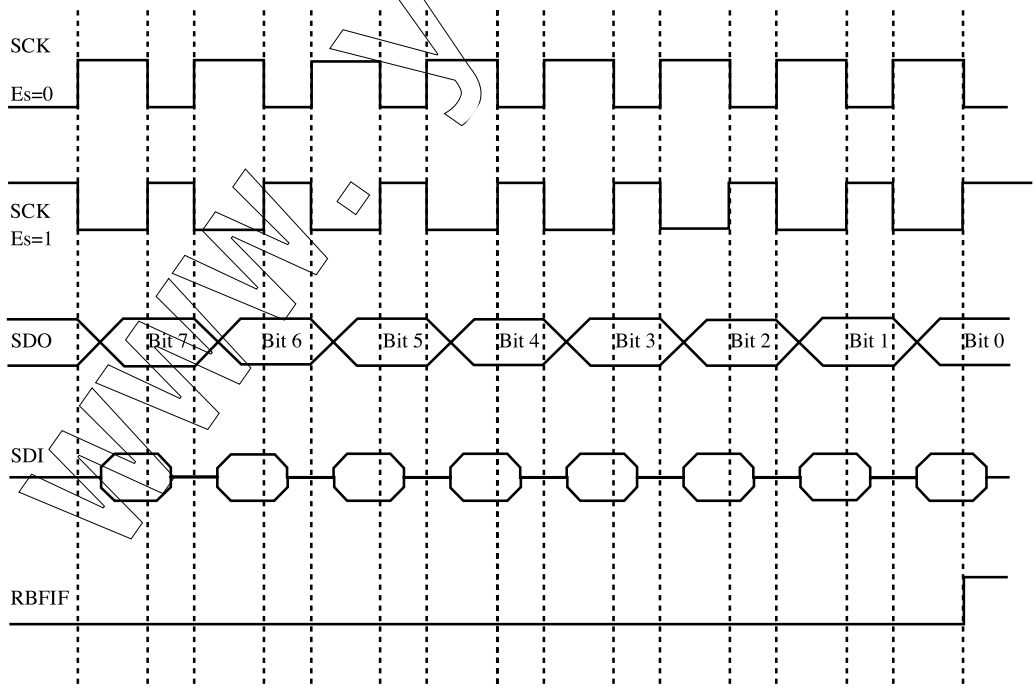


Fig. 12 SPI Mode with /SS disabled

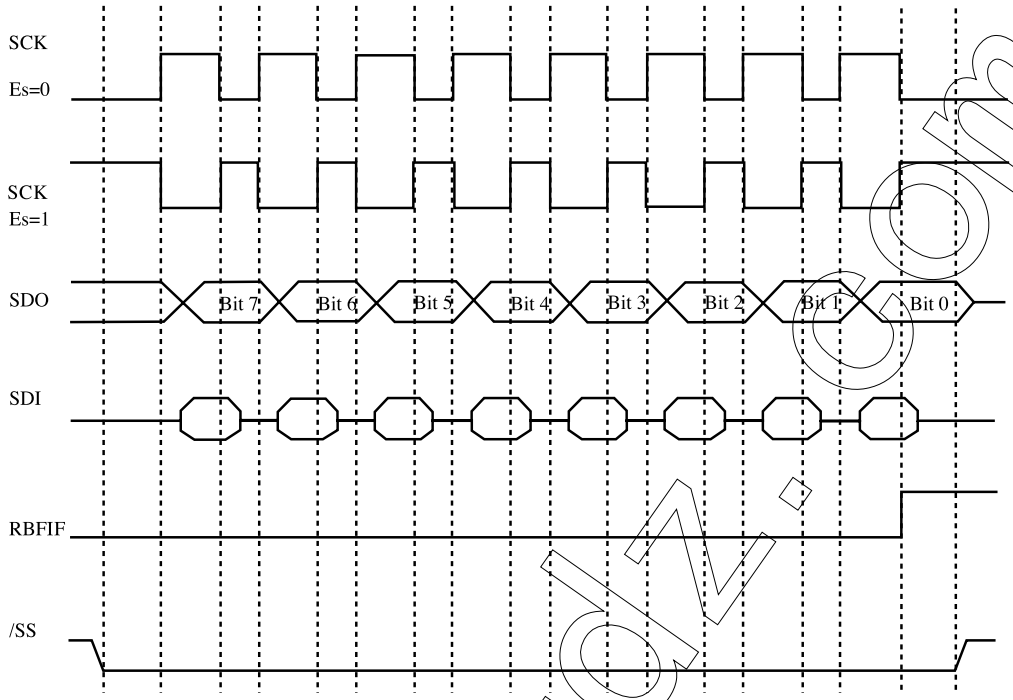


Fig. 13 SPI Mode with /SS enabled

6. Software Application of SPI

Example of SPI

```
;Define RAM
R_0     == 0        ;Indirect Addressing Register
PSW     == 3        ;Status Register
RSR     == 4        ;RAM Select Register
P9                  == 9 ;Port 9
SPIRB   == 0XA      ;SPI Read Buffer
SPIWB   == 0XB      ;SPI Write Buffer
SPIS    == 0XC      ;SPI Status Register
SPIC    == 0XD      ;SPI Contolr Register
R_3F                == 0X3F         ;Interrupt Status Register

I_A                 == 0X13         ;Saving ACC during  interrupt
I_PSW   == 0X14     ;Saving PSW during interrupt

;Define the control register
C_P9                == 0X9          ;Control Register of Port 9
C_INT   == 0XF      ;Interrupt Control Register
C_WDT               == 0XD          ;Enable Watchdog Timer<bit 4>

;Define bit
RUN     == 4        ;SPIC<bit 4>
```

```
;Define pin
C_WDT       ==0XD       ;Enable Watchdog Timer<bit 4>

SS          ==5         ;Port9<bit 5>

            ORG 0x02
INT_VECT:                           ;The initial address of interrupt subroutine
            MOV         I_A,A       ;Save Acc
            SWAP        I_A         ;No status flags effected
            SWAPA       PSW         ;Save PSW, and no status flags effected as well
            MOV         I_PSW, A    ;
            BS          P9,5        ;SPI disabled by setting //SS(port9<bit 5>) to 1

;The following three bits must be cleared in order
            BC          SPIS, 0     ;RBF=0 (SPIS<bit 0>)
            BC          SPIS, 1     ;RBFI= 0 (SPIS<bit 0>)
            BC          R_3F, 2     ;SPIIE=0 (R_3F<bit 2>)

;           (User Program)

            SWAPA       I_PSW       ;
            MOV         PSW, A      ;Recover PSW
            SWAPA       I_A         ;Recover ACC
            RETI
SPI:
            DISI        ;Disable interrrupt
            JBS         RX, BX      ;Mode select
            JMP SLAVE   ;If true, go to the MASTER mode;
                                    ;else go to the SLAVE mode
MASTER:
            MOV         A,@0bXXXXX1XX   ;Set SDI to be input, "X":users define
            IOW P9      ;
            MOV         A,@0b010001000' ;The initial value of SPIC as a master mode
            MOV         SOIC, A     ;
SLAVE:
            MOV         A, @0bXX1XX1XX; Set SDI to be input, "X":users define
            IOW P9
            MOV         A, @0b01000101; The initial value of SPIC as a Slave mode
            MOV         SPIC, A     ;

;Initiate the system configuration
            MOV         A, @0b00000111;
            CONTW
            MOV         A, @0b00000100; Enable the SPI interrupt function
            IOW C_INT   ;
            CLR R_3F                ; Clear all the interrupt flags
```

```
                BS P9, 5                        ; SPI disabled by setting /SS(port9<bit 5>) to 1
                ENI             ; Enable the interrupt function

;               (User Program)

                DISI

; In the SLAVE mode, trying to keep the RUN bit to 1 as possible.
                JBC  SPIC, RUN                  ; Check if RUN==0
                JMP START TO RUN;
                BS              SPIC, RUN       ; Set the RUN bit to 1
START TO RUN:                   ;
                ENI             ; Enable the interrupt function

;               (User Program)

;The MASTER mode is being implemented
                BC              P9, SS          ; Enable the SPI function by setting /SS to 0

;               (User Program)

                MOV             SPIWB, A        ; Load the transmitted value to SPIWB

;               (User Program)

                BS              SPIC, RUN       ; Start to execute the SPI function

;               (User Program)
                EOP             ; End of program
                ORG0XFFF        ; The initial address
                JMP SPI                         ; Go to the SPI program
```

VI.6 Timer

1. Overview

Timer1(TMR1) is an eight-bit clock counter with a programmable prescaler. It is designed for the SPI module as a baud rate clock generator. TMR1 can be read and written and cleared on any reset conditions. If employed, it can be turned down for power saving by setting TMR1EN bit [T1CON<2>] to 0.

2. Function Description

Fig. 14 shows TIMER1 block diagram. Each signal and block are described as following:

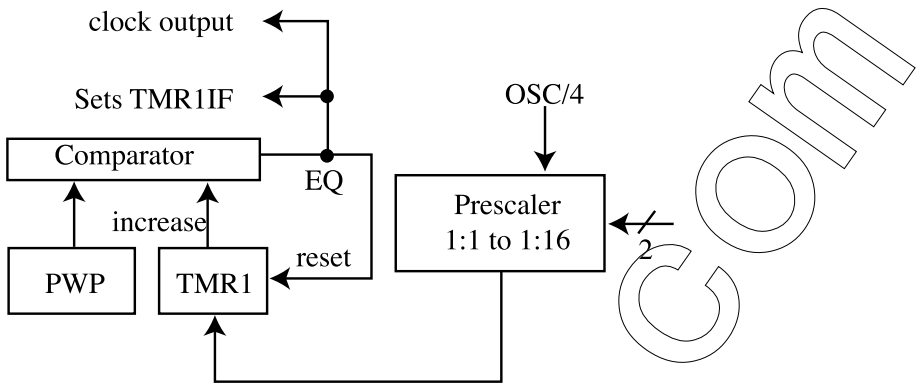


Fig. 14 TIMER1 block diagram

OSC/4: Input clock.

Prescaler: Option of 1:1, 1:4, 1:8, or 1:16 defined by T1CLK1 and T1CLK2(T1CON<1, 0>). It is cleared while a value is written to TMR1, T1CON or any kind of reset.

PWP: Pulse width preset register; the desired width of baud clock is written in advance.

TMR1: Timer 1 register; TMR1 increases until it matches with PWP, and then resets to 0. If it is chosen optionally in the SPI mode, its output is fed as a shift clock.

Comparator: To change the output status while the match occurs. The TMR1IF flag will be set at the same time.

3. Programming the related registers

As the TMR1 is defined, the related registers of this operation are shown in Table 6 and Table 7.

Table 6 Related control registers of the TMR1

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0C	SPIS/RC	0	0	0	T1IF	OD3	OD4	RBFIF	RBF
0x0F	INTC/IOCF	0	0	0	0	T1IE	SPIIE	EXIE	TCIE

Table 7 Related status/data registers of the TMR1

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X0E	TMR1/RE	TMR17	TMR16	TMR15	TMR14	TMR13	TMR12	TMR11	TMR10
0x0F	PWP/RF	PWP7	PWP6	PWP5	PWP4	PWP3	PWP2	PWP1	PWP0
0x0C	T1CON/IOCC	0	0	0	0	0	T1E	T1P1	T1P0

<Note>*Bit name/initial valve

Table 8 The rate of FOSC for timer1

TIP1	TIP0	RATE
0	0	1:1
0	1	1:4
1	0	1:8
1	1	1:16

VI.7 RESET and Wake-up

The RESET can be caused by
(1) Power-on reset, or
(2) WDT time-out. (if enabled)

The device will be kept in a RESET condition for a period of approx. 18ms (one oscillator start-up timer period) after the reset is detected. Once the RESET occurs, the following functions are performed.

- The oscillator is running, or will be started.
- The Program Counter (R2) is set to all "1".
- Upon power-on, bits 5~6 of R3 and the upper 2 bits of R4 are cleared.
- All I/O port pins are configured as input mode (high-impedance state).
- The Watchdog timer and prescaler are cleared.
- The Watchdog timer is enabled if Code Option bit WTC is "1".
- The CONT register is set to all "1" except bit 6 (INT flag).
- Bits 3,6 of IOCE register are cleared and bits 0,4~5 of IOCE register are set to "1".
- Bit 0 of R3F register and bit 0 of IOCF register are cleared.

The sleep mode (power-down mode) can be entered by executing the SLEP instruction (named as SLEEP1 MODE). While entering sleep mode, the WDT (if enabled) is cleared but keeps running. The controller can be awakened by WDT timeout (if enabled), and it will cause the controller to be reset. The T and P flags of R3 can be used to determine the source of the reset (wake-up).

In addition to the basic SLEEP1 MODE, EM78P451 has another sleep mode (caused by clearing "SLPC" bit of IOCE register, named as SLEEP2 MODE). In the SLEEP2 MODE, the controller can be awakened by

(a) input triggered, refer to Fig.15. When wake-up, the controller will continue to execute the successive address. In this case, before entering SLEEP2 MODE, the wake-up function of the trigger sources (P60~P67, P74~P75, and P90~P91)should be selected (e.g. input pin) and enabled (e.g. pull-high, wake-up control). One caution should be noted is that after waking up, the WDT is enabled if Code Option bit WTC is "1". The WDT operation (to be enabled or disabled) should be appropriately controlled by software after waking up.
(b) WDT time-out (if enabled). When wake-up, it will cause the controller to reset.

VI.8 Interrupt

The EM78P451 has the following interrupts:
(1) TCC overflow interrupt.
(2) External interrupt (/INT).
(3) Serial Peripheral Interface (SPI) completed.
(4) Reloadable counter match.

R3F is the interrupt status register, which records the interrupt request in flag bit. IOCF is the interrupt mask register. Global interrupt is enabled by ENI instruction and is disabled by DISI instruction. When one of the interrupts (when enabled) is generated, the next instruction will be fetched from address 001H. Once in the interrupt service routine the source of the interrupt can be determined by polling the flag bits in the R3F register. The interrupt flag bit must be cleared in software before leaving the interrupt service routine and enabling interrupts to avoid recursive interrupts.

The flag in the Interrupt Status Register (R3F) is set regardless of the status of its mask bit or the execution of ENI instruction. Note that reading R3F will get the output of logic AND of R3F and IOCF. Refer to Fig. 15.
The RETI instruction exits interrupt routine and enables the global interrupt (execution of ENI instruction).

When an interrupt is generated by the INT instruction (when enabled), the next instruction will be fetched from address 002H.

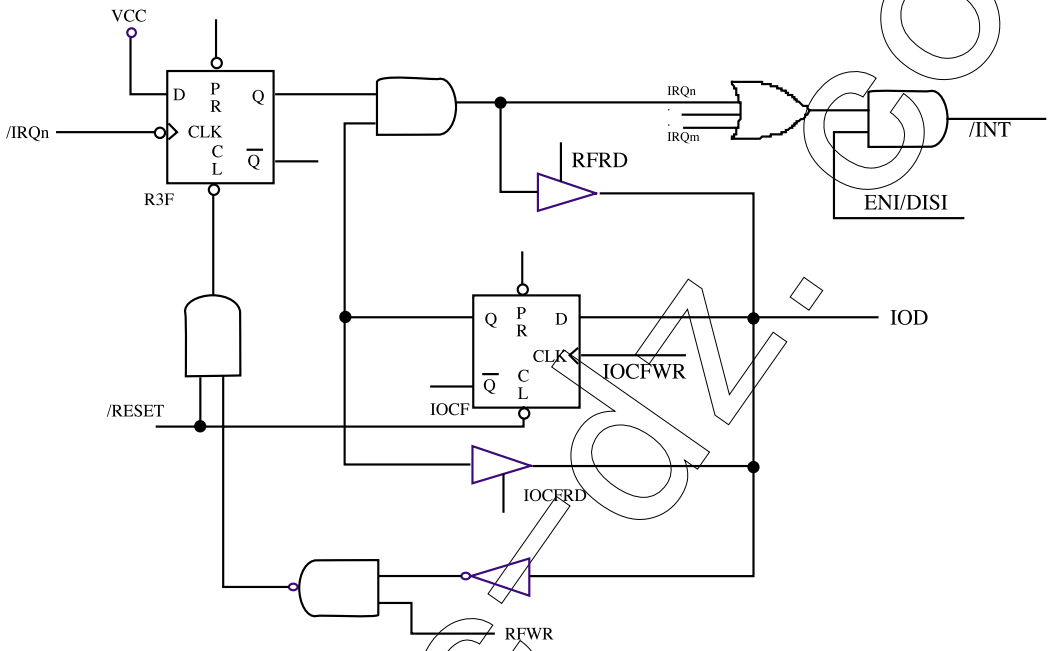


Fig. 15 Interrupt input circuit

VI.9 Instruction Set

Each instruction in the instruction set is a 13-bit word divided into an OP code and one or more operands. All instructions are executed within one single instruction cycle (consists of 2 oscillator periods), unless the program counter is changed by

(a) Executing the instruction "MOV R2,A", "ADD R2,A", "TBL", or any instruction which writes to R2 (e.g. "SUB R2,A", "BS R2,6", "CLR R2", ...).
(b) CALL, RET, RETI, RETL, JMP, Conditional skip (JBS, JBC, JZ, JZA, DJZ, DJZA) tested to be true.

In these cases, the execution takes two instruction cycles.

In addition, the instruction set has the following features:
(1) Every bit of any register can be set, cleared, or tested directly.
(2) The I/O registers can be regarded as general registers. That is, the same instruction can operate on the I/O register.

The symbol "R" represents a register designator which specifies which one of the registers (including operational registers and general-purpose registers) to be utilized by the instruction. Bits 6 and 7 in R4 determine the selected register bank. The symbol "b" represents a bit field designator which selects the number of the bit located in the register "R" affected by the operation. The symbol "k" represents an 8 or 10-bit constant or literal value.

Table 9 The list of the instruction set of EM78P451

INSTRUCTION BINARY	HEX	MNEMONIC	OPERATION	STATUS AFFECTED
0 0000 0000 0000	0000	NOP	No Operation	None
0 0000 0000 0001	0001	DAA	Decimal Adjust A	C
0 0000 0000 0010	0002	CONTW	A→CONT	None
0 0000 0000 0011	0003	SLEP	0→WDT, Stop oscillator	T,P
0 0000 0000 0100	0004	WDTC	0→WDT	T,P
0 0000 0000 rrrr	000r	IOW R	A→IOCR	None <Note1>
0 0000 0001 0000	0010	ENI	Enable Interrupt	None
0 0000 0001 0001	0011	DISI	Disable Interrupt	None
0 0000 0001 0010	0012	RET	[Top of Stack] PC	None
0 0000 0001 0011	0013	RETI	[Top of Stack] PC Enable Interrupt	None
0 0000 0001 0100	0014	CONTR	CONT→A	None
0 0000 0001 rrrr	001r	IOR R	IOCR→A	None <Note1>
0 0000 0010 0000	0020	TBL	R2+A→R2 Bits 8~9 of R2 unchanged	Z,C,DC
0 0000 01rr rrrr	00rr	MOV R,A	A→R	None
0 0000 1000 0000	0080	CLRA	0→A	Z
0 0000 11rr rrrr	00rr	CLR R	0→R	Z
0 0001 00rr rrrr	01rr	SUB A,R	R-A→A	Z,C,DC
0 0001 01rr rrrr	01rr	SUB R,A	R-A→R	Z,C,DC
0 0001 10rr rrrr	01rr	DECA R	R-1→A	Z
0 0001 11rr rrrr	01rr	DEC R	R-1→R	Z
0 0010 00rr rrrr	02rr	OR A,R	A∨VR→A	Z
0 0010 01rr rrrr	02rr	OR R,A	A∨VR→R	Z
0 0010 10rr rrrr	02rr	AND A,R	A & R→A	Z
0 0010 11rr rrrr	02rr	AND R,A	A & R→R	Z
0 0011 00rr rrrr	03rr	XOR A,R	A ⊕ R→A	Z
0 0011 01rr rrrr	03rr	XOR R,A	A ⊕ R→R	Z
0 0011 10rr rrrr	03rr	ADD A,R	A + R→A	Z,C,DC
0 0011 11rr rrrr	03rr	ADD R,A	A + R→R	Z,C,DC
0 0100 00rr rrrr	04rr	MOV A,R	R→A	Z
0 0100 01rr rrrr	04rr	MOV R,R	R→R	Z
0 0100 10rr rrrr	04rr	COMA R	/R→A	Z
0 0100 11rr rrrr	04rr	COM R	/R→R	Z
0 0101 00rr rrrr	05rr	INCA R	R+1→A	Z
0 0101 01rr rrrr	05rr	INC R	R+1→R	Z
0 0101 10rr rrrr	05rr	DJZA R	R-1→A, skip if zero	None
0 0101 11rr rrrr	05rr	DJZ R	R-1→R, skip if zero	None
0 0110 00rr rrrr	06rr	RRCA R	R(n)→A(n-1) R(0)→C, C→A(7)	C
0 0110 01rr rrrr	06rr	RRC R	R(n)→R(n-1) R(0)→C, C→R(7)	C
0 0110 10rr rrrr	06rr	RLCA R	R(n)→A(n+1) R(7)→C, C→A(0)	C
0 0110 11rr rrrr	06rr	RLC R	R(n)→R(n+1) R(7)→C, C→R(0)	C

INSTRUCTION BINARY	HEX	MNEMONIC	OPERATION	STATUS AFFECTED
0 0111 00rr rrrr	07rr	SWAPA R	R(0-3)→A(4-7) R(4-7)→A(0-3)	None
0 0111 01rr rrrr	07rr	SWAP R	R(0-3)↔R(4-7)	None
0 0111 10rr rrrr	07rr	JZA R	R+1→A, skip if zero	None
0 0111 11rr rrrr	07rr	JZ R	R+1→R, skip if zero	None
0 100b bbrr rrrr	0xxx	BC R,b	0→R(b)	None <Note2>
0 101b bbrr rrrr	0xxx	BS R,b	1→R(b)	None <Note3>
0 110b bbrr rrrr	0xxx	JBC R,b	if R(b)=0, skip	None
0 111b bbrr rrrr	0xxx	JBS R,b	if R(b)=1, skip	None
1 00kk kkkk kkkk	1kkk	CALL k	PC+1→[SP] (Page, k) →PC	None
1 01kk kkkk kkkk	1kkk	JMP k	(Page, k)→PC	None
1 1000 kkkk kkkk	18kk	MOV A,k	k→A	None
1 1001 kkkk kkkk	19kk	OR A,k	A∨ k→A	Z
1 1010 kkkk kkkk	1Akk	AND A,k	A & k→A	Z
1 1011 kkkk kkkk	1Bkk	XOR A,k	A ⊕k→A	Z
1 1100 kkkk kkkk	1Ckk	RETL k	k→A, [Top of Stack]→PC	None
1 1101 kkkk kkkk	1Dkk	SUB A,k	k-A→A	Z,C,DC
1 1110 0000 0001	1E01	INT	PC+1→[SP], 002H→PC	None
1 1111 kkkk kkkk	1Fkk	ADD A,k	k+A→A	Z,C,DC

<Note1> This instruction can operate on IOC5 ~ IOC9, IOCD~IOCF only.
<Note2> This instruction is not recommended to operate on R3F.
<Note3> This instruction cannot operate on R3F.

VII. ABSOLUTE MAXIMUM RATINGS

Items	Sym.	Condition	Rating
Temperature under bias	T_{OPR}		0°C to 70°C
Storage temperature	T_{STR}		-65°C to 150°C
Input voltage	V_{IN}		-0.3V to +6.0V
Output voltage	V_O		-0.3V to +6.0V

VIII. DC ELECTRICAL CHARACTERISTIC (Ta=0°C ~ 70°C, VDD=5V, VSS=0V)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
IIL	Input Leakage Current	VIN = VDD, VSS			±1	μA
VIH	Input High Voltage		2.0			V
VIL	Input Low Voltage				0.8	V
VIHX	Clock Input High Voltage	OSCI	3.5			V
VILX	Clock Input Low Voltage	OSCI			1.5	V
VOH1	Output High Voltage (ports 5,6,8,9 and P74~P77)	IOH = -12.0mA	2.4			V
VOH2	Output High Voltage (P70~P72)(S7=0)	IOH = -10.0mA		2		V
VOH3	Output High Voltage (P70~P72)(S7=1)	IOH = -10.0mA	2.4			V
VOL1	Output Low Voltage (port5,6,8,9 and P74~P75)	IOL =5.0mA			0.4	V

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VOL2	Output Low Voltage (P70~P72)(S7=0)	IOL =12.0mA			0.4	V
VOL3	Output Low Voltage (P70~P72)(S7=1), P76~P77)	IOL =10.0mA		3		V
IPH	Pull-high current	Pull-high active, input pin at VSS	-250	-400	-500	μA
ISB1	Power-down current	All input and I/O pin at VDD,output pin floating, WDT disable			1	μA
ISB2	Power-down current	All input and I/O pin at VDD,output pin floating, WDT enabled			10	μA
ICC1	Operating supply current (VDD=5.0V) at two cycles/two clocks	/RESET = High, Fosc=1.84324MHz(CK2="0"), output pin floating			3	mA

IX. AC ELECTRICAL CHARACTERISTIC (Ta=0°C ~ 70°C, VDD=5V, VSS=0V)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Dclk	Input CLK duty cycle		45	50	55	%
Tins	Instruction cycle time (CLK="0")	RC Type 3.679M	500		DC	ns ns
Ttcc	TCC input period		(Tins+20)/N*			ns
Twdt	Watchdog Timer period	Ta = 25°C		18		ms
Tdrh	Device reset hold period	Ta = 25°C		18		ms

Note : N* = selected prescaler ratio.

X. Application Software (SPI transceiver)

```
#This demostration program was witten in EMC++.
#EM45
;DEFINE CPU RAM
R_0         == 0                ;DEFINE BIT
TCC         == 1                #DEFINE B_KEY   R_BIT.0
PC          == 2                #DEFINE SPI_RUN SPIC.4
PSW         == 3
RSR         == 4                #DEFINE CY PSW.0
P5          == 5                #DEFINE DC PSW.1
P6          == 6                #DEFINE Z PSW.2
P7          == 7                #DEFINE D6 RSR.6
P8          == 8                #DEFINE D7 RSR.7
P9          == 9
SPIRB       == 0XA              #DEFINE P_IN P6
SPIWB       == 0XB              #DEFINE P_OUT P5
SPIS        == 0XC
```

```
SPIC            == 0XD
TMR1            == 0XE
PWP             == 0XF
R_3F            == 0X3F

R_ACC           == 0X10
R_ACC2          == 0X11
R_ACC3          == 0X12
I_A             == 0X13
I_PSW           == 0X14
I_RSR           == 0X15
I_ACC           == 0X16

R_BIT           == 0X17
R_CODE          == 0X18

C_P5            == 0X5
C_P6            == 0X6
C_P7            == 0X7
C_P8            == 0X8
C_P9            == 0X9
C_T1CON         == 0XC
C_HIGH          == 0XD
C_WDT           == 0XE
C_INT           == 0XF

P_OUT=SPIRB
P_SPI_SS=1


 SPIS.0=0
SPIS.1=0
R_3F.2=0



RSR=I_RSR
R_ACC=I_ACC
SWAPA I_PSW
PSW=A
SWAPA I_A
```

```
;DEFINE PROT
#DEFINE P_START P9.0
#DEFINE P_MS_SEL P9.1
#DEFINE P_SPI_SS P9.5

        ORG 0

        MAIN()

        ORG 1
        NOP
        I_A=A
        SWAP I_A
        SWAPA PSW
        I_PSW=A
        I_RSR=RSR
        I_ACC=R_ACC

        PSW=0
        RSR=0

        P8++


        ENDIF

        !OPTION=0B111
        !C_HIGH=0
        !C_WDT=0B00110001
        !C_INT=0B00000100



        PSW=0
        RSR=0
        R_3F=0

        RSR=0X10
        DO
        R_0=0
        D6=1
        R_0=0
```

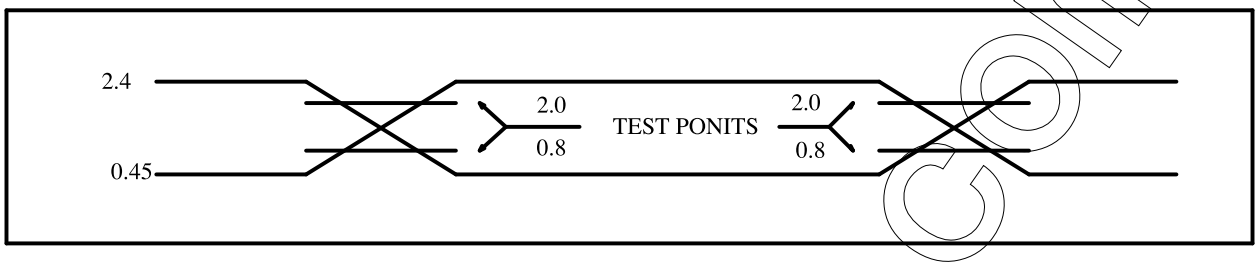
```
        RETI

MAIN()

        DISI

        P5=0
        !P5=0
        P6=0
        !P6=0XFF
        P7=0
        !P7=0
        P8=0
        !P8=0
        P9=0
        IF P_MS_SEL
       !P9=0B00000111
       SPIC=0B01000100
        ELSE
         !P9=0B00100111
       SPIC=0B01000101
      ENDIF
```

```
        D7=1
        R_0=0
        D6=0
        R_0=0
        D7=0
        WHILE++RSR!=0X40
        RSR=0

        P_SPI_SS=1

        ENI

LOOP:
        WDTC

        IF P_MS_SEL==0
        SPIWB=R_CODE
        DISI
IF SPI_RUN==0
        IF P_SPI_SS==0
        R_CODE++
```

```
                SPI_RUN=1
            ENDIF
        ENDIF
    ENI
ENDIF



IF P_START==0
    IF B_KEY==0
        B_KEY=1
            IF SPI_RUN==0
                P_SPI_SS=0
                SPIWB=0xAA
                FOR R_ACC=1,R_ACC!=0,R_ACC++
                  NOP
                  NOP
                NEXT


                SPI_RUN=1
            ENDIF
        ENDIF
    ELSE
        B_KEY=0
    ENDIF
    GOTO LOOP

    EOP
    ORG 0XFFF
    JMP MAIN
```

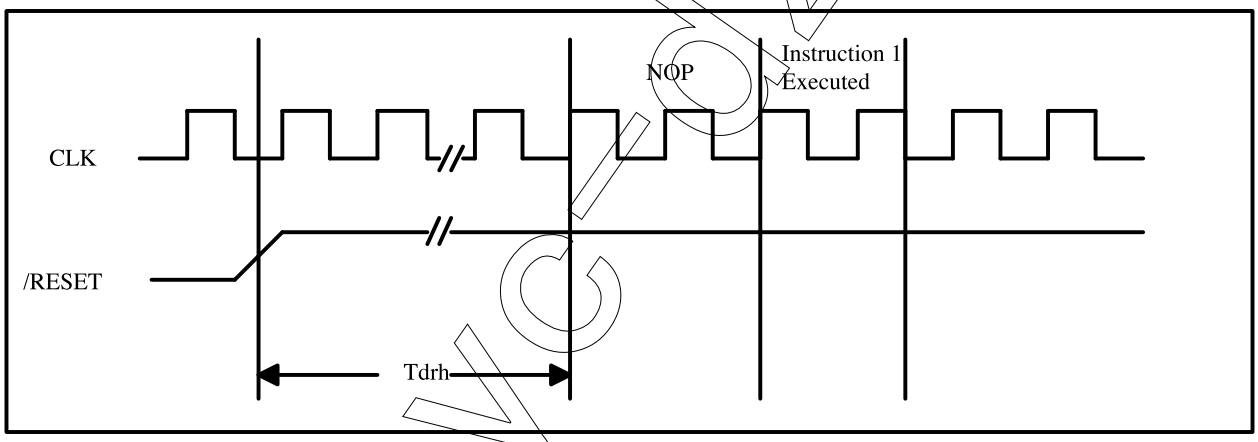
XI. TIMING DIAGRAMS

AC Test Input/Output Waveform

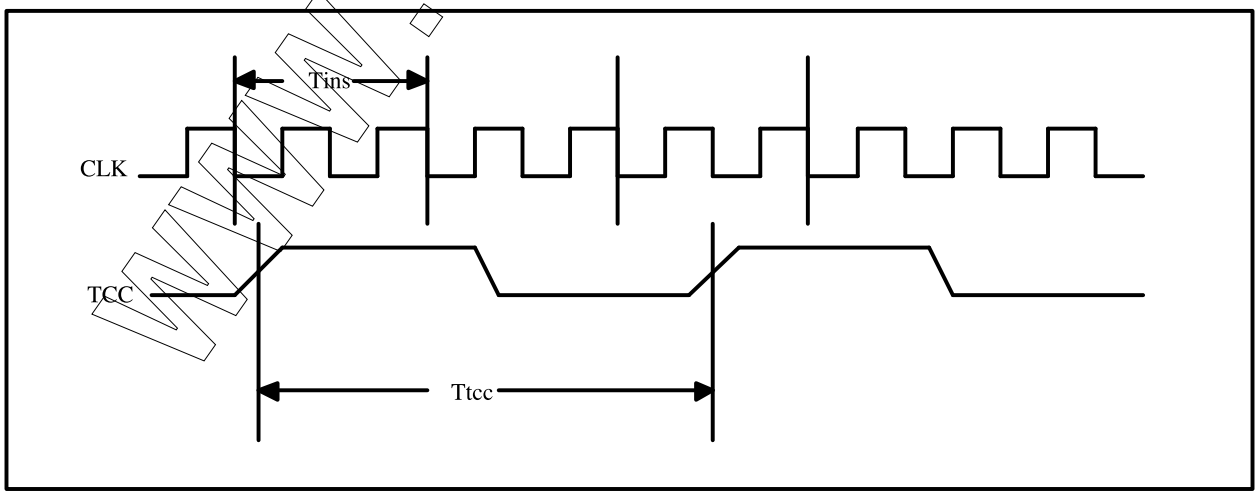


AC Testing : Input is driven at 2.4V for logic "1", and 0.45V for logic "0". Timing measurements are made at 2.0V for logic "1", and 0.8V for logic "0".

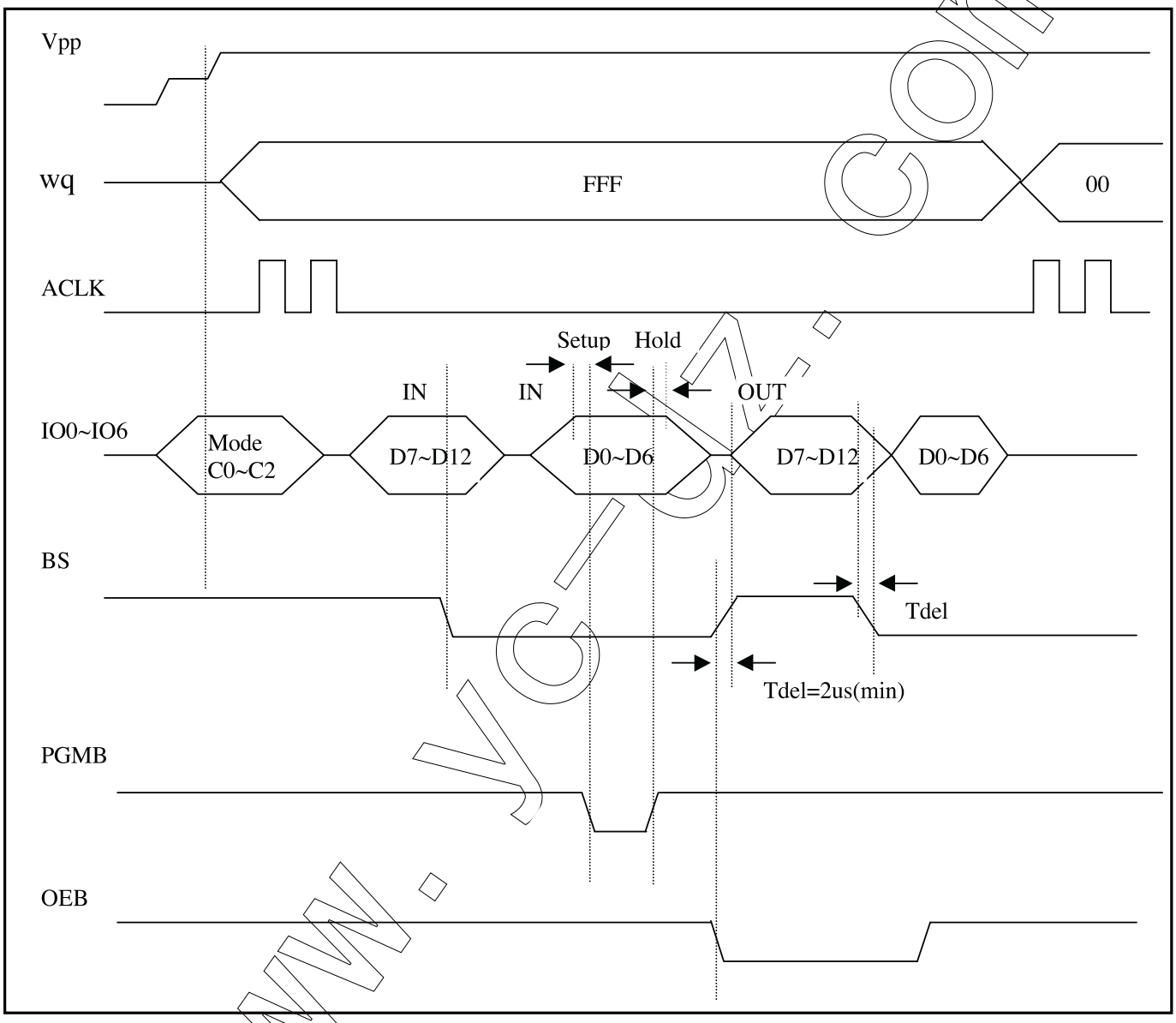
RESET Timing (CLK="0")



TCC Input Timing (CLK="0")



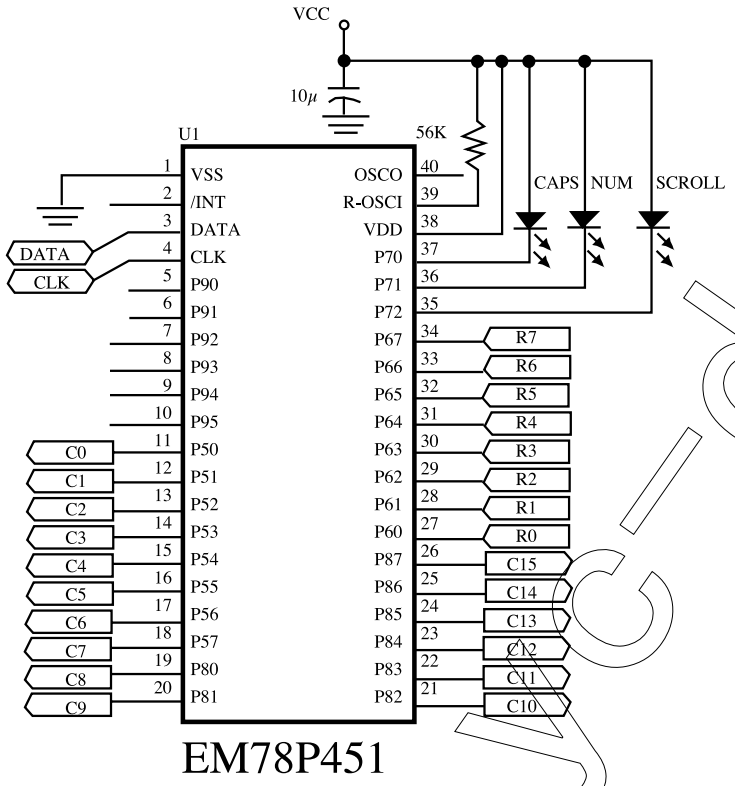
REGULAR and OPTION MODE Timing Waveform



Attention : 1. Setup & Hold time of data-in D0~D6

2. ACLK

XII. APPLICATION CIRCUIT



	R0	R1	R2	R3	R4	R5	R6	R7
C0			058				064	
C1		044					057	
C2	110	016	001	002	017	031	046	
C3	045	030	112	003	018	032	047	
C4	115	114	113	004	019	033	048	
C5	035	021	006	005	020	034	049	050
C6	036	022	007	008	023	037	052	051
C7		118	119	010	025	039	054	
C8	116	015	120	121		029	043	061
C9	117	028	013	009	024	038	053	
C10	041	027	012	011	026	040	042	055
C11		092	076	122	091	093	090	084
C12	099	097	075	123	096	098	095	089
C13	104	102	085	086	101	103	100	105
C14	083		080	081	016	108	126	079
C15	060			124	125			062