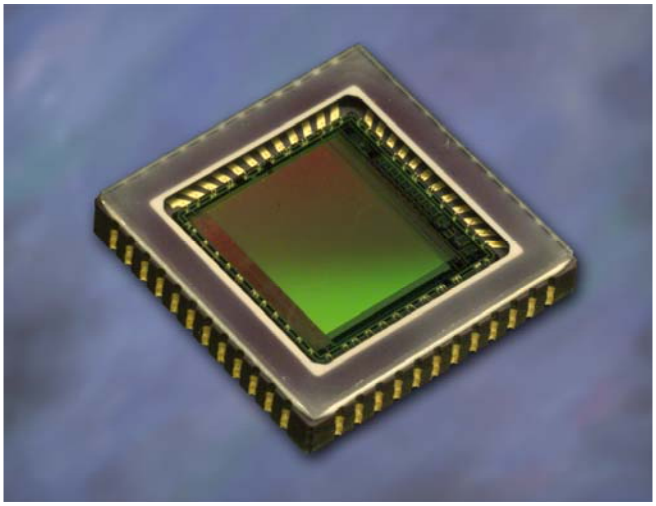
Kodak Digital Science^{TM} KAC – 1310

1280 x 1024 SXGA CMOS Image Sensor



Features

- ½” Color SXGA Advanced CMOS Image Sensor
- 1280 x 1024 active imaging pixels - progressive scan
- Monochrome or Bayer (RGB or CMY) Color Filters
- 6.0µm pitch square pixels with microlenses
- Kodak patented pinned photodiode architecture; high blue QE, low dark current, lag free
- High sensitivity, quantum efficiency, and charge conversion efficiency
- True Correlated Double Sampling for low read noise
- Low fixed pattern noise and wide dynamic range
- Antiblooming control and Continuous variable speed rolling electronic shutter
- Single 3.3V power supply; Single master clock
- Digitally programmable via I^2C compatible interface
- Pixel addressability to support ‘Window of Interest’ windowing, resolution, and sub-sampling
- External sync signal for use with strobe flash
- On-chip 20x programmable gain for white balance and exposure gain
- 10-bit, pipelined algorithmic RSD ADC
- 15 fps full SXGA at 20MHz Master Clock Rate
- 48 pin CLCC package
- Dark reference pixels with automatic Frame Rate Dark Clamp
- Encoded Sync data stream
- Column offset correction circuitry

Key Specifications

- **Pixel size:** 6.0µm x 6.0µm
- **Resolution:** 1280 x 1024 active
- **Image Size:** 7.68mm x 6.14mm (~1/2”)
- **ISO:** 180
- **Saturation Signal:** 40,000 electrons
- **Scan Modes:** Progressive Scan
- **Shutter Modes:** Continuous and Single Frame Rolling Shutter Capture
- **Maximum Readout Rate:** 20 MSPS
- **Frame Rate:** 0-15 frames per second
- **System Dynamic Range:** 56dB (1 - 10 MHz); 48 dB (11 – 15 MHz); 44 dB (16 – 20 MHz)
- **Response Non-Linearity:** <2%, 0 – 90% Vsat
- **Programmable Gain Range:**
  Global: 7.5x, 0.02x steps
  White Balance: 2.7x, 0.02x steps
- **ADC:** 10-bit, RSD ADC (DNL +/-0.5 LSB, INL +/-1.0 LSB)
- **Power Dissipation:** <250mW (dynamic) / 25mW (standby)

Release Date: April 30, 2002

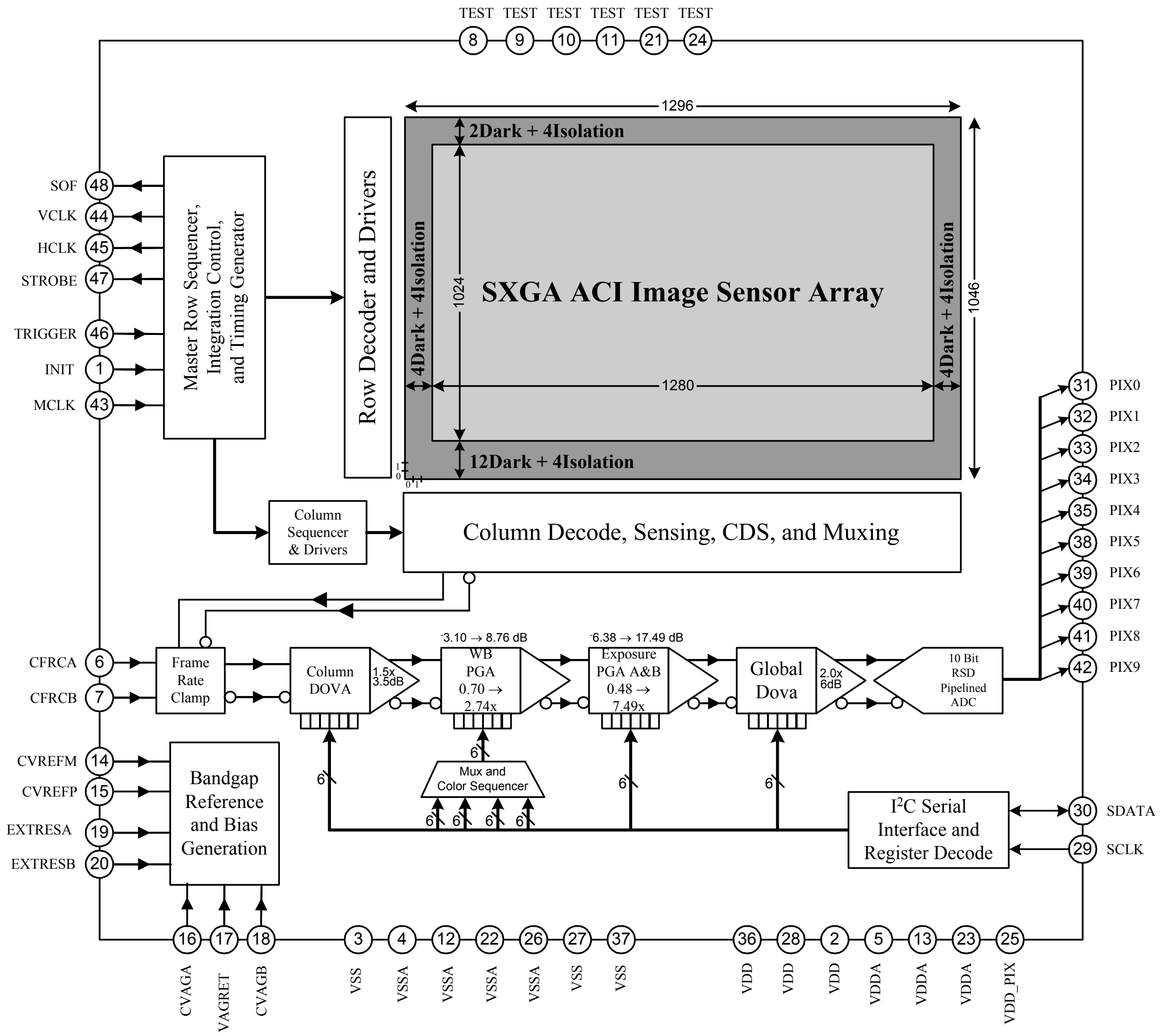


Figure 1: KAC-1310 Block Diagram

The KAC-1310 is a fully integrated, high performance ½” optical format Megapixel CMOS image sensor including integrated timing control and programmable analog signal processing. This sensor provides system designers a complete imaging solution with a monolithic image capture and processing engine. System benefits enable design of smaller, portable, low cost and low power systems. Each pixel on the sensor is individually addressable allowing the user to control the “Window of Interest” (WOI), panning and zooming, sub-sampling, resolution, exposure, white balance, and other image processing features via a two pin I^{2}C compatible interface. This device runs from a single 3.3V supply and single master clock.

The imager uses Kodak’s patented Pinned Photodiode CMOS active pixels. The 6.0µm pixel design provides true correlated double sampling for low read noise operation, high quantum efficiency, low dark current, and no image lag. Kodak’s patented pixel design combined with low noise mixed signal circuits provides a high sensitivity, low noise integrated “camera on a chip”.

Table 1: KAC-1310 Pin Definitions:

Pin No.	Pin Name	Description	Pin Type	Power	Value	Pin No.	Pin Name	Description	Pin Type	Power	Value
1	INIT	Sensor Initialize	I	D		25	VDD_PIX	Pixel Array Power	P	A	3.3 V
2	VDD	Digital Power	P	D	3.3 V	26	VSSA	Analog Ground	G	A	0 V
3	VSS	Digital Ground	G	D	0 V	27	VSS	Digital Ground	G	D	0 V
4	VSSA	Analog Ground	G	A	0 V	28	VDD	Digital Power	P	D	3.3 V
5	VDDA	Analog Power	P	A	3.3 V	29	SCLK	I^{2}C Serial Clock Line	I/O	D	3.3k Ω
6	CFRCA	Frame Rate Clamp Capacitor A	O	A	0.1µF	30	SDATA	I^{2}C Serial Data Line	I/O	D	3.3k Ω
7	CFRCB	Frame Rate Clamp Capacitor B	O	A	0.1µF	31	PIX0	Output Bit 0=1_{10} Weight	O	D	
8	TST_VRO	Analog Test Reference Output	O			32	PIX1	Output Bit 1=2_{10} Weight	O	D	
9	TST_VSO	Analog Test Signal Output	O			33	PIX2	Output Bit 2=4_{10} Weight	O	D	
10	TST_VRI	Analog Test Reference Input	I			34	PIX3	Output Bit 3=8_{10} Weight	O	D	
11	TST_VSI	Analog Test Signal Input	I			35	PIX4	Output Bit 4=16_{10} Weight	O	D	
12	VSSA	Analog Ground	G	A	0 V	36	VDD	Digital Power	P	D	3.3 V
13	VDDA	Analog Power	P	A	3.3 V	37	VSS	Digital Ground	G	D	0 V
14	CVREFM	ADC Bottom Bias Ref Capacitor	O	A	0.1µF	38	PIX5	Output Bit 5=32_{10} Weight	O	D	
15	CVREFP	ADC Top Bias Ref Capacitor	O	A	0.1µF	39	PIX6	Output Bit 6=64_{10} Weight	O	D	
16	CVAGA	Common Mode Capacitor Input	O	A	0.1µF	40	PIX7	Output Bit 7=128_{10} Weight	O	D	
17	VAGRET	Return for VAG external caps	O	A		41	PIX8	Output Bit 8=256_{10} Weight	O	D	
18	CVAGB	Common Mode Reference Capacitor	O	A	0.1µF	42	PIX9	Output Bit 9=512_{10} Weight	O	D	
19	EXTRESA	External Bias Resistor	I	A	39k Ω	43	MCLK	Master Clock = Pixel Rate	I	D	
20	EXTRESB	External Bias Resistor	I	A	39k Ω	44	VCLK	Line Sync	O	D	
21	NC					45	HCLK	Pixel Sync	O	D	
22	VSSA	Analog Ground	G	A	0 V	46	TRIGGER	Sensor Trigger Signal	I	D	
23	VDDA	Analog Power	P	A	3.3 V	47	STROBE	External Sync for Strobe Flash	O	D	
24	TST_INJ	Pixel Row 1046./1047 Inj Bbias In	I		3.3 V	48	SOF	Start of Frame Sync	O	D	

Legend:
P = VDD
G = VSS
I = Input
O = Output
D = Digital
A = Analog

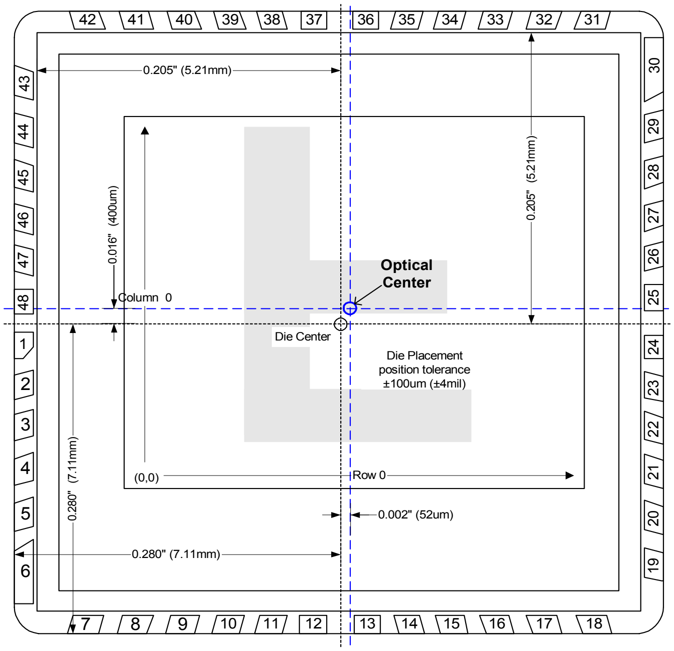


Figure 2. Pinout Diagram

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Kodak Digital Science KAC-1310 CMOS Image Sensor

1. Overview

The KAC-1310 is a solid state CMOS Active CMOS Imager **(ACI^{TM})** that integrates the functionality of complete analog image acquisition, digitizer, and digital signal processing system on a single chip. The image sensor comprises a SXGA format pixel array with 1280x1024 active elements. The image size is fully programmable to user-defined windows of interest. The pixels are on a 6.0µm pitch. High sensitivity and low noise are a characteristic of the pinned photodiode[2] architecture utilized in the pixels. The sensor is available in a Monochrome version without microlenses, or Bayer (RGB or CMY) patterned Color Filter Arrays **(CFAs)** with standard microlenses to further enhance sensitivity.

Integrated timing and programming controls allow video or still image capture progressive scan modes. Frame rates are programmable while keeping the Master Clock frequency constant. User programmable row and column start/stop allow windowing down to a 1x1 pixel window for digital zoom of a panable viewport. Sub-sampling provides reduced resolution while maintaining constant field of view.

The analog video output of the pixel array is processed by an on-chip analog signal pipeline. Correlated Double Sampling **(CDS)** eliminates the pixel reset temporal and pattern noise. The Frame Rate Clamp **(FRC)** enables real time optical black level calibration and offset correction. The programmable analog gain consists of exposure/global gain to map the signal swing to the ADC input range, and white balance gain to perform color balance in the analog domain. The ASP signal chain consists of (1) Column op-amp (1.5x fixed gain); (2) Column DOVA(1.5x fixed gain); (3) White Balance PGA (0.70 → 2.74x); (4) Global PGA (0.48 → 7.50x); and (5) Global DOVA (2.0x fixed gain). These Digitally Programmable Amplifiers **(DPGAs)** allow real time color gain correction for Auto White Balance **(AWB)** as well as exposure gain adjustment. Offset calibration can be done on a per column basis and globally. This per-column offset correction can be applied by using stored values in the on chip registers. A 10-bit Redundant Signed Digit **(RSD)** ADC converts the analog data to a 10-bit digital word stream. The fully differential analog signal processing pipeline serves to improve noise immunity, signal to noise ratio, and system dynamic range. The sensor uses an industry standard two line I^{2}C compatible serial interface. It operates with a single 3.3V power supply with no additional biases and requires only a single Master Clock for operation up to 20 MHz. It is housed in a 48 pin ceramic LCC package.

The KAC-1310 is designed taking into consideration interfacing requirements to standard video encoders. In addition to the 10 bit Bayer (RGB or CMY) encoded data stream, the sensor outputs the valid frame, line, and pixel sync signals needed for encoding. The sensor interfaces with a variety of commercially available video image processors to allow encoding into various standard video formats. In addition, the 3 sync signals can be integrated into the video data stream eliminating the need of the 3 sync outputs

The KAC-1310 is an elegant and extremely flexible single chip solution that simplifies a system designer's tasks of image sensing, processing, digital conversion, and digital signal processing to a high performance, low cost, low power IC. A chip solution that supports a wide range of low power, portable, consumer digital imaging applications.

2.0 Sensor Interface

2.1 Pixel Architecture

The KAC-1310 sensor comprises a 1280x1024 active pixel array and supports progressive readout. The basic operation of the pixel relies on the photoelectric effect where, due to its physical properties, silicon is able to detect photons of light. The photons generate electron-hole pairs in direct proportion to the intensity and wavelength of the incident illumination. The application of an appropriate bias allows the user to collect the electrons and meter the charge in the form of a useful parameter such as voltage.

The pixel architecture is based on a "four transistor" **(4T)** Advanced CMOS Imager^{TM1} pixel which requires all pixels in a row to have common Reset, Transfer, and Row Select controls. In addition all pixels have common supply (V_{DD}) and ground (V_{SS}) connections. This optimized cell architecture provides enhancements such as noise reduction, fill factor maximization, and anti-blooming. The use of pinned photodiodes[2] and proprietary transfer gate devices in the photo-elements enables enhanced sensitivity in the entire visual spectral range and a low lag operation. The nominal photo-responses of the KAC-1310 are shown in Figure 2 (monochrome sensor without microlenses), Figure 3 (Bayer RGB sensor with microlenses) and Figure 4 (Bayer CMY sensor with microlenses).

In addition to the imaging pixels, there are additional pixels called dark and isolation pixels at the periphery of the imaging section (see Figure 1). The dark pixels are covered by a light-blocking shield that makes these pixels insensitive to photons. These pixels provide the sensor means to measure the dark level offset which is used downstream in the signal processing chain to perform auto black level calibration. The isolation pixels are provided at the array's periphery to eliminate inexact measurements due to light piping into the dark pixels adjacent to active pixels and for extra pixels needed for color interpolation algorithms. Electronic shuttering, also known as electronic exposure timing in photographic terms, is a standard feature. The pixel integration time can be widely varied from a small fraction of a given frame readout time to the entire frame time.

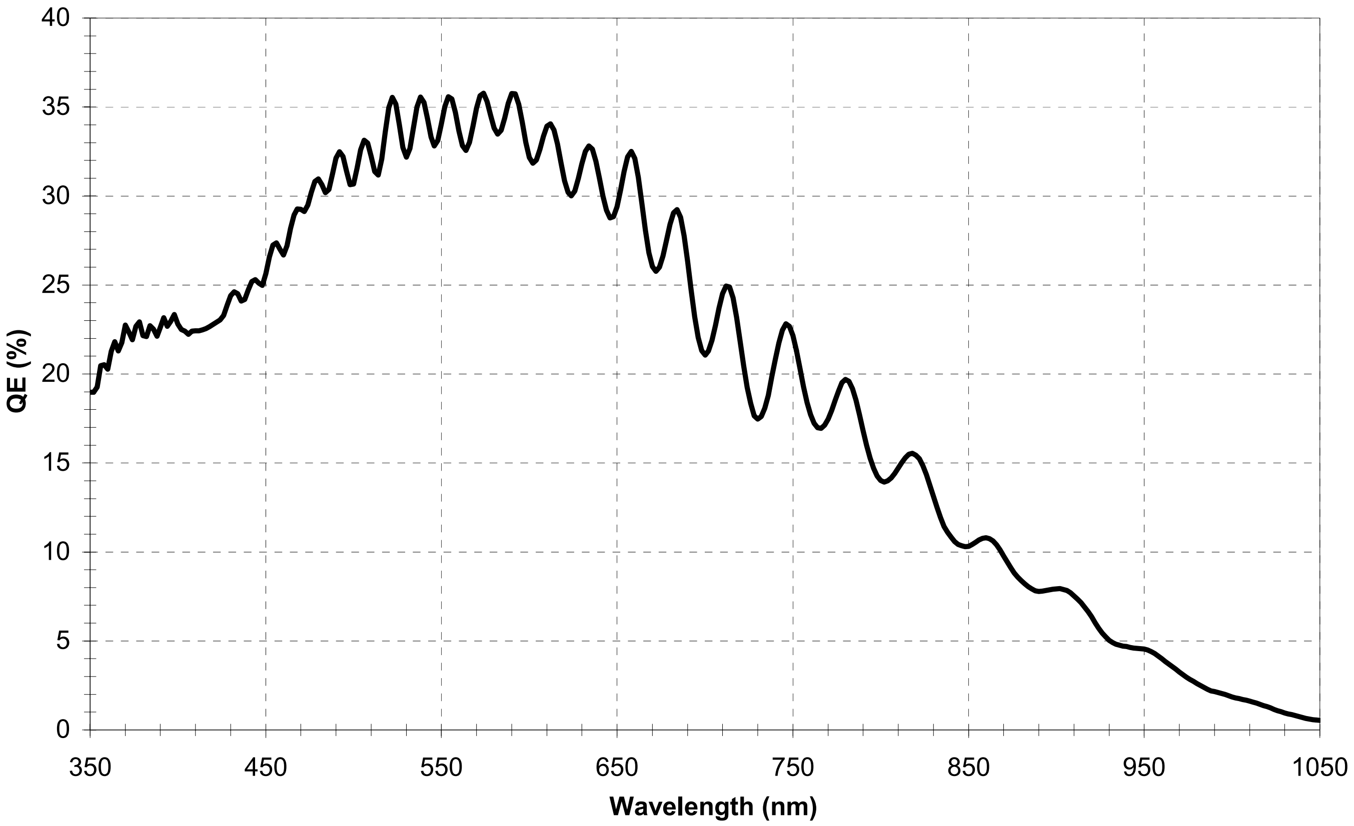

Figure 3: KAC-1310 Typical Monochrome Spectral Response

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[1] Advanced CMOS Imager (ACI) is a Kodak trademark
[2] Patents held jointly by Kodak and Motorola

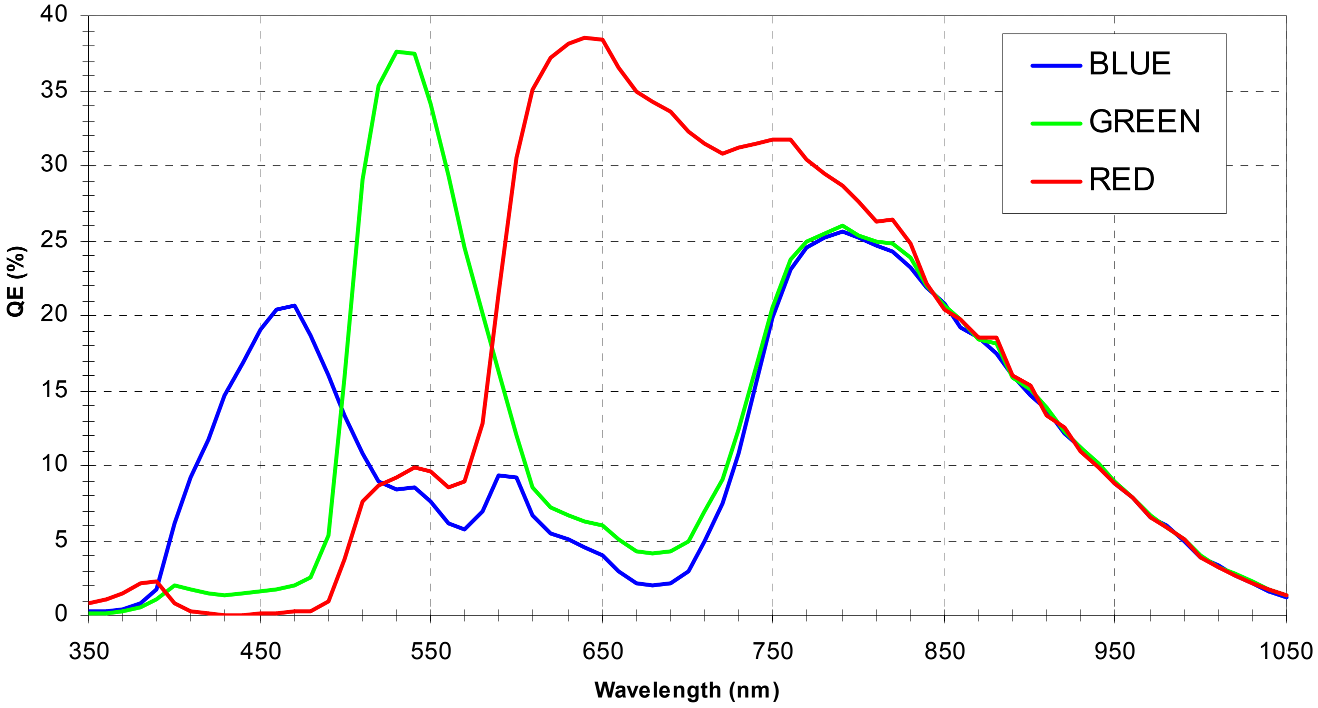


Figure 4: KAC-1310 Typical Bayer RGB Spectral Response

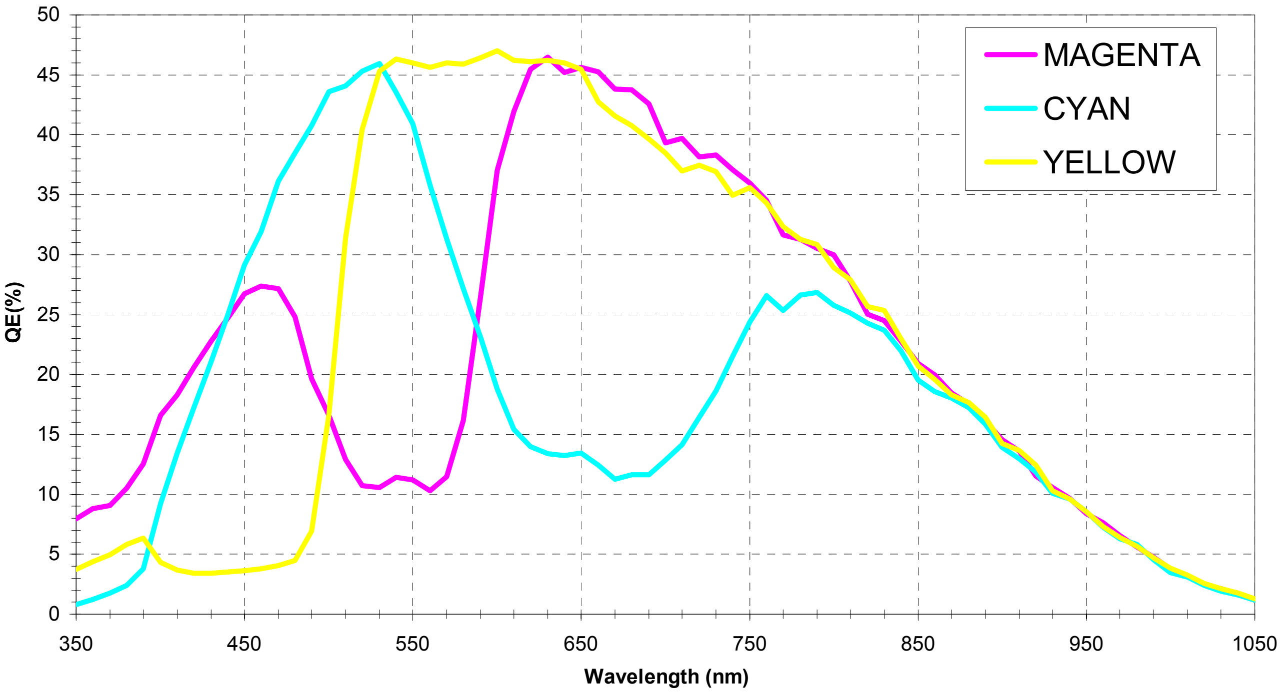
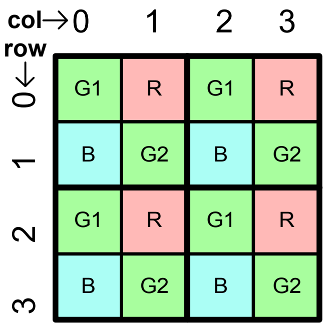


Figure 5: KAC-1310 Typical Bayer CMY Spectral Response

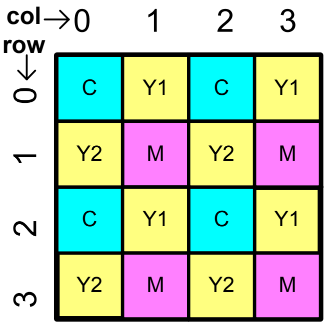
2.2 Color Filters and Lenslets

The KAC-1310 family is offered with the option of monolithic polymer color filter arrays **(CFA's)**. The combination of an extremely planarized process and proprietary color filter technology results in CFA's with superior spectral and transmission properties. It is available in Bayer RGB (Figure 6) or CMY (Figure 7) patterns. The complimentary Bayer CMY array provides a 50% increase in sensitivity over primary RGB pattern and are often the best choice for low light applications. This is due to the higher quantum efficiency **(QE)** and larger wavelength spread per color. If the application is utilizing a color correction matrix, then this matrix will automatically convert the CMY to RGB. Other wise a simple matrix must be applied to affect the conversion from CMY to RGB space.



row↓ col→	0	1	2	3
0	G1	R	G1	R
1	B	G2	B	G2
2	G1	R	G1	R
3	B	G2	B	G2

Figure 6: Optional Bayer RGB Pattern CFA



row↓ col→	0	1	2	3
0	C	Y1	C	Y1
1	Y2	M	Y2	M
2	C	Y1	C	Y1
3	Y2	M	Y2	M

Figure 7: Optional Bayer CMY Pattern CFA

Applications requiring higher sensitivity can benefit from the microlens arrays shown in Figure 8. The lenslet arrays can improve the fill factor (aperture ratio) of the sensor by approximately 1.6x depending on the F-number of the lens used in the camera system. Microlenses yield the greatest benefits when the main lens has a high F-number or a highly telecentric design. The fill factor of the pixels without microlenses is ~40%.

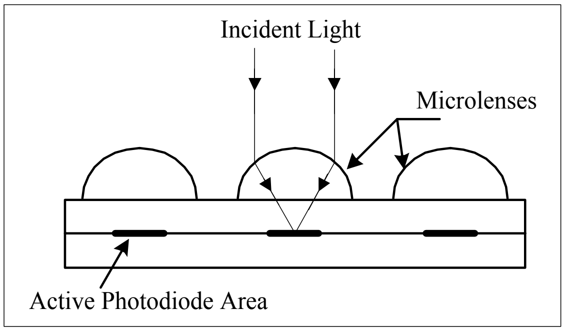


Figure 8: Increase of sensitivity due to microlenses

2.3 Frame Capture Modes

There are two frame capture modes:

1) Continuous Frame Rolling Shutter **(CFRS)**
2) Single Frame Rolling Shutter **(SFRS)**

The sensor can be put into either one of these modes by writing either "1" or "0" to **cms** bit (bit 6) of Capture Mode Control Register (40_h) (Table 20 on page 38).

The KAC-1310 uses a progressive readout mode. Progressive scanning refers to non-interlaced or sequential row-by-row scanning of the entire sensor in a single pass. The image readout happens at one instant of time.

2.3.1 Continuous Frame Rolling Shutter Capture Mode (CFRS)

The default mode of image capture is the Continuous Frame Rolling Shutter Capture Mode **(CFRS)**. In this mode the TRIGGER input pin is ignored. This mode is most suitable for full motion video capture and will yield SXGA sized Frame Rates up to 15 FPS at 20 MHz MCLK and VGA frames at >30 FPS. In this mode the image integration and row readout take place in parallel. While a row of pixels is being readout, another row or rows are being integrated. Since the integration time **(T_{int})** must be equal for all rows, the start of integration for rows is staggered.

2.3.1.1 CFRS Video Encoded Data Stream

The Encoded Sync Control Register (65_h) (Table 44 on page 51) allows the user to select how the output pixel data stream in CFRS mode is encoded/formatted. In default mode, internally generated signals SOF, VCLK, HCLK etc. drive the integration and readout of the pixel data frames, but only the valid pixel data is readout of the sensor. When a “1” is written to bit 5, it causes the output pixel data to be encoded with four (4) 10-bit pixel codes at the beginning of each line for SOF, VCLK and End Of Frame (EOF) signals. Operation in this mode will allow a camera system to capture streaming video and reconstruct the frame afterwards when the SOF, VCLK, and HCLK signals are no longer available. The Video Encoded Signal Definitions, (Table 2), defines the four (4) 10-bit pixel code data that represents the SOF, VCLK, and EOF signals.

Signal	Description	Data
SOF	Start of Row readout (i.e. Readout of Row 1)	[3FF][3FF][3FF][3FF] Note: $3FF_h = 1023_d$ $000_h = 0_d$
VCLK	Start of Row readout of Rows 2+	[3FF][3FF][000][000]
EOF	Readout of last Row complete	[000][000][000][000]

Table 2. Video Encoded Signal Definitions

2.3.2 Single Frame Rolling Shutter capture mode (SFRS)

In this mode of capture, the start of integration is triggered by the TRIGGER signal. Similar to the CFRS capture mode, readout of each row follows the integration of that row. The imager can be placed in SFRS capture mode using register 40_h (see Table 20 on page 38). In this mode the imager will remain idle until the TRIGGER pin is pulled high. The imager then begins integration followed by image readout. If the TRIGGER input is still high when the SFRS Frame is finished reading out, then a second Frame is started. Detailed timing can be found in Figure 21 on page 22. There are additional controls for SFRS mode that can be found in register 42_h, Table 22 on page 40.

The TRIGGER signal can be generated internally by the sensor or be driven via Pin #46 of the sensor. To set whether the signal is generated internally or externally, along with other setting of this signal, refer to TRIGGER and STROBE Control register (42_h), Table 22 on page 40.

2.3.3 Window of Interest (WOI) Control

The pixel data to be read out of the device is defined as a ‘Window of Interest’ (**WOI**). The window of interest can be defined anywhere on the pixel array at any size. The user provides the upper-left pixel location and the size in both rows and columns to define the WOI. The WOI is defined using the WOI Pointer, WOI Depth, and WOI Width registers, (Table 23 on page 41 through Table 30 on page 43). Please refer to Figure 9 for a pictorial representation of the WOI within the active pixel array. Any pixels not included in the WOI will be skipped over and never readout (note: the minimum valid values are 2 for the WOI row pointer (wrp), and 0 for the WOI column pointer (wcp)). The first pixel readout will always be the first pixel of the WOI.

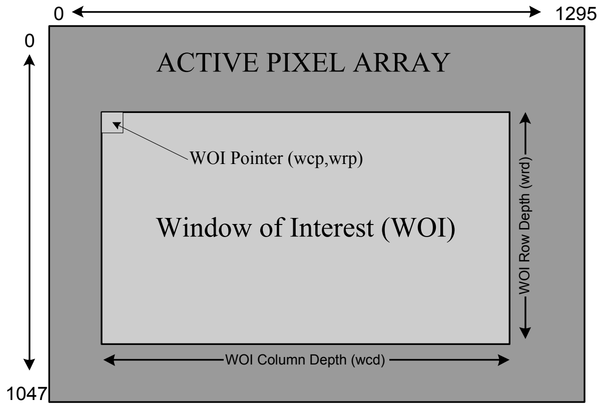
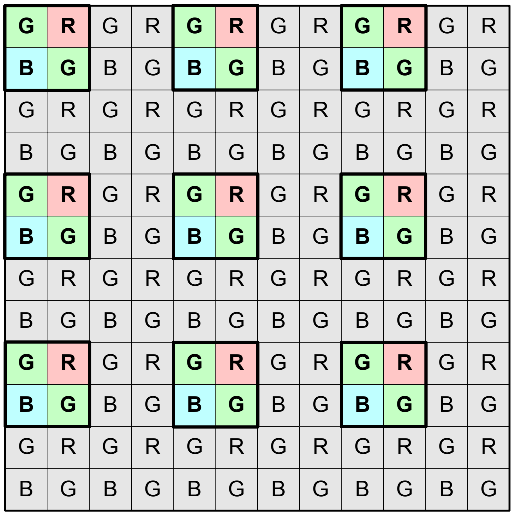


Figure 9: WOI Definition

2.3.4 Sub-Sampling Control (Resolution)

The WOI can be sub-sampled in either monochrome or color pixel space in both the horizontal and vertical direction independently. The resolution of each axis can be set to four different sampling rates: full, ½, ¼, or $^1/_8$. Sub-sampling the imager by ¼ in both horizontal and vertical directions results in only $^1/_{16}$ of the pixels being readout. The frame readout rate can therefore be increased by 16x. The user controls the sub-sampling via the Sub-Sample Control Register (41_h), Table 21 on page 39. An example of RGB Bayer space sub-sampling is shown in Figure 10. If the imager is set as a color imager then the sub-sampling is done by reading out two cols/rows and then skipping two. This prevents the sub-sampling from breaking up a color kernel. If the imager is set to Monochrome mode the sub-sampling will skip every other col/row performing a more uniform reduction is resolution. Activating Sub-Sampling alone will not increase the Frame Rate.

The Frame Rate is controlled by the Virtual Frame (see Section 2.4). For example, if Sub-Sampling is first turned on to $^1/_8$ x $^1/_8$ mode, the WOI will shrink by $^1/_{64}$. To keep the Frame Rate constant, the KAC-1310 fills in the rest of the rows and columns with blanking pixels. The Virtual Frame can now be reduced by 1/8 x 1/8 to take advantage of the Sub-Sampled WOI. The Frame Rate will now have increased by 64x with no compromise to the field of view (in CFRS mode).



G	R	G	R	G	R	G	R	G	R	G	R
B	G	B	G	B	G	B	G	B	G	B	G
G	R	G	R	G	R	G	R	G	R	G	R
B	G	B	G	B	G	B	G	B	G	B	G
G	R	G	R	G	R	G	R	G	R	G	R
B	G	B	G	B	G	B	G	B	G	B	G
G	R	G	R	G	R	G	R	G	R	G	R
B	G	B	G	B	G	B	G	B	G	B	G
G	R	G	R	G	R	G	R	G	R	G	R
B	G	B	G	B	G	B	G	B	G	B	G
G	R	G	R	G	R	G	R	G	R	G	R
B	G	B	G	B	G	B	G	B	G	B	G

Figure 10: RGB Bayer ½ x ½ Sub-sample Example. Sub-sample Control Register(41_h) = xxx10101$_b$

2.4 Virtual Frame (VF)

Changing the WOI does not change the Frame Rate of the imager. This is done by varying the size of a Virtual Frame surrounding the WOI. Refer to Figure 11 for a pictorial description of the Virtual Frame and its relationship to the WOI.

The VF is a method for defining the horizontal and vertical blanking (over clocking) in Frame Readout. As the WOI is adjusted, the total Frame Size is set by the VF. To maintain constant Frame Rate, the KAC-1310 adjusts the number of blanking pixels to account for changes in the WOI. The VF can be set to any size. If the VF is greater than the WOI then the readout is padded with blanking pixels (invalid dark pixels). The WOI and the VF may both be larger than the actual imager size. In this case the WOI is also padded with blanking pixels (invalid dark pixels). Figure 11 illustrates a WOI smaller than the VF. If the WOI is set larger than the VF, then the WOI will be clipped by the VF and the Frame Rate will still be equal to the VF size.

The first pixel of the VF is always equal to the first pixel of the WOI. Thus the WOI is always in the upper left corner of the VF.

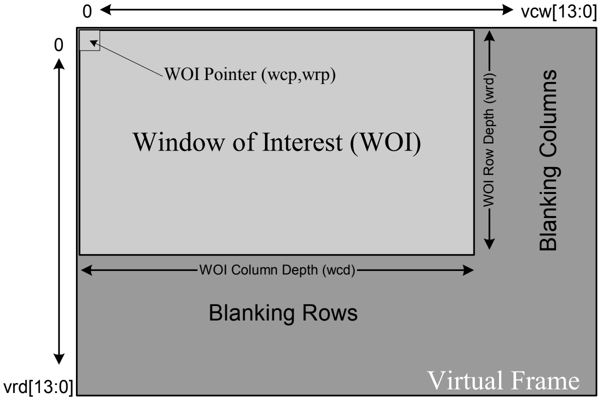


Figure 11: Virtual Frame Definition

2.5 Integration Time

2.5.1 CFRS Integration Time

The Integration Time in CFRS is defined and quantized by the time to read out a single row. Once a Virtual Frame has been defined, the time to read out one row can be calculated. Any integer multiple of the Row Time (T_{row}) can be selected. The number of Row Times desired for integration time is programmed into the Integration Time Registers. The Integration Time is defined by a combination of the width of the VF and the Integration Time Registers ($4E_h$ and $4F_h$), (Table 31 and Table 32 on page 49); and can be expressed as:

Integration Time (T_{int}) = ($cint_d$ + 1) * T_{row}

where $cint_d$ is the number of virtual frame row times desired for integration time. Therefore, the integration time can be adjusted in steps of VF row times.

Row Time (T_{row}) = (vcw_d+shA_d+shB_d+19) * $MCLK_{period}$

If the integration time is programmed to be larger than the VF then it will be truncated to the number of rows in the VF. The VF must be increased before the Integration Time can be increased further.

NOTE: The **upd bit** of Reg $4E_h$ is used to indicate a change to **cint**[13:0]. Since multiple I^2C writes may be needed to complete desired frame to frame integration time changes, the **upd** bit signals that all desired programming has been completed, and to apply these changes to the next frame captured. This prevents undesirable changes in integration time that may result from I^2C writes that span the “End of Frame” boundary. This **upd** bit has to be toggled from its previous state in order for the new value of **cint**[13:0] to be accepted/updated by the sensor and take effect. i.e. If its previous state is “0”, when writing a new **cint** value, first write cint[7:0] to register $4F_h$, then write both **cint** [13:8] and “1” to the **upd** bit to register $4E_h$. The **upd** bit should be sent as close to the Start of Frame as possible to ensure a smooth transition from the old integration time to the new.

2.5.2 SFRS Integration Time

Just as with operation in CFRS mode, the integration time is defined by a number of Row Times. As before:

Row Time (T_{row}) = (vcw_d+shA_d+shB_d+19) * $MCLK_{period}$

where vcw_d defines the number of columns in the virtual frame. The user controls vcw_d via the Virtual Frame Column Width registers (Table 35 and Table 36 on page 46).

Integration Time (T_{int}) = ($cint_d$ + 1) * T_{row}

where $cint_d$ is the number of virtual frame row times desired for integration time.

Note: In CFRS operation, the integration time is limited (clipped) by the readout time (which is also the Frame Time). In SFRS mode, the Frame Time is expanded to include any programmed integration time. Thus in SFRS operation there is no boundary to the integration time.

2.6 Frame Rate

The Frame Rate can be defined as the time required to readout an entire frame of data plus the required blanking time. There is a different relationship between the Frame Rate and Virtual Frame for CFRS and SFRS mode operation.

2.6.1 CFRS Frame Rate

In CFRS, the Frame Rate of the imager is controlled by varying the size of the Virtual Frame surrounding the WOI, and is independent of Integration Time. Refer to Figure 11 for a pictorial description of the Virtual Frame **(VF)** and its relationship to the WOI. In CFRS operation, the Frame Rate **(FR)** (Frame Rate = 1/Frame Time) is defined by the VF size and clock speed (MCLK). The Frame Time **(FT)** and can be expressed as:

FT =(vrd_d +1) * T_{row}

where vrd_d defines the number of rows in the virtual frame. The user controls vrd_d via the Virtual Frame Row Depth registers (Table 33 and Table 34 on page 45).

If the VF width (vcw_d) is <1296, then the timing block holds the two Frame Rate Clamp **(FRC)** rows to a length of 1296 even while all of the other rows are shorter. This is to ensure enough time for the clamping circuit. If the FRC is turned off (see Clamp Control and HCLK Delay Register (64_h), it is recommended that the CFRCA and CFRCB pins be tied to ground directly (i.e. no 0.1 µF capacitor).

NOTE: The WOI and Integration Time will be clipped by the VF.

2.6.2 SFRS Frame Rate

There are two main differences when running in SFRS mode versus CFRS mode. The first is that the Frame Rate is no longer the readout rate. In SFRS mode there is no overlap of the Integration and the readout. Therefore, at the top of each Frame, Integration must first occur then readout. The Frame Rate is now Integration plus readout.

The second major difference is the length of readout. In CFRS mode, the only reason for making the VF length larger than the WOI length (vrd > wrd) is to add vertical blanking rows to control the time between frames. In SFRS mode, the time between frames is controlled by the TRIGGER input pin, and therefore vertical blanking serves no purpose. Rather than have the user change the VF depth (vrd), the imager uses the WOI depth (wrd).

Therefore, the Frame Rate equations are:

Frame Time (T_{frame}) =

Integration Time (T_{int})+ Readout Time (T_{rd})

Where:

Integration Time (T_{int}) = ($cint_d + 1$) * T_{row}

Readout Time (T_{rd}) = T_{row} * (wrd_d+1)

Row Time (T_{row}) = (vcw_d+shA_d+shB_d+19) * $MCLK_{period}$

Frame Rate = 1/Frame Time

3.0 Analog Signal Processing Chain (ASP)

The KAC-1310's analog signal processing **(ASP)** chain incorporates Correlated Double Sampling **(CDS),** Frame Rate Clamp **(FRC),** two Digitally Programmable Gain Amplifiers **(DPGA),** Offset Correction **(DOVA)**, and a 10-bit Analog to Digital Converter **(ADC)**. See Figure 1 for a block diagram of the ASP chain.

3.1 Correlated Double Sampling (CDS)

The uncertainty associated with the reset action of a capacitive node results in a reset noise which is proportional to kTC; 'C' being the capacitance of the node, 'T' the temperature, and 'k' the Boltzmann constant. A common way of eliminating this noise source in all image sensors is to use Correlated Double Sampling. The output signal is sampled twice, once for its reset (reference) level and once for the actual video signal. These values are sampled and held while a difference amplifier subtracts the reference level from the signal output. Double sampling of the signal eliminates correlated noise sources.

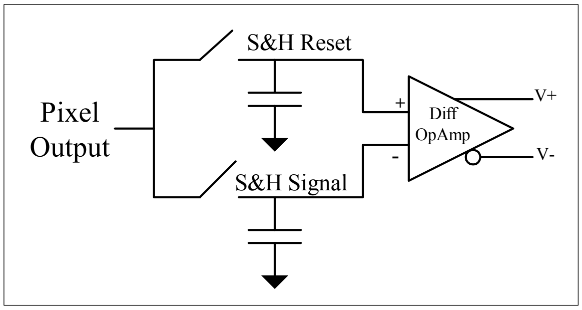


Figure 12: Conceptual block diagram of CDS

3.2 Frame Rate Clamp (FRC)

The FRC (Figure 13) is designed to provide a feed-forward dark level compensation. In the automatic FRC mode, the optical black level reference is reestablished each time that the image sensor begins a new frame. The KAC-1310 uses optical black (dark) pixels to establish this reference.

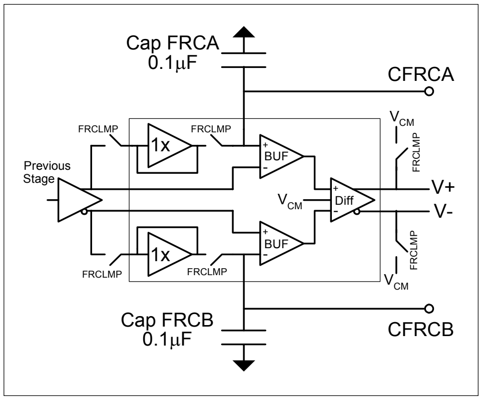


Figure 13: FRC Conceptual Block Diagram

The dark pixel sample period is automatically controlled internally and it is set to skip the first 3 dark rows and then sample the next 2 dark rows. When "dark clamping" is active, each dark pixel is processed and held to establish pixel reference level at the CFRCA and CFRCB pins. During this period, the FRC's differential outputs (V^+ and V^- on the Diff Amp) shown in Figure 13 are clamped to V_{cm}. Together, these actions help to eliminate the dark level offset, simultaneously establishing the desired zero code at the ADC output. The user can disable the FRC via the Clamp Control and HCLK Delay Register (64_h), (Table 43 on page 50) which allows the ASP chain to drift in offset. If the FRC is disabled, it is recommended that the CFRCA and CFRCB pins be grounded. Care should be exercised in choosing the capacitors for the CFRCA and CFRCB pins to reflect different Frame Rates. For small WOI or fast Frame Rates, a smaller capacitor may be used.

3.3 Column Digital Offset Voltage Adjust (CDOVA)

A programmable per-column offset adjustment is available on the KAC-1310. There are 64 registers that can be programmed with an offset that is added to each 64th column (Mod64 Column Offset Registers; Table 45 on page 52). Each register is 6 bits, (5 bits plus 1 sign bit), providing ±32 register values. This set of 64 values is then repeatedly applied to each bank of 64 columns in the sensor via the column DOVA stage of the ASP chain.

In addition to the per column offset there is a global column offset that can be added to every column. This is used to remove any variation of the dark level with respect to varying gain. The DC offset is loaded as a 6-bit value into the Column DOVA DC Offset Register, (Table 16 on page 34). The Column DOVA stage has only six bits of total range. The value in Register 20_h and 80_h-BF_h are added together prior to application to the column. If the sum is greater than ±31, it will be truncated to ±31.

3.4 Programmable Gain Amplifiers (PGA)

3.4.1 Gain Modes

Three different gain modes are available when the sensor is performing White Balance and Exposure gain. The gain mode is set using Register 22_h described in Table 18, page 36. The three gain modes are:

Raw Gain Mode (WB and Exposure)
Gain $\approx 0.6950 + 0.02175 * Reg_d$ $0 \le Reg_d \le 31$ $(0.0695x \rightarrow 1.36925x)$
$\approx 1.3475 + 0.04350 * (Reg_d - 31)$ $32 \le Reg_d \le 63$ $(1.3910x \rightarrow 2.7395x)$

Lin1 Gain Mode (WB and Exposure)
Gain $\approx 0.6950 + 0.04350 * Reg_d$ $0 \le Reg_d \le 47$ $(0.695x \rightarrow 2.7395x)$

Lin2 Gain Mode (Exposure gain stage only)
Gain $\approx 0.483 + 0.11119 * (Reg\ 10_h)_d$ $0 \le Reg_d \le 63$ $(0.483x \rightarrow 7.488x)$

Raw Gain Mode:
The three gain stages are each designed as two-piece linear gain stages where the gain increment doubles for the second half of the programmable range. The gain increment is 0.02175 for the first 32 programmable steps, and precisely twice that (0.04350) for the last 32 programmable steps.

Lin1 Gain Mode:
Some applications do not need the finer gain increment provided by the Raw Gain Mode in the first 32 register values. In Lin1 mode, every other step of the lower register is skipped, providing 16 uniform gain steps of 0.04350. As a result, the entire gain stage now appears to be a linear gain stage with 48 uniform steps of 0.04350.

Lin2 Gain Mode:
This mode is only available for the exposure gain mode. In this mode, both gain stages are automatically coordinated to affect a single gain stage. The gain step size of Lin2 Mode is almost, but not completely uniform. Any one step may deviate from the mean step size of 0.11119 by a small amount. This is due to the fact that Lin2 Mode actually varies two gain stages with fixed step sizes to make one equivalent gain step.

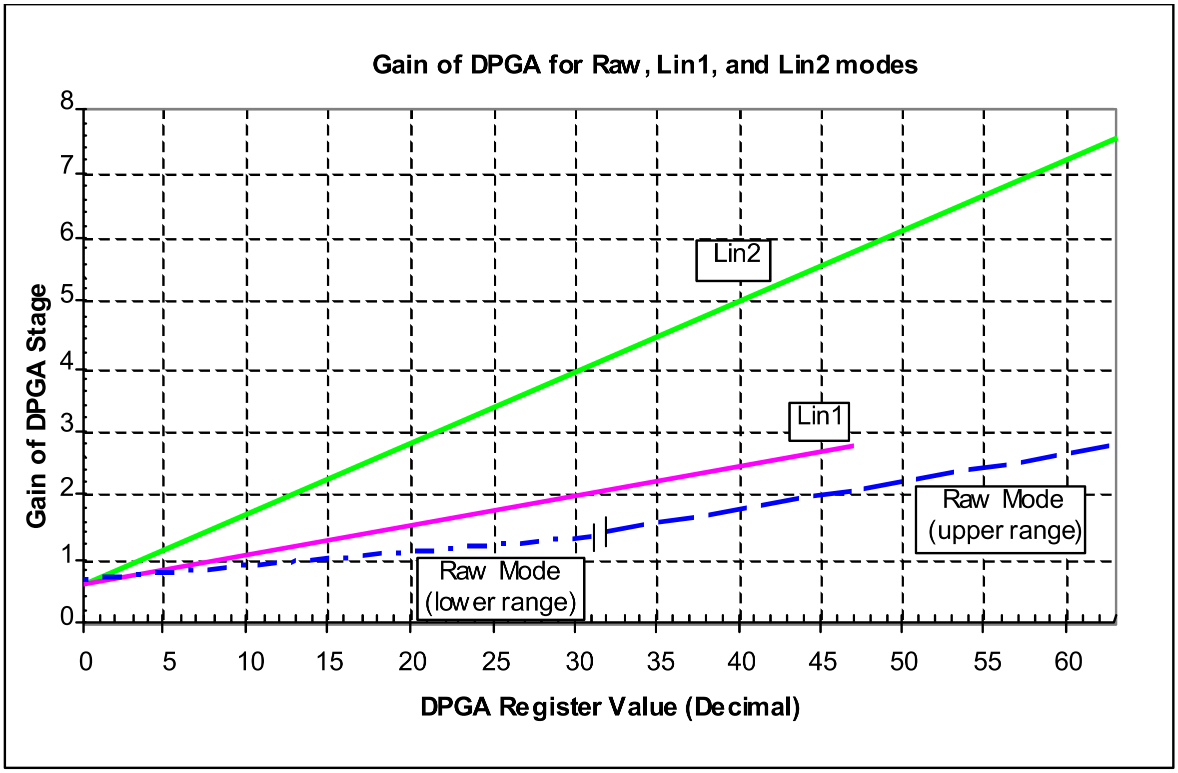


Figure 14: PGA Gain Modes

3.4.2 White Balance Control PGA (WB Gain)

[For the purposes of illustration, the following discussion assumes a Bayer RGB color pattern; with the appropriate correlation (as shown in Figure 15), the CMY Bayer pattern may be substituted throughout.]

The sensor produces three primary color outputs, Red, Green, and Blue. These are monochrome signals that represent luminance values in each of the primary colors. When added in equal amounts they mix to make neutral color. White balancing is a technique where the gain coefficients of the Green1, Red, Blue, and Green2 pixels comprising the Bayer RGB pattern are set so as to equalize their outputs for neutral gray color scenes. Since the sensitivity of the two green pixels in the Bayer pattern may not be equal, an individual color gain register is provided for each component of the Bayer pattern.

Once all color gain registers are loaded with the desired gain coefficients, white balance is achieved in real time and in analog space. The appropriate values are selected and applied to the pixel output via a high-speed path, the delay of which is much shorter than the pixel clock rate. Real time updates can be performed to any of the gain registers. However, latency associated with the I^{2}C interface should be taken into consideration before changes occur. In most applications, users will be able to assign predefined settings such as daylight, fluorescent, tungsten, and halogen to cover a wide gamut of illumination conditions.

Both DPGA designs use switched capacitors to minimize accumulated offset and improve measurement accuracy and dynamic range. The white balance gain registers are 6-bits and can be programmed to allow gain of 0.695x to 2.74x in varying steps depending on which gain mode is selected (RAW or LIN mode).

The WB Gain Stage (PGA WB) is a two-segment piecewise Linear gain stage. In Raw Mode this stage produces smaller gain steps for the first half of its gain range, and larger gain steps for second half of its gain range. This allows fine adjustment for color ratios as well as a large gain swing.

If the piecewise linear mode is difficult to manage and the fine steps are not required, this gain stage can be placed into Lin1 Mode. In this mode every other gain step is skipped for the first 1/3 of the gain range. This produces the same gain range but with uniform gain steps throughout the range.

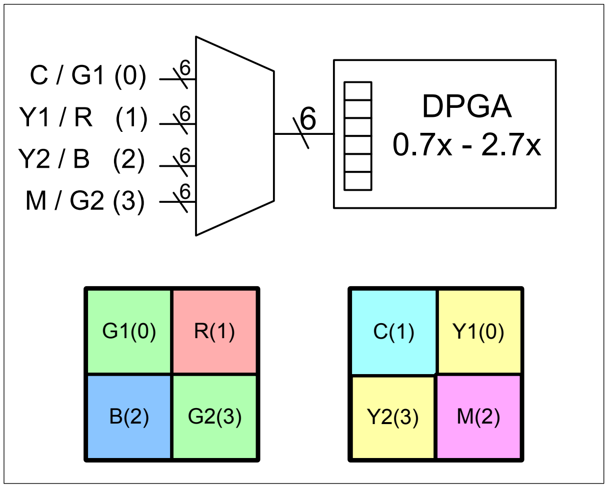


Figure 15: Color Gain Register Selection

3.4.3 Exposure Gain PGA (Exp Gain A/B)

The Exposure (Global) Gain consists of two Gain stages (A and B) in series. Each of these gain stages has a Raw and Lin1 mode as described in the previous WB Gain section. Thus all colors can be amplified by the value in Exp GainA (reg 10_h) and then again by Exp GainB (reg 21_h) to compensate for varying exposure of the scene. The easiest way to implement this is to program Exp GainB at unity and then adjust Exp GainA until it is at its maximum of 2.7395x. Then increase the Exp GainB until the final exposure gain is reached. The gains of the two Exp Gain stages are controlled by Registers 10_h and 21_h, (Table 14 and Table 17 on pages 32 and 35). The Exp Gain Mode is defined in Register 22_h, (Table 18 on page 36).

The dual gain-stage implementation of the Exp Gain may cause difficulty in some auto-exposure routines; this can be avoided by setting the Exp Gain to Lin2 Mode. In Lin2 Mode, Reg 10_h is used to set both gain stages in an attempt to give uniform gain steps across the entire 7.5x range of the two Exp Gain stages. Only one register is used to simplify user programming, and thus the gain step size is increased to ~0.11119 to allow the full range to be accessed by a single 6-bit register. Note that the gain step size is almost but not completely uniform. Any one step may deviate from the mean step size of 0.11119 by a small amount.

3.5 Global Digital Offset Voltage Adjust (GDOVA)

A programmable global offset adjustment is available on the KAC-1310. A user defined offset value is loaded via a 6-bit signed magnitude programming code via the ADC DOVA Register, (Table 19 on page 37).

Offset correction allows fine-tuning of the signal to remove any additional residual error that may have accumulated in the analog signal path. This function is performed directly before analog to digital conversion and allows the user to set the 'black' level in the ADC range.

3.6 Analog to Digital Converter (ADC)

The ADC is a fully differential, low power circuit. A pipe-lined, Redundant Signed Digit (RSD) algorithmic technique is used to yield an ADC with superior characteristics for imaging applications.

Integral Noise Linearity (INL) and Differential Noise Linearity (DNL) performance is specified at ±1.0 and ±0.5, respectively, with no missing codes. The input dynamic range of the ADC is programmed via a Programmable Voltage Reference Generator. The positive reference voltage (VREFP) and negative reference voltages (VREFM) can be programmed from 2.5V to 1.25V and 0V to 1.25V respectively in steps of 5mV via the Reference Voltage Registers (Table 10 and Table 11 on page 29). This feature is used independently or in conjunction with the PGAs to maximize the system dynamic range based on incident illumination. The default input range for the ADC is 1.86V for VREFP and 0.59V for VREFM hence allowing a 10 bit digitization of a 1.3V peak to peak signal.

$$\frac{mV}{10dn} = \frac{2(V^+ - V^-)}{1024} = \frac{2(1.86 - 0.59)}{1024} = 2.48\,\frac{mV}{10dn}$$

If the 20x gain provided by the PGAs is not sufficient, the ADC references can be used to apply additional gain to the ASP. To increase the gain the ADC references need to be moved closer to V_{cm} (1.25V). This should be used only after the PGAs have been used to their fullest since moving the ADC references too far will degrade the ADC performance. The effective gain of the ADC block will be:

$$Gain = \frac{2.48}{\frac{2(V^+ - V^-)}{1024}}$$

Ex. If Reg $0A_h$=Reg $0B_h \equiv BA_h$ then the ADC Gain = 2.

$$Gain = \frac{2.48}{\frac{2(1.57 - 0.93)}{1024}} = 1.98$$

The user should connect 0.1 µF capacitors to CVREFP (pin 15) and CVREFM (pin 14) (see Figure 2) to accurately hold the biases.

4.0 Additional Operational Conditions

The KAC-1310 includes initialization, standby modes, and external reference voltage outputs to afford the user additional application flexibility.

4.1 Initialization (Standby Mode)

The INIT input (pin 42) controls hardware re-initialization of the KAC-1310. This serves to assure controlled chip and system startup. The chip enters standby mode when INIT is asserted via a logic high input. This state must be held a minimum of 1 ms. The chip remains in low-power mode while in the INIT state.

When INIT is removed (logic low), the chip begins initialization. An additional 1 ms "wait period" should be allowed after INIT goes low. This ensures that the start-up routines within the KAC-1310 have run to completion, and that all holding and bypass capacitors, etc. have achieved their required steady-state values. Start-up tasks include resetting registers to their default values, resetting all internal counters and latches, and initializing the analog signal processing chain.

4.2 Standby Mode

The standby mode option is implemented to allow the user to reduce system power consumption during periods that do not require operation of the KAC-1310. This feature allows the user to extend battery life in low power applications.

By utilizing this mode, the user may reduce dynamic power consumption from 400mW (full power, full speed), to <50 mW in the standby mode (note that dynamic power consumption is also reduced in slower conversion speed applications).

The standby mode is activated by applying an active high signal to the INIT pin (#42). The sensor can also be put in the stand by mode via the **sby** bit ("0") on the Power Configuration Register (OC_h) (Table 12, page 30). The registers retain their programmed values and are not reset to default when the power configuration register is used to enter/exit standby mode.

The user may also reduce power consumption by placing the KAC-1310's outputs in the tri-state mode. This action may be accomplished by setting the **dbt** bit on the Power Configuration Register ($0C_h$). In addition, further power savings can be obtained by increasing the external resistance value (see section 4.6).

4.3 Output Tristate

The Tristate Control Register (12_h), (Table 15 on page 33) is used to set the chip outputs into tristate. This functionality is useful if these outputs are on a buss that is being shared by other devices. When the **tsctl** bit is reset (ie "0") the SOF, VCLK, HCLK, and STROBE output pins are placed in tristate mode. The 10 ADC output pins can be tristated by resetting the **tspix** bit ("0").

4.4 Readout Order

Register 57_h (Table 40 on page 49) allows the user to change the direction of readout of the columns or rows. This can be used to compensate for and orientation of the imager in the optical system. The **rrc** when enabled causes the column data to be readout in the reverse direction as compared to the normal readout direction. The **rrr** when enabled causes the row data to be readout in the reverse direction as compared to the normal readout direction. The normal readout direction of the imager is shown in Figure 2 on page 3 (i.e. bottom-to-top; left-to-right).

4.5 Readout Speed

The imager will hold all specifications from 1 MHz to 10 MHz. The nominal maximum speed is 10 MHz (10FPS). The imager will work well beyond this nominal maximum speed. As the speed increases beyond 10 MHz, the power consumption increases slightly, temporal noise rises linearly resulting in a decrease in dynamic range (see Figure 16), and ADC INL degrades. Severe degradation in sensor performance will occur when operating in excess of 20 MHz.

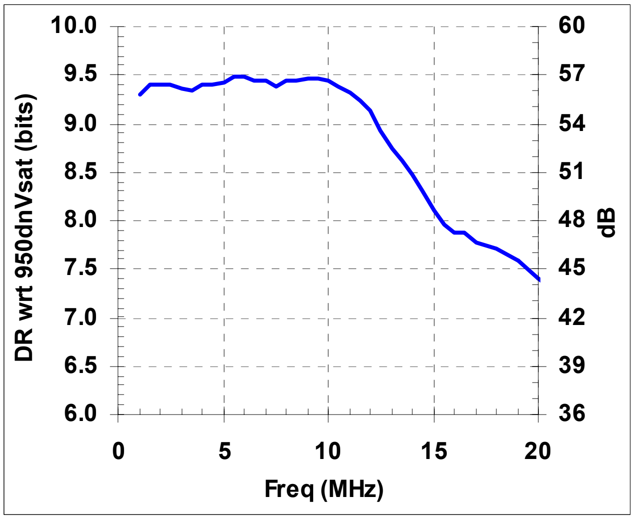


Figure 16: Dynamic Range wrt Mclk Frequency

When operating at speeds greater than 10 MHz, it is possible that horizontal banding might occur. This is due to one of the sample and hold stages not settling. If this condition is observed, it can be rectified by widening the SHA and SHB pulses in registers $5F_h$ (page 49) and 60_h (page 50).

Note: this will change the T_{row} equation given on page 13.

Further image improvements can also be obtained by increasing the power of the chip with the external resistor (see section 4.6).

Note: When increasing the SHA and SHB pulses, the SOF Delay (Register 54_h) will need to be increased as well in order to place the syncs back in the same position relative to the first WOI valid pixel.

4.6 Internal Bias Current Control

The ASP chain has internally generated bias currents that result in an operating power consumption of nearly 400mW. By attaching a resistor between pin 19, EX-TRESA; and pin 20, EXTRESB; the user can reduce the power consumption of the device. This feature is enabled by writing a 1_b to bit **res** of the Power Configuration Register ($0C_h$). Figure 17 depicts the power savings that can be achieved with an external resistor at nominal clock rate (10 MHz). An external resistance (R_{ext}) of 39 kΩ is recommended for optimal sensor performance. Additional power savings can be achieved at lower clock rates.

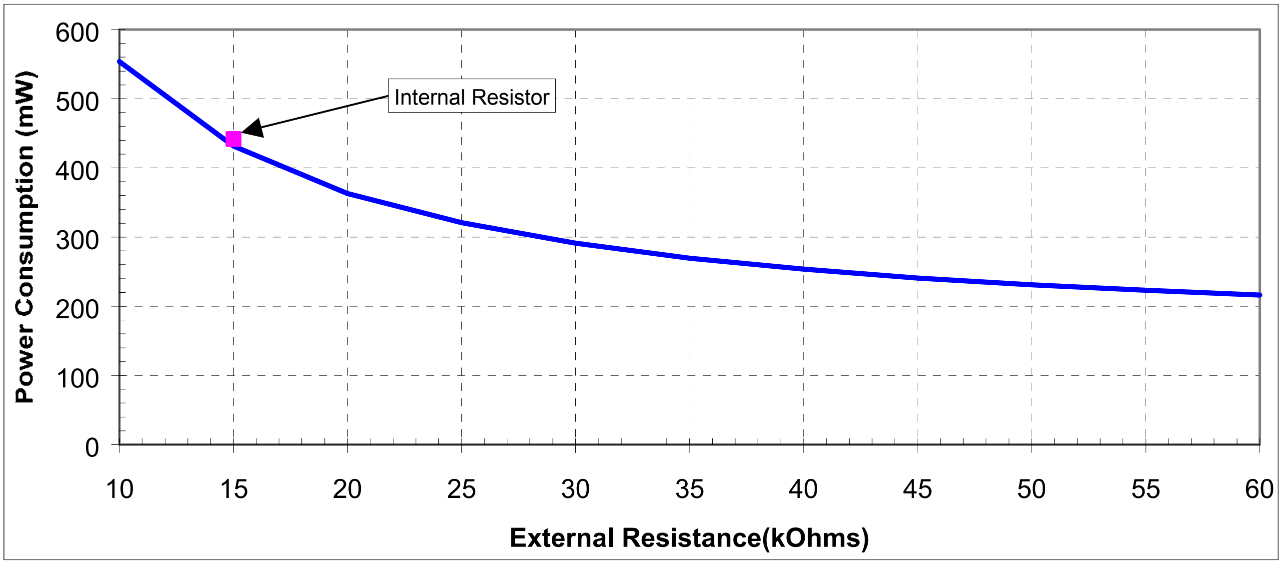


Figure 17: Power Consumption Dependence on External Resistor

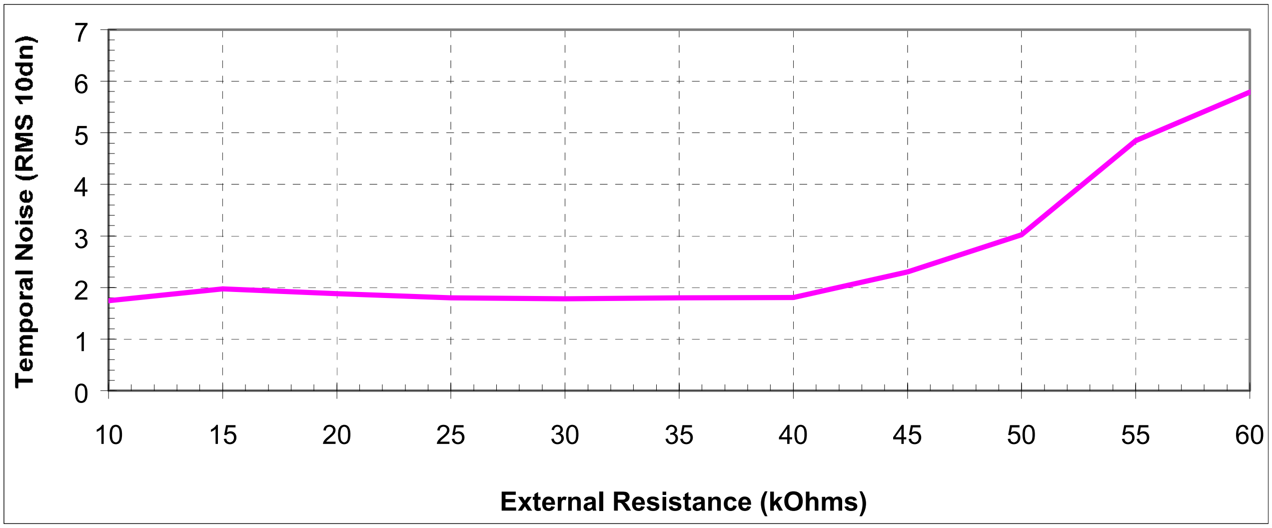


Figure 18: Temporal Noise Dependence on External Resistor

5.0 Waveform Diagrams

The waveforms depicted on the following pages show the output data stream for the KAC-1310 under various operating conditions. The individual SOF, VCLK, and HCLK pulse positions and widths can be moved and inverted using registers 40_h (Table 20, page 38), 54_h (Table 37, page 47), 55_h (Table 38, page 47), 56_h (Table 39, page 48), and 64_h (Table 43, page 50).

5.1 Start of Row Readout (SOF)

This signal triggers the start of the first row readout of the frame. This signal is an output and can be read via Pin #48 of the sensor. The SOF signal delay as well as its length can be set via the SOF Delay Register (Table 37, page 47), and the SOF & VCLK Signal Length Control Register, (Table 39, page 48).

5.2 Horizontal Data Sync (VCLK)

This signal triggers the readout of the sequential rows of the frame. This signal is an output and can be read via Pin #44 of the sensor. The VCLK signal delay in relation to SOF, as well as its length can be set via the VCLK Delay Register (Table 38, page 47), and the SOF&VCLK Signal Length Control Register, (Table 39, page 48)

5.3 Data Valid (HCLK)

This signal triggers a single active pixel data has been readout (example Column 2 of Row 5 data has been read out). This signal is an output and can be read via Pin #45 of the sensor. The HCLK signal delay can be set via the HCLK Delay Register (Table 43, page 50).

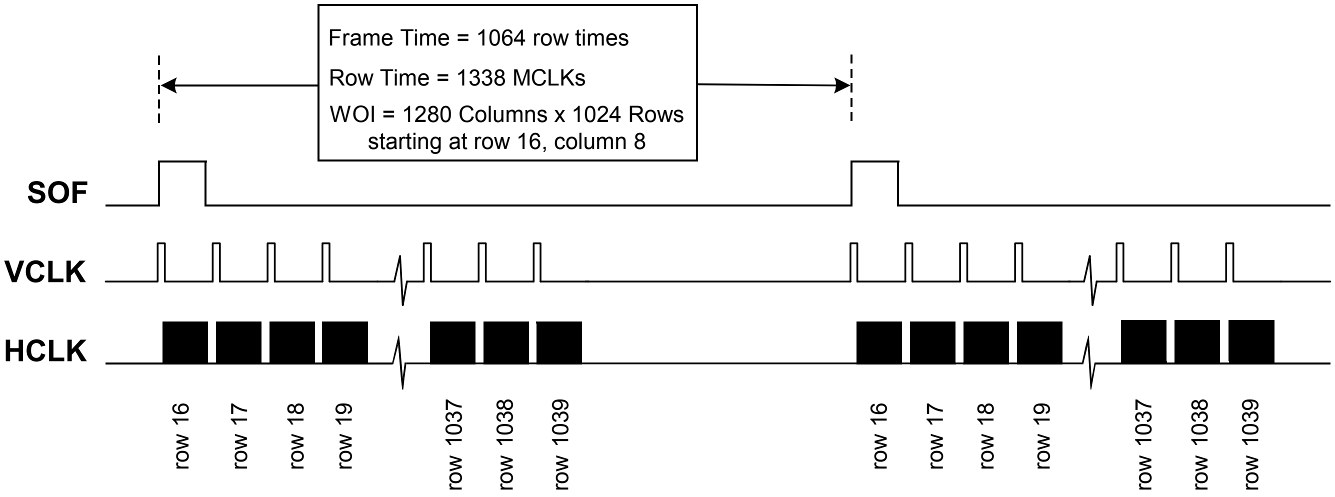


Figure 19: CFRS Default Frame Sync Waveforms

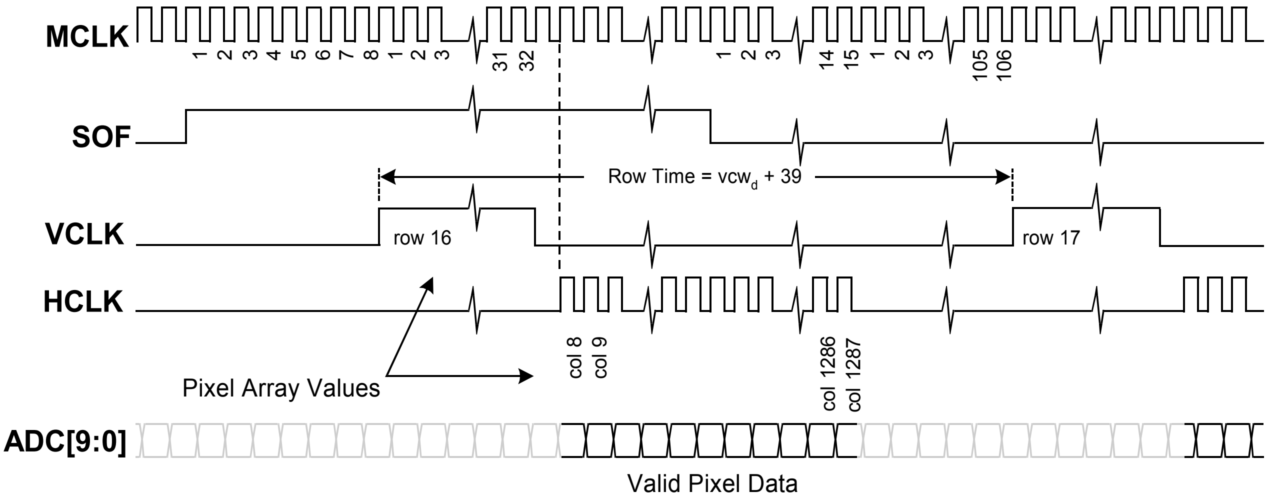


Figure 20: CFRS Default Row Sync Waveforms

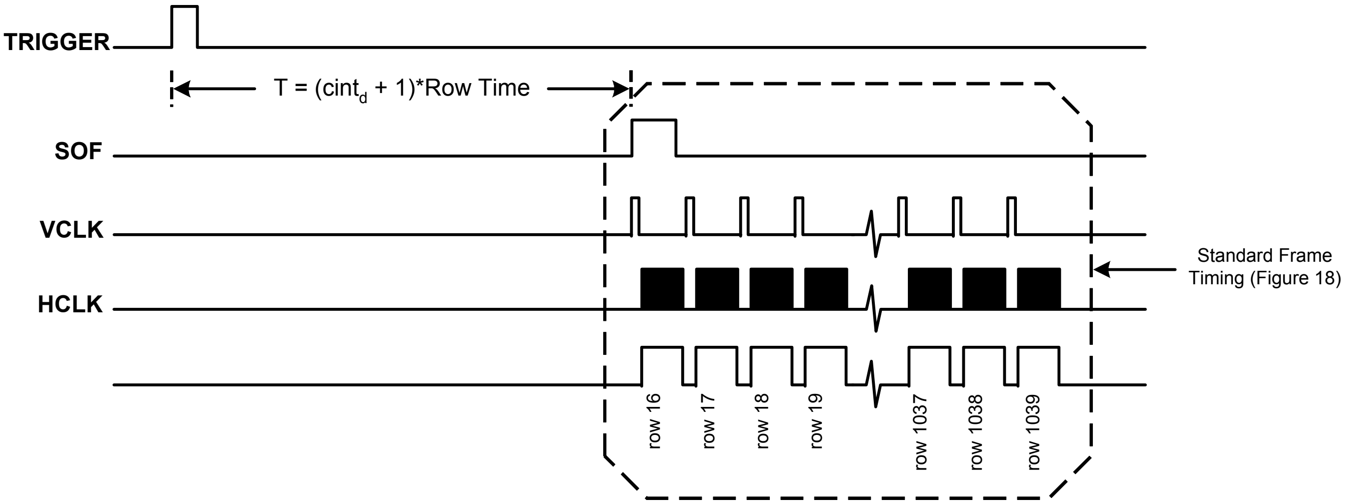


Figure 21: Single Frame Capture Mode (SFRS)

5.4 Strobe Signal

The Strobe signal is an output pin on the KAC-1310 sensor. It can be activated by writing a “1” to **vsg** (bit 5) of the Trigger and Strobe Control Register (Table 22, page 40) while operating in SFRS mode. When activated, the Strobe signal goes high when all rows are integrating simultaneously and ends on row period (T_{row}) before the last row begins to integrate. The start of the strobe signal can also be set by the user. In default mode, when the strobe is activated, the signal fires two row periods before the first row begins to readout and lasts for a length of one T_{row}. A timing diagram for the Strobe signal is shown below in Figure 22.

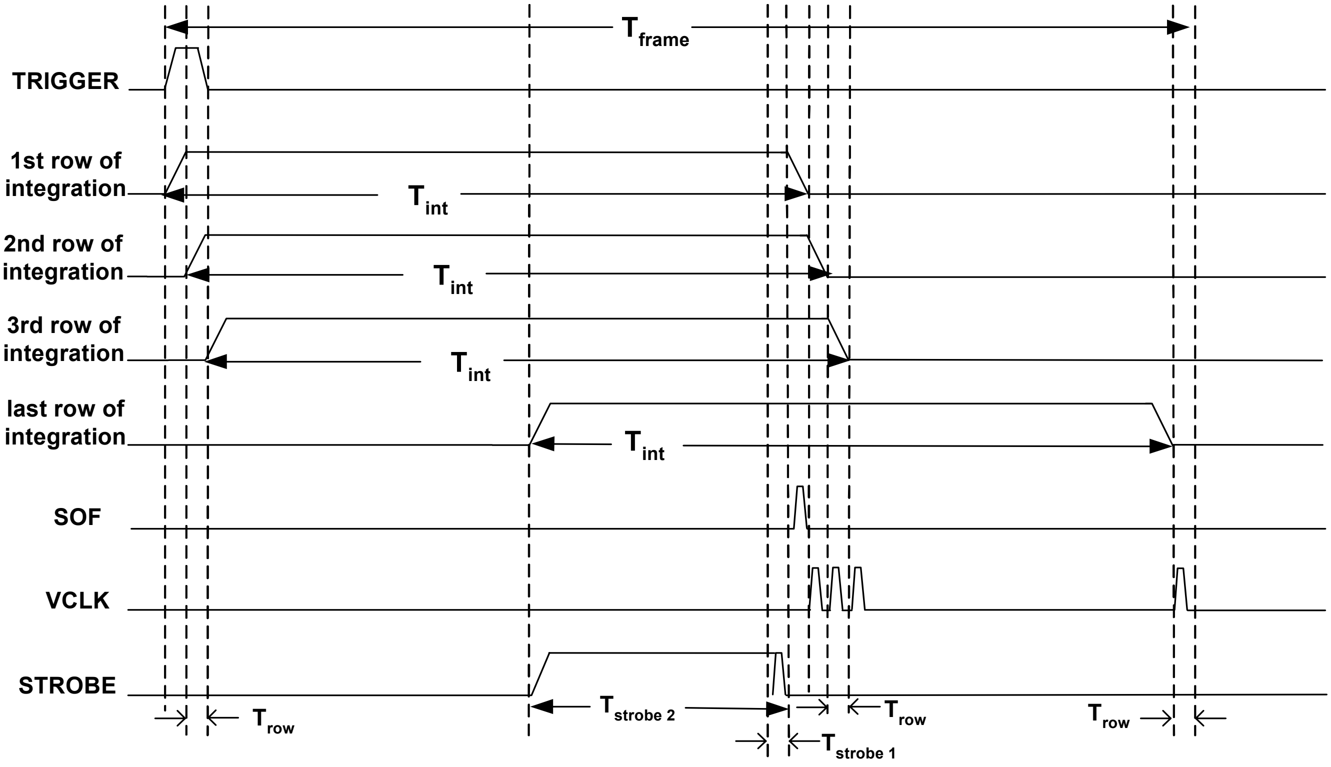


Figure 22: STROBE Output Waveforms

To ensure that the Strobe signal fires, the integration time must be large enough to ensure that all rows are integrating simultaneously for at least 2 row periods (T_{row}) where

Row Time (T_{row}) = ($vcw_d+shA_d+shB_d+19$) * $MCLK_{period}$

To accomplish this , one must ensure that the integration time ($cint_d$) is more than 2 row periods (T_{row}) larger than the active Window of Interest Row depth (wrd_d). Therefore, minimum integration time:

$$T_{intmin} = (cint_{dmin}+1) * T_{row}$$

where $cint_{dmin} = wrd_d + 3$.

$$T_{strobe1} = T_{row}$$
$$T_{strobe2} = T_{intmin} - (wrd_d+1)*T_{row}$$

An example of Strobe related calculations is provided below:

Assumptions:

1) Active Window of Interest = 1280 X 1024
ie. (wcwd) = 1279
(wrdd) = 1023
2) Virtual Column Width (vcwd) = 1290
3) Virtual Row Depth (vrdd)=1034
4) Sample & hold time (shA_d) = 10
5) Sample & hold time (shB_d) = 10
6) MCLK = 10 MHz

Variables: Integration Time ($\mathrm{cint}_{\mathrm{dmin}}$) is the main variable used to control the time of the Strobe signals.

$$\mathbf{T_{intmin} = (cint_{dmin}+1) * T_{row}}$$

Calculations:

$$\begin{aligned} T_{row} &= (vcw_d + 10+10+19) * MCLK_{period} \\ &= (1290 + 39) * 1e\text{-}7 \\ &= 132.9\mu s \end{aligned}$$

$$\begin{aligned} T_{intmin} &= (cint_{dmin} + 1) * T_{row} \\ &= (wrd_d + 3 + 1) * T_{row} = (1023 + 4) * 132.9\mu s \\ &= 136.48 \text{ ms} \end{aligned}$$

$$\begin{aligned} T_{strobe2} &= T_{intmin} - (wrd_d+1)*T_{row} \\ &= 136.48 \text{ ms} - [(1023+1) * 132.9\mu s] \\ &= 390.4 \ \mu s \end{aligned}$$

$$\begin{aligned} T_{Frame} &= T_{int} + T_{rd} \\ &= [(wrd_d) + (cint_d) + 2] * T_{row} \\ &= (1023 + 1026 + 2) * 132.9\mu s \\ &= 272.6 \text{ ms} \end{aligned}$$

Results Summary:

Signal	Value
T_{row}	132.9 μs
T_{intmin}	136.48 ms
$T_{strobe1}$	132.9 μs
$T_{strobe2}$	390.4 μs
T_{Frame}	272.6 ms

6.0 Register List Reference

Note: In each table where a suffix code is used; h = hex, b = binary, and d = decimal.

The I^2C addressing is broken up into groups and assigned to a specific digital block. The designated block is responsible for driving the internal control bus, when the assigned range of addresses is present on the internal address bus. The grouping designation and assigned range are listed in Table 3. Each block contains registers that are loaded and read by the digital and analog blocks to provide configuration control via the I^2C serial interface.

Address Range	Block Name
$00_h - 2F_h$	Analog Register Interface
$40_h - 7F_h$	Sensor Interface
80_h - BF_h	Column Offset Coefficients

Table 3. I^2C Address Range Assignments

Table 4 and Table 5 contain all the I^2C address assignments. The table includes a column indicating whether the register values are shadowed with respect to the sensor interface. If the register is shadowed, the sensor interface will only be updated upon frame boundaries, thereby eliminating intra-frame artifacts resulting from register changes.

Hex Address	Register Function	Default	Ref Table	Shadowed?
00_h	DPGA Color 1 Gain Register (Green1 or Yellow1)	$0E_h$	Table 6, pg 27	Yes
01_h	DPGA Color 2 Gain Register (Red or Magenta)	$0E_h$	Table 7, pg 28	Yes
02_h	DPGA Color 3 Gain Register (Blue or Cyan)	$0E_h$	Table 8, pg 28	Yes
03_h	DPGA Color 4 Gain Register (Green2 or Yellow2)	$0E_h$	Table 9, pg 28	Yes
04_h	*Unused*			
05_h	*Factory Use Only*			
06_h	*Factory Use Only*			
07_h	*Factory Use Only*			
08_h	*Factory Use Only*			
09_h	*Factory Use Only*			
$0A_h$	Negative ADC Reference Register	76_h	Table 10, pg 29	No
$0B_h$	Positive ADC Reference Register	80_h	Table 11, pg 29	No
$0C_h$	Power Configuration Register	00_h	Table 12, pg 30	No
$0D_h$	*Factory Use Only*			
$0E_h$	Reset Control Register	00_h	Table 13, pg 31	No
$0F_h$	Device Identification (read only)	50_h		No
10_h	PGA Exposure (Global) Gain A Register	$0E_h$	Table 14, pg 32	Yes
11_h	*Unused*			
12_h	Tristate Control Register	03_h	Table 15, pg 33	
13_h	*Factory Use Only*			
$14_h \rightarrow 1F_h$	*Unused*			
20_h	Column DOVA DC Register	00_h	Table 16, pg 34	No
21_h	PGA Exposure Global Gain B Register	$0E_h$	Table 17, pg 35	Yes
22_h	PGA Gain Mode Register	00_h	Table 18, pg 36	No
23_h	ADC DOVA Register	00_h	Table 19, pg 37	No
$24_h \rightarrow 3F_h$	*Unused*			

Table 4: I^2C Address Assignments (0_h- $3F_h$)

Hex Address	Register Function	Default	Ref Table	Shadowed?
40_h	Capture Mode Register	$2A_h$	Table 20, pg 38	Yes
41_h	Sub-Sample Control Register	10_h	Table 21, pg 39	Yes
42_h	TRIGGER and Strobe Control Register	02_h	Table 22, pg 40	Yes
$43_h \rightarrow 44_h$	*Unused*			
45_h	WOI Row Pointer MSB Register	00_h	Table 23, pg 41	Yes
46_h	WOI Row Pointer LSB Register	10_h	Table 24, pg 41	Yes
47_h	WOI Row Depth MSB Register	03_h	Table 27, pg 42	Yes
48_h	WOI Row Depth LSB Register	FF_h	Table 28, pg 42	Yes
49_h	WOI Column Pointer MSB Register	00_h	Table 25, pg 41	Yes
$4A_h$	WOI Column Pointer LSB Register	08_h	Table 26, pg 42	Yes
$4B_h$	WOI Column Width MSB Register	04_h	Table 29, pg 43	Yes
$4C_h$	WOI Column Width LSB Register	FF_h	Table 30, pg 43	Yes
$4D_h$	*Unused*			
$4E_h$	Integration Time MSB Register	04_h	Table 31, pg 44	Yes
$4F_h$	Integration Time LSB Register	FF_h	Table 32, pg 44	Yes
50_h	Virtual Frame Row Depth MSB Register	04_h	Table 33, pg 45	Yes
51_h	Virtual Frame Row Depth LSB Register	27_h	Table 34, pg 45	Yes
52_h	Virtual Frame Column Width MSB Register	05_h	Table 35, pg 46	Yes
53_h	Virtual Frame Column Width LSB Register	13_h	Table 36, pg 46	Yes
54_h	SOF Delay Register	$4C_h$	Table 37, pg 47	No
55_h	VCLK Delay Register	02_h	Table 38, pg 47	No
56_h	SOF & VLCK Width Register	$0E_h$	Table 39, pg 48	No
57_h	Readout Direction Control Register	04_h	Table 40, pg 49	No
$58_h \rightarrow 5E_h$	*Unused*			
5Fh	Internal Timing Control Register (SHA)	$0A_h$	Table 41, pg 49	Yes
60_h	Internal Timing Control Register (SHB)	$0A_h$	Table 42, pg 50	Yes
$61_h \rightarrow 63_h$	*Factory Use Only*			
64_h	Clamp Control and HCLK Delay Register	$5C_h$	Table 43, pg 50	Yes
65_h	Encoded Sync Register	00_h	Table 44, pg 51	
66_h	*Unused*			
$67_h \rightarrow 68_h$	*Factory Use Only*			
$69_h \rightarrow 7F_h$	*Unused*			
$80_h \rightarrow BF_h$	Mod64 Col Offset Registers	00_h	Table 45, pg 52	
$C0_h \rightarrow FF_h$	*Unused*			

Table 5: I^{2}C Address Assignments (40_h - FF_h)

7.0 Detailed Register Block Assignments

This section describes in further detail the functional operation of the various KAC-1310 programmable registers.

7.1 Color Gain Registers $00_h \rightarrow 03_h$

The four Color Gain Registers, Color Tile Configuration Register, and four Color Tile Row definitions define how white balance is achieved on the device. Six-bit gain codes can be selected for four separate colors: Table 6, Table 7, Table 8, and Table 9. Gain for each individual color register is programmable given the gain function defined in the table. The user programs these registers to account for changing light conditions to assure a white balanced output. The default value in each register provides for a unity gain for the default Raw Mode. In addition, the default CFA pattern color is listed in the title of each register.

The Gain Mode is set by Register 22_h, Table 18 on page 36.

Raw Gain Mode (WB and Exposure)

Gain $\approx 0.6950 + 0.02175 * \text{Reg}_d$ $\quad 0 \leq \text{Reg}_d \leq 31 \quad (0.0695\text{x} \rightarrow 1.36925\text{x})$

$\approx 1.3475 + 0.04350 * (\text{Reg}_d - 31)$ $\quad 32 \leq \text{Reg}_d \leq 63 \quad (1.3910\text{x} \rightarrow 2.7395\text{x})$

Lin1 Gain Mode (WB and Exposure)

Gain $\approx 0.6950 + 0.04350 * \text{Reg}_d$ $\quad 0 \leq \text{Reg}_d \leq 47 \quad (0.695\text{x} \rightarrow 2.7395\text{x})$

Lin2 Gain Mode (**Exposure gain stage only**)

Gain $\approx 0.483 + 0.11119 * (\text{Reg } 10_h)_d$ $\quad 0 \leq \text{Reg}_d \leq 63 \quad (0.483\text{x} \rightarrow 7.488\text{x})$

<table>
<tr><th>Address
00_h</th><th colspan="6">PGA Color 1 Gain Code
Green1 or Yellow1</th><th>Default
0E_h</th></tr>
<tr><td>7 (msb)</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0 (lsb)</td></tr>
<tr><td>x</td><td>x</td><td>cg1[5]</td><td>cg1[4]</td><td>cg1[3]</td><td>cg1[2]</td><td>cg1[1]</td><td>cg1[0]</td></tr>
<tr><td>Bit Number</td><td>Function</td><td colspan="5">Description</td><td>Reset State</td></tr>
<tr><td>7 - 6</td><td>Unused</td><td colspan="5">Unused</td><td>xx_b</td></tr>
<tr><td>5 - 0</td><td>Gain</td><td colspan="5">See Gain Equation
Default Gain in Raw mode = 1.0
Default Gain in Lin1 Mode = 1.3</td><td>001110_b</td></tr>
</table>

Table 6: PGA Color 1 Gain Register (00_h)

Address 01_h		**PGA Color 2 Gain Code Red or Magenta**					**Default $0E_h$**
7 (msb)	**6**	**5**	**4**	**3**	**2**	**1**	**0 (lsb)**
x	x	cg2[5]	cg2[4]	cg2[3]	cg2[2]	cg2[1]	cg2[0]

Bit Number	**Function**	**Description**	**Reset State**
7 - 6	Unused	Unused	xx_b
5 - 0	Gain	See Gain Equation Default Gain in Raw mode = 1.0 Default Gain in Lin1 Mode = 1.3	001110_b

Table 7: PGA Color 2 Gain Register (01_h)

Address 02_h		**PGA Color 3 Gain Code Blue or Cyan**					**Default $0E_h$**
7 (msb)	**6**	**5**	**4**	**3**	**2**	**1**	**0 (lsb)**
x	x	cg3[5]	cg3[4]	cg3[3]	cg3[2]	cg3[1]	cg3[0]

Bit Number	**Function**	**Description**	**Reset State**
7 - 6	Unused	Unused	xx_b
5 - 0	Gain	See Gain Equation Default Gain in Raw mode = 1.0 Default Gain in Lin1 Mode = 1.3	001110_b

Table 8: PGA Color 3 Gain Register (02_h)

Address 03_h		**PGA Color 4 Gain Code Green2 or Yellow2**					**Default $0E_h$**
7 (msb)	**6**	**5**	**4**	**3**	**2**	**1**	**0 (lsb)**
x	x	cg4[5]	cg4[4]	cg4[3]	cg4[2]	cg4[1]	cg4[0]

Bit Number	**Function**	**Description**	**Reset State**
7 - 6	Unused	Unused	xx_b
5 - 0	Gain	See Gain Equation Default Gain in Raw mode = 1.0 Default Gain in Lin1 Mode = 1.3	001110_b

Table 9: PGA Color 4 Gain Register (03_h)

7.2 Reference Voltage Adjust Registers (0A$_h$, 0B$_h$)

The analog register block allows programming the input voltage range of the analog to digital converter to match the saturation voltage of the pixel array (this effectively sets the *mV/dn* conversion ratio). The voltage reference generator can be programmed via two registers; "positive" ADC reference voltage (**prv**) (2.5V to 1.25V) in Table 11, and "negative" ADC reference voltage (**nrv**) (0 to 1.25V) in Table 10, in 5mV steps. The default settings for **prv** produce a 1.86V positive reference. The default settings for **nrv** produce a 0.59V negative reference. These two references define the ADC analog input range. When adjusting these values, the user should keep the voltage range centered at 1.25V. These ADC references can be adjusted to mV/DN of the ADC. This effectively acts as another gain stage just before the ADC. Excessive adjustment of these values from their default can result in increased power consumption and increased image artifacts. The following equation defines the mV/DN at the input to the ADC:

$$\frac{mV}{10dn} = \frac{2(V^{+} - V^{-})}{1024} = \frac{2(1.86 - 0.59)}{1024} = 2.48\,\frac{mV}{10dn}$$

If the 20x gain provided by the PGAs is not sufficient, the ADC references can be used to apply additional gain to the ASP. To increase the gain the ADC references need to be moved closer to Vcm (1.25V). This should be used only after the PGAs have been used to their fullest since moving the ADC references too far will degrade the ADC performance. The effective gain of the ADC block will be:

$$Gain = \frac{2.48}{\frac{2(V^{+} - V^{-})}{1024}}$$

Address 0A$_h$	"Negative" ADC Reference Voltage						Default 76$_h$
7 (msb)	**6**	**5**	**4**	**3**	**2**	**1**	**0 (lsb)**
nrv[7]	nrv[6]	nrv[5]	nrv[4]	nrv[3]	nrv[2]	nrv[1]	nrv[0]
Bit Number	**Function**	**Description**					**Reset State**
7 - 0	Reference	Voltage = 0.0 + (5mV * nrc$_d$)					01110110$_b$ (0.59V)

Table 10: Negative Voltage Reference Register (0A$_h$)

Address 0B$_h$	"Positive" ADC Reference Voltage						Default 80$_h$
7 (msb)	**6**	**5**	**4**	**3**	**2**	**1**	**0 (lsb)**
prv[7]	prv[6]	prv[5]	prv[4]	prv[3]	prv[2]	prv[1]	prv[0]
Bit Number	**Function**	**Description**					**Reset State**
7 - 0	Reference	Voltage = 2.5 - (5mV * prc$_d$)					10000000$_b$ (1.86V)

Table 11: Positive Voltage Reference Register (0B$_h$)

7.3 Power Configuration Registers (0C$_h$)

The Power Configuration Register controls the internal analog functionality that directly affects power consumption of the device. A pair of external precision resistor pins are available on the KAC-1310 that may be used to more accurately regulate the internal current sources. This serves to minimize variations in power consumption that are caused by variations in internal resistor values as well as offer a method to reduce the power consumption of the device. The default for this control uses the internally provided resistor which is nominally 12.5kΩ. This feature is enabled by setting the **res** bit of the Power Configuration Register and placing a resistor between the EXTRESA and EXTRESB pins. Figure 17 on page 20 depicts the power savings that can be achieved with an external resistor at the nominal clock rate of 10 MHz. Power is further reduced at lower clock rates. Figure 18 shows how the noise of the system is affected by the EXTRES. It is recommended that the External Resistor be kept at 39kΩ at nominal speed. The optimal EXTRES value will change based on system needs and chip frequency.

The KAC-1310 is put into a standby mode via the I^{2}C interface by setting the **sby** bit of the Power Configuration Register. While the imager is in this mode the power consumption is reduced considerably (see Table 50). Also, the I^{2}C continues to work and any number of registers can be programmed. Upon leaving standby state the imager will remember all register settings and apply them to the first imager captured.

Address 0C$_h$			**Power Configuration**				**Default 00$_h$**
7 (msb)	**6**	**5**	**4**	**3**	**2**	**1**	**0 (lsb)**
x	x	x	fuo	res	fuo	fuo	sby

Bit Number	**Function**	**Description**	**Reset State**
7 - 5	Unused	Unused	xxx$_b$
4	FUO	Factory Use Only	0_b
3	Int/Ext Resistor	0_b = Internal Resistor 1_b = External Resistor	0_b
2 - 1	FUO	Factory Use Only	00_b
0	Software Standby	0_b = Soft Standby Inactive 1_b = Soft Standby Active	0_b

Table 12: Power Configuration Register (0C$_h$)

7.4 Reset Control Register ($0E_h$)

Setting the **asr**, **ssr**, **par**, and **sir** bits of this register will reset all the non-user programmable registers to a known reset state. All programmable registers will retain their values. This is useful in situations when control of the KAC-1310 has been lost due to system interrupts and the device needs only be restarted using the earlier user programmed values. Setting the **sit** bit allows the user to completely reset the KAC-1310 to the default state via the serial control interface. All user programmable registers will revert to default values. For each of these reset bits a value of 0 must be sent to register 0Eh after use to take the imager back out of reset mode. Typically only the first two bits are needed. Bit 1 (ssr) resets all state machines and internal registers, but leaves the programmable registers intact. Bit 0 (sit) resets all registers, internal and user programmable to default values.

Address **$0E_h$**				**Reset Control**			**Default** **00_h**
7 (msb)	**6**	**5**	**4**	**3**	**2**	**1**	**0 (lsb)**
x	x	x	asr	par	sir	ssr	sit

Bit Number	**Function**	**Description**	**Reset State**
7 - 5	Unused	Unused	xxx_b
4	ASP(A2D) Reset	0_b = Normal Mode 1_b = Reset registers in the ASP and ADC (state machine reset)	0_b
3	Post ADC Reset	0_b = Normal Mode 1_b = Reset non-programmable POST ADC internal registers to init state	0_b
2	Sensor Interface Reset	0_b = Normal Mode 1_b = Reset non-programmable Sensor Interface registers (state machines) to init state	0_b
1	State Reset	0_b = Normal Mode 1_b = Reset all non-programmable registers to default state	0_b
0	Soft Reset	0_b = Normal Mode 1_b = Reset all registers to default state (all programmed regs>default)	0_b

Table 13: Reset Control Register ($0E_h$)

7.5 Exposure Gain A Register (10_h)

The PGA Exposure (Global) Gain Register allows the user to set one of the global gains via a 6 bit register. This is applied universally to all the pixel outputs. This enables the user to account for varying light conditions. The gain range depends on the Exposure Gain Mode setting (Register 22_h, Table 18 on page 36). In Raw or Lin1 mode both Exposure Gain A (10_h) and Exposure Gain B (21_h) are programmed as successive gains stages. If Lin2 Mode is selected then Register 10_h is used to program both Exposure gain stages as if they were one linear gain stage. Further discussion of the Gain stages can be found section 3.4 on page 15, and section 3.5 on page 17. If register 10_h is increased to its maximum and still more gain is needed, Exposure Gain B can then be increased, via Register 21_h, Table 17 on page 35.

The gain equations of each gain mode are:

Raw Gain Mode (WB and Exposure)

Gain $\approx 0.6950 + 0.02175 * Reg_d$ $\quad 0 \leq Reg_d \leq 31$ $\quad (0.0695x \rightarrow 1.36925x)$

$\approx 1.3475 + 0.04350 * (Reg_d - 31)$ $\quad 32 \leq Reg_d \leq 63$ $\quad (1.3910x \rightarrow 2.7395x)$

Lin1 Gain Mode (WB and Exposure)

Gain $\approx 0.6950 + 0.04350 * Reg_d$ $\quad 0 \leq Reg_d \leq 47$ $\quad (0.695x \rightarrow 2.7395x)$

Lin2 Gain Mode (**Exposure gain stage only**)

Gain $\approx 0.483 + 0.11119 * (Reg\ 10_h)_d$ $\quad 0 \leq Reg_d \leq 63$ $\quad (0.483x \rightarrow 7.488x)$

NOTE: the gain step size of Lin2 Mode is almost, but not completely uniform. Any one step may deviate from the mean step size of 0.11119 by a small amount. This is due to the fact that Lin2 Mode actually varies two gain stages with fixed step sizes to make one equivalent gain step.

Address 10_h			**Global Gain A**				**Default $0E_h$**
7 (msb)	**6**	**5**	**4**	**3**	**2**	**1**	**0 (lsb)**
x	x	gg1[5]	gg1[4]	gg1[3]	gg1[2]	gg1[1]	gg1[0]

Bit Number	**Function**	**Description**	**Reset State**
7 - 6	Unused	Unused	xx_b
5 - 0	Gain	Gain equation depends on Gain Mode: Raw, Lin1, or Lin2 (Default is unity gain for Raw mode)	001110_b

Table 14: PGA Exposure Gain A Register (10_h)

7.6 Tristate Control Register (12_h)

The Tristate Control Register is used to set the chip outputs into tristate. This functionality is useful if these outputs are on a bus that is being shared by other devices. When the **tsctl** bit is reset (ie “0”) the SOF, VCLK, HCLK, and STROBE output pins are placed in tristate mode. The 10 ADC output pins can be tristated by resetting the **tspix** bit (“0”).

Address 12_h			**Tristate Control**				**Default 03_h**
7 (msb)	**6**	**5**	**4**	**3**	**2**	**1**	**0 (lsb)**
FUO	FUO	FUO	FUO	FUO	FUO	tsctl	tspix

Bit Number	**Function**	**Description**	**Reset State**
7 - 2	FUO	Factory Use Only	000000_b
1	Sync Tristate	0_b = HCLK, SOF, VCLK, and Strobe sync pins tristated 1_b = Sync pins driven	1_b
0	ADC Tristate	0_b = ADC outputs pins tristated 1_b = ADC output pins driven	1_b

Table 15: Tristate Control Register (12_h)

7.7 Column DOVA DC Register (20_h)

Offset adjustments for the KAC-1310 are done in separate sections of the ASP to facilitate FPN removal and final image black level set. The primary purpose of the Column DOVA DC Register is to compensate for pre-gain offset. If this register is set to zero the user may find that the dark level of some chips may move with different programmed gain values. In addition the white balance gain stage can result in different effective dark levels for different colors. These effects MAY cause distortion with certain post image signal processing. In these cases the Column DOVA DC Register can be programmed such that the dark pixel level is independent of programmed gain values. The simplest method for setting this register is to place the imager in the dark and record the mean value for the dark pixels. Then increase the global gain register (10_h) to the maximum gain to be used in the application. Adjust register 20_h until the dark level has returned to the level previously recorded with unity gain. This process can be repeated again for greater accuracy since the dark level at unity gain will now have shifted slightly. For many applications, this register can be left in its default state of 00_h. If during the calibration of this register the value of any pixels are observed to be clipping at zero counts, it is then necessary to temporarily increase the ADC DOVA (reg 23_h) to avoid clipping. Register 20_h should not be used to adjust the code value of the dark level for the ADC, this should always be done with the ADC DOVA (reg 23_h)

The Column DOVA stage is also used to correct for patterned column noise. This is done pre-gain. The column pattern correction offsets are defined in Reg 80_h→ BF_h, see Table 45 on page 52. The Column DOVA stage has only six bits of programmability. Registers 20_h is added to the value in 80_h→ BF_h for that column. The final sum is clipped to ±32_d.

Address 20_h	**Column DOVA DC**						**Default 00_h**
7 (msb)	**6**	**5**	**4**	**3**	**2**	**1**	**0 (lsb)**
x	x	cdd[5]	cdd[4]	cdd[3]	cdd[2]	cdd[1]	cdd[0]

Bit Number	**Function**	**Description**	**Reset State**
7 - 6	Unused	Unused	xx_b
5	Sign	0_b = Positive Offset 1_b = Negative Offset	0_b
4 - 0	Column DC Offset	Offset = 2.6 * cdd_d (64 steps @ 2.6 mV/step)	00000_b

Table 16: Column DOVA DC Offset (20_h)

7.8 Exposure GainB (21_h)

The PGA Exposure (Global) Gain Register allows the user to set one of the global gains via a 6 bit register. This is applied universally to all the pixel outputs. This enables the user to account for varying light conditions. The gain range depends on the Exposure Gain Mode setting (Register 22_h, Table 18 on page 36). In Raw or Lin1 mode both Exposure Gain A(10_h) and Exposure Gain B(21_h) are programmed as successive gains stages. If Lin2 Mode is selected then Register 10_h is used to program both Exposure gain stages as if they were one linear gain stage. Further discussion of the Gain stages can be found in section 3.4 on page 15, and section 3.5 on page 17.

The gain equations of each gain mode are:

Raw Gain Mode (WB and Exposure)

Gain $\approx 0.6950 + 0.02175 * Reg_d$ $\quad 0 \le Reg_d \le 31$ $\quad (0.0695x \rightarrow 1.36925x)$
$\approx 1.3475 + 0.04350 * (Reg_d - 31)$ $\quad 32 \le Reg_d \le 63$ $\quad (1.3910x \rightarrow 2.7395x)$

Lin1 Gain Mode (WB and Exposure)

Gain $\approx 0.6950 + 0.04350 * Reg_d$ $\quad 0 \le Reg_d \le 47$ $\quad (0.695x \rightarrow 2.7395x)$

Lin2 Gain Mode

This register is not used in this mode. See Exposure Gain A, Table 14 on page 32 for programming this mode.

Address 21_h	**Exposure Gain B**						**Default $0E_h$**
7 (msb)	**6**	**5**	**4**	**3**	**2**	**1**	**0 (lsb)**
x	x	gg2[5]	gg2[4]	gg2[3]	gg2[2]	gg2[1]	gg2[0]
Bit Number	**Function**	**Description**					**Reset State**
7 - 6	Unused	Unused					xx_b
5 - 0	Gain	Gain equation depends on Gain Mode: Raw, Lin1, or Lin2 (Default is unity gain for Raw mode)					001110_b

Table 17: Exposure Gain B (21_h)

7.9 PGA Gain Mode (22_h)

There exist three different gain modes that are available when the sensor is performing White Balance and Exposure gain. Plots of the three gain modes are illustrated in Figure 14 on page 16. The three gain modes are:

Raw Gain Mode (WB and Exposure)

Gain	$\approx 0.6950 + 0.02175 * \text{Reg}_d$	$0 \le \text{Reg}_d \le 31$	(0.0695x → 1.36925x)
	$\approx 1.3475 + 0.04350 * (\text{Reg}_d - 31)$	$32 \le \text{Reg}_d \le 63$	(1.3910x → 2.7395x)

Lin1 Gain Mode (WB and Exposure)

Gain	$\approx 0.6950 + 0.04350 * \text{Reg}_d$	$0 \le \text{Reg}_d \le 47$	(0.695x → 2.7395x)

Lin2 Gain Mode (**Exposure gain stage only**)

Gain	$\approx 0.483 + 0.11119 * (\text{Reg } 10_h)_d$	$0 \le \text{Reg}_d \le 63$	(0.483x → 7.488x)

NOTE: the gain step size of Lin2 Mode is almost, but not completely uniform. Any one step may deviate from the mean step size of 0.11119 by a small amount. This is due to the fact that Lin2 Mode actually varies two gain stages with fixed step sizes to make one equivalent gain step.

The **wbm** bit sets the gain mode for the WB gain (Register 0_h-3_h, pages 27 and 28).
The **egm** bits set the gain mode for the Exposure Gains Registers (10_h page 32 and 21_h page 35.

Address 22_h			PGA Gain Mode				Default 00_h
7 (msb)	6	5	4	3	2	1	0 (lsb)
x	x	x	x	x	wbm	egm[1]	egm[0]

Bit Number	Function	Description	Reset State
7 - 3	Unused	Unused	xxxxx_b
2	WB Gain Mode	0_b = Raw Gain Mode 1_b = Lin1 Gain Mode	0_b
1 - 0	Exposure Gain Mode	00_b = Raw Gain Mode 01_b = Lin1 Gain Mode 1x_b = Lin2 Gain Mode	00_b

Table 18: PGA Gain Mode (22_h)

7.10 ADC DOVA (23_h)

The Global DOVA Register performs a final offset adjustment in analog space just prior to the ADC. The 6-bit register uses its MSB to indicate positive or negative offset. Each register value changes the offset by 4 LSB code levels hence giving an offset range of ±124 dn. As an example, to program an offset of +92 dn, the value of 010111_b (23_d, 17_h) should be loaded. This offset is used to place the dark level within the ADC range.

Address 23_h			**ADC DOVA**				**Default 00_h**
7 (msb)	**6**	**5**	**4**	**3**	**2**	**1**	**0 (lsb)**
x	x	gd[5]	gd[4]	gd[3]	gd[2]	gd[1]	gd[0]

Bit Number	**Function**	**Description**	**Reset State**
7 - 6	Unused	Unused	xx_b
5	Sign	0_b = Positive Offset 1_b = Negative Offset	0_b
4 - 0	Column DC Offset	Offset (mV) = 12 * gd_d (64 steps @ 12 mV/step)	00000_b

Table 19: ADC DOVA Register (23_h)

7.11 Capture Mode Control (40_h)

The Capture Mode Control Register defines how the data is captured and how the data is to be provided at the output. Setting the **cms** bit will stop the current CFRS output data stream at the end of the current frame and place the imager in Single Frame Capture Mode (SFRS). While the **cms** bit is set (SFRS), the output of frames can be paused with the TRIGGER input pin. When the TRIGGER pin is low (V_{SS}) the output of frames is suspended. When the TRIGGER pin is high (V_{DD}) frames are continuous. The default for **cms** is 0 (CFRS). In CFRS the frames are continuously output and the TRIGGER pin is ignored. The Frame Rate is slightly reduced when the **cms** is set (SFRS) because care is taken in the startup such that the first frame output is valid. This causes a slight delay at the start of each frame. See Figure 21 on page 22 for a timing diagram for SFRS mode. With the **cms** low(=0), the Frame Rate is faster, but the first frame will be invalid (wrong integration time).

When the **hm** bit is set, the HCLK sync is high whenever valid WOI pixel data is being clocked out and low during the other blanking intervals. The HCLK does NOT toggle at the MCLK rate when the **hm** bit is set. When **hm** is set the HCLK will go high once at the beginning of the valid pixel data and remain high until the last WOI pixel has been clocked out. When the **hm** bit is set the **he** bit is ignored. The **sp** bit is used to define whether SOF is active high or low. SOF is active high by default. The **ve** bit is used to determine whether VCLK is output at the beginning of the virtual frame rows or only for the WOI rows. The **ve** bit defaults to VCLK on WOI rows only. The **vp** bit is used to define whether VCLK is active high(the default) or active low. The **he** bit is used to determine whether HCLK is output continuously (needed for some frame grabbers) or only for pixels within the WOI (default). The **hp** bit is used to define whether HCLK is active high (default) or low.

Address 40_h			**Capture Mode Control**				**Default $2A_h$**
7 (msb)	**6**	**5**	**4**	**3**	**2**	**1**	**0 (lsb)**
FUO	cms	sp	ve	vp	he	hp	hm

Bit Number	**Function**	**Description**	**Reset State**
7	FUO	Factory Use Only	0_b
6	RSCM Mode	0_b = Continuous Frame Rolling Shutter (CFRS) 1_b = Single Frame Rolling Shutter (SFRS)	0_b
5	SOF Phase	0_b = SOF sync active low 1_b = SOF sync active high	1_b
4	VCLK Enable	0_b = VCLK Sync on WOI rows only 1_b = VCLK Sync on WOI and Virtual Rows	0_b
3	VCLK Phase	0_b = Active low 1_b = Active high	1_b
2	HCLK Enable	0_b = Pixel sync on WOI pixels only 1_b = Continuous pixel sync	0_b
1	HCLK Phase	0_b = Active low 1_b = Active high	1_b
0	HCLK Mode	0_b = Toggles - Toggles at MCLK rates defined by (he) bit 1_b = Continuous - Pixel Valid Envelope	0_b

Table 20: Capture Mode Register (40_h)

7.12 Sub-sample Control (41_h)

The sub-sample Control Register is used to define what pixels of the WOI are read and the method they are output. See section 2.3.4 on page 11 for details on the readout modes. Sub-sampled frames readout faster than the full frame image. Any pixel not selected in the sub-sample mode is ignored, thereby not slowing the Frame Rate.

Bit **cm** can be cleared for monochrome imagers. This allows the imager to skip single columns and rows improving uniformity of sub-sampled MTF. In color mode sub-sampling is done in column and row pairs to conserve color integrity. The degree of sub-sample is defined by **rf** [1:0] for the rows, while the column sub-sample is independently defined by **cf** [1:0]. Row binning (even/odd row summing) is activated with the **bn** bit.

Address 41_h			**Capture Mode Control**				**Default 10_h**
7 (msb)	**6**	**5**	**4**	**3**	**2**	**1**	**0 (lsb)**
x	FUO	bn	cm	rf[1]	rf[0]	cf[1]	cf[0]

Bit Number	**Function**	**Description**	**Reset State**
7	Unused	Unused	x_b
6	FUO	Factory Use Only	0_b
5	Binning	0_b = Full WOI readout 1_b = Even/Odd Row Summing	0_b
4	Color Mode	0_b = Monochrome Pattern Sampling (kernel=1) 1_b = Bayer Pattern Sampling (kernel=2)	1_b
3 - 2	Row Sub-Sampling Mode	00_b = Full WOI readout 01_b = Read one kernel, skip one (1/2 sampled) 10_b = Read one kernel, skip three (1/4 sampled) 11_b = Read one kernel, skip seven (1/8 sampled)	00_b
1 - 0	Column Sub-Sampling Mode	00_b = Full WOI readout 01_b = Read one kernel, skip one (1/2 sampled) 10_b = Read one kernel, skip three (1/4 sampled) 11_b = Read one kernel, skip seven (1/8 sampled)	00_b

Table 21: Sub-Sample Control Register (41_h)

7.13 TRIGGER and STROBE Control Register (42_h)

The **saw** bit allows the user to select how long the STROBE signal is going to be on. If the bit is set to 1, the STROBE output will go high when all lines are concurrently integrating and will go low when the integration time has completed and readout has begun. It is during this period while STROBE is high that a mechanical shutter must open and close and/or flash must fire and quench if these devices are being used with the imager. If the shutter or flash operate at any other time image artifacts can result. Note the integration time must be greater than a frame readout time for this output to be useful. The **sae** bit when enabled will enable the STROBE signal to be generated automatically by the sensor. This will only work in Single Frame Rolling Shutter (SFRS) mode.

The **se** bit, when enabled, will allow for an external signal to drive the trigger signal via the TRIGGER pin on the chip. Enabling the **sa** bit forces the trigger signal high until this bit is disabled. This causes continuous frame processing in SFRS mode. The **sr** bit, when enabled, causes the TRIGGER signal to go high for exactly one clock cycle, and then returns to a low. It remains low until the **sr** bit is enabled again. This is used to trigger a single frame capture via I^2C rather than the TRIGGER pin.

Address 42_h			**TRIGGER and STROBE Control**				**Default 02_h**
7 (msb)	**6**	**5**	**4**	**3**	**2**	**1**	**0 (lsb)**
x	x	sso	saw	sae	se	sa	sr

Bit Number	**Function**	**Description**	**Reset State**
7 - 6	Unused	Unused	xx_b
5		*Factory Use Only*	0_b
4	Strobe Width	0_b = 1 line time 1_b = Pulse width is high while all rows are silultaneously integrating	0_b
3	STROBE Enable	0_b = STROBE pin Disabled 1_b = STROBE pin Enabled	0_b
2	TRIGGER Enable	0_b = External TRIGGER input pin Disabled (ignored) 1_b = External TRIGGER input pin Enabled	0_b
1	TRIGGER Always On	0_b = No effect 1_b = TRIGGER input is internally held HIGH, TRIGGER input pin is ignored	1_b
0	Software TRIGGER	0_b = No effect 1_b = Triggers a single frame capture via I^2C	0_b

Table 22: TRIGGER and STROBE Control Register (42_h)

7.14 Programmable Window of Interest (WOI) (45_h-$4C_h$)

The WOI is defined by a set of registers that indicate the upper-left starting point for the window and another set of registers that define the size of the window. Refer to Figure 9 on page 11 for a pictorial representation of the WOI within the active pixel array. The WOI Row Pointer, **wrp**[8:0], and the WOI Column Pointer, **wcp**[9:0], mark the upper-left starting point for the WOI. The WOI Row Depth, **wrd**[9:0] and the WOI Column Depth, **wcw**[10:0] indicate the size of the WOI. The user must be careful to create a WOI that is completely confined within the Virtual Frame. There is no logic in the sensor interface to prevent the user from defining a WOI that addresses nonexistent pixels.

Address 45_h			**WOI Row Pointer MSB**				**Default** 00_h
7 (msb)	**6**	**5**	**4**	**3**	**2**	**1**	**0 (lsb)**
x	x	x	x	x	wrp[10]	wrp[9]	wrp[8]

Bit Number	**Function**	**Description**	**Reset State**
7 - 3	Unused	Unused	xxxxx$_b$
2 - 0	WOI Row Pointer	In conjunction with the WOI Row Pointer LSB Register, forms the 11-bit WOI Row Pointer wrp[10:0]	000$_b$

Table 23: WOI Row Pointer MSB Register (45_h)

Address 46_h			**WOI Row Pointer LSB**				**Default** 10_h
7 (msb)	**6**	**5**	**4**	**3**	**2**	**1**	**0 (lsb)**
wrp[7]	wrp[6]	wrp[5]	wrp[4]	wrp[3]	wrp[2]	wrp[1]	wrp[0]

Bit Number	**Function**	**Description**	**Reset State**
7 - 0	WOI Row Pointer	In conjunction with the WOI Row Pointer MSB Register, forms the 11-bit WOI Row Pointer wrp[10:0]	00010000$_b$ (16_d)

Table 24: WOI Row Pointer LSB Register (46_h)

Address 49_h			**WOI Column Pointer MSB**				**Default** 00_h
7 (msb)	**6**	**5**	**4**	**3**	**2**	**1**	**0 (lsb)**
x	x	x	x	x	wcp[10]	wcp[9]	wcp[8]

Bit Number	**Function**	**Description**	**Reset State**
7 - 3	Unused	Unused	xxxxx$_b$
2 - 0	WOI Column Pointer	In conjunction with the WOI Column Pointer LSB Register, forms the 11-bit WOI Column Pointer wcp[10:0]	000$_b$

Table 25: WOI Column Pointer MSB Register (49_h)

Address **$4A_h$**	**WOI Column Pointer LSB**						**Default** **08_h**
7 (msb)	**6**	**5**	**4**	**3**	**2**	**1**	**0 (lsb)**
wcp[7]	wcp[6]	wcp[5]	wcp[4]	wcp[3]	wcp[2]	wcp[1]	wcp[0]
Bit Number	**Function**	**Description**					**Reset State**
7 - 0	WOI Column Pointer	In conjunction with the WOI Column Pointer MSB Register, forms the 11-bit WOI Column Pointer wcp[10:0]					00001000_b (8_d)

Table 26: WOI Column Pointer LSB Register ($4A_h$)

Address **47_h**	**WOI Row Depth MSB**						**Default** **03_h**
7 (msb)	**6**	**5**	**4**	**3**	**2**	**1**	**0 (lsb)**
x	x	x	x	x	wrd[10]	wrd[9]	wrd[8]
Bit Number	**Function**	**Description**					**Reset State**
7 - 3	Unused	Unused					$xxxxx_b$
2 - 0	WOI Row Depth	In conjunction with the WOI Row Depth LSB Register, forms the 11-bit WOI Row Depth wrd[10:0]					011_b

Table 27: WOI Row Depth MSB Register (47_h)

Address **48_h**	**WOI Row Depth LSB**						**Default** **FF_h**
7 (msb)	**6**	**5**	**4**	**3**	**2**	**1**	**0 (lsb)**
wrd[7]	wrd[6]	wrd[5]	wrd[4]	wrd[3]	wrd[2]	wrd[1]	wrd[0]
Bit Number	**Function**	**Description**					**Reset State**
7 - 0	WOI Row Depth	In conjunction with the WOI Row Depth MSB Register, forms the 11-bit WOI Row Depth wrd[10:0] Desired = wrd_d+1					11111111_b 1024 Rows

Table 28: WOI Row Depth LSB Register (48_h)

Address $4B_h$			**WOI Column Width MSB**				**Default 04_h**
7 (msb)	**6**	**5**	**4**	**3**	**2**	**1**	**0 (lsb)**
x	x	x	x	x	wcw[10]	wcw[9]	wcw[8]

Bit Number	**Function**	**Description**	**Reset State**
7 - 3	Unused	Unused	$xxxxxx_b$
2 - 0	WOI Column Width	In conjunction with the WOI Column Width LSB Register, forms the 11-bit WOI Column Width wcw[10:0]	100_b

Table 29: WOI Column Width MSB Register ($4B_h$)

Address $4C_h$			**WOI Column Width LSB**				**Default FF_h**
7 (msb)	**6**	**5**	**4**	**3**	**2**	**1**	**0 (lsb)**
wcw[7]	wcw[6]	wcw[5]	wcw[4]	wcw[3]	wcw[2]	wcw[1]	wcw[0]

Bit Number	**Function**	**Description**	**Reset State**
7 - 0	WOI Column Width	In conjunction with the WOI Column Width MSB Register, forms the 11-bit WOI Column Width wcw[10:0] Desired = $wcw_d + 1$	11111111_b 1280 Columns

Table 30: WOI Column Width LSB Register ($4C_h$)

7.15 Integration Time Control ($4E_h$ → $4F_h$)

The integration Time registers control the integration time for the pixel array. Integration time is measured in Virtual Row times. Refer to Figure 11 on page 12 for a pictorial description of the Virtual Frame and its relationship to the WOI Frame. A Virtual Frame is the mechanism by which the user controls the integration time and frame time for the output data stream. By adding additional rows or columns as 'blanking' to the WOI to form the Virtual Frame, the user can control the amount of blanking in both horizontal and vertical space.

NOTE: The **upd bit** of Reg $4E_h$ is used to indicate a change to **cint**[13:0]. Since multiple I^2C writes may be needed to complete desired frame to frame integration time changes, the **upd** bit signals that all desired programming has been completed, and to apply these changes to the next frame captured. This prevents undesirable changes in integration time that may result from I^2C writes that span the "End of Frame" boundary. This **upd** bit has to be toggled from its previous state in order for the new value of **cint**[13:0] to be accepted/updated by the sensor and take effect. i.e. If its previous state is "0", when writing a new **cint** value, first write cint[7:0] to register $4F_h$, then write both **cint** [13:8] and "1" to the **upd** bit to register $4E_h$.

Integration Time = $(cint_d + 1) * (vcw_d + shA_d + shB_d + 2) * MCLK_{period}$

where vcw_d is defined in registers 52_h and 53_h, Table 35 and Table 36 on page 46.

Address $4E_h$			**Integration Time MSB**				**Default 04_h**
7 (msb)	**6**	**5**	**4**	**3**	**2**	**1**	**0 (lsb)**
x	upd	cint[13]	cint[12]	cint[11]	cint[10]	cint[97]	cint[8]

Bit Number	**Function**	**Description**	**Reset State**
7	Unused	Unused	x_b
6	Update	This bit must be toggled from its previous state to apply cint to the integration time counter.	0_b
5 - 0	Integration Time	In conjuction with the Integration Time LSB Register, forms the 14-bit Integration Time cint[13:0].	000100_b

Table 31: Integration Time MSB Register ($4E_h$)

Address $4F_h$			**Integration Time LSB**				**Default FF_h**
7 (msb)	**6**	**5**	**4**	**3**	**2**	**1**	**0 (lsb)**
cint[7]	cint[6]	cint[5]	cint[4]	cint[3]	cint[2]	cint[1]	cint[0]

Bit Number	**Function**	**Description**	**Reset State**
7 - 0	Integration Time	In conjuction with the Integration Time MSB Register, forms the 14-bit Integration Time cint[13:0]. Integration Time = (cintd +1) * Trow	11111111_b 1280 Rows

Table 32: Integration Time LSB Register ($4F_h$)

7.16 Programmable Virtual Frame (50_h → 53_h)

A Virtual Frame is the mechanism by which the user controls the integration time and frame time for the output data stream. By adding additional rows or columns as ‘blanking’ to the WOI to form the Virtual Frame, the user can control the amount of blanking in both horizontal and vertical space. Both the Virtual Frame Row Depth, **vrd**[13:0], and the Virtual Frame Column Width, **vcw**[13:0], have a range of 0_d to 16384_d. The Virtual Frame defines the maximum integration time. If the integration register is programmed with more rows than are in the Virtual Frame then the integration time will be clipped to the number of rows in the virtual frame.

The user should be careful to create a Virtual Frame that is larger than the WOI. There is no logic in the sensor interface to prevent the user from defining a Virtual Frame smaller than the WOI. Therefore, pixel data may be lost. The Virtual Frame must be at least 1 row and 6 columns larger than the WOI.

Address 50_h			**Virtual Frame Row Depth MSB**				**Default 04_h**
7 (msb)	**6**	**5**	**4**	**3**	**2**	**1**	**0 (lsb)**
x	x	vrd[13]	vrd[12]	vrd[11]	vrd[10]	vrd[9]	vrd[8]

Bit Number	**Function**	**Description**	**Reset State**
7 - 6	Unused	Unused	xx_b
5 - 0	Virtual Row Depth	In conjunction with the Virtual Frame Row Depth LSB Register, forms the 14-bit Virtual Fram Row Depth vrd[13:0].	000100_b

Table 33: Virtual Frame Row Depth MSB (50_h)

Address 51_h			**Virtual Frame Row Depth LSB**				**Default 27_h**
7 (msb)	**6**	**5**	**4**	**3**	**2**	**1**	**0 (lsb)**
vrd[7]	vrd[6]	vrd[5]	vrd[4]	vrd[3]	vrd[2]	vrd[1]	vrd[0]

Bit Number	**Function**	**Description**	**Reset State**
7 - 0	Virtual Row Depth	In conjunction with the Virtual Frame Row Depth MSB Register, forms the 14-bit Virtual Fram Row Depth vrd[13:0]. WOI is always top-left justified in Virtual Frame. vrd_d minimim = wrd_d +1	00100111_b 1064 Rows

Table 34: Virtual Frame Row Depth LSB (51_h)

Address 52$_h$		Virtual Frame Column Width MSB					Default 05$_h$
7 (msb)	**6**	**5**	**4**	**3**	**2**	**1**	**0 (lsb)**
x	x	vcw[13]	vcw[12]	vcw[11]	vcw[10]	vcw[9]	vcw[8]

Bit Number	Function	Description	Reset State
7 - 6	Unused	Unused	xx$_b$
5 - 0	Virtual Column Width	In conjunction with the Virtual Frame Column Width LSB Register, forms the 14-bit Virtual Frame Column Width vcw[13:0].	000101$_b$

Table 35: Virtual Frame Column Width MSB (52$_h$)

Address 53$_h$		Virtual Frame Column Width LSB					Default 13$_h$
7 (msb)	**6**	**5**	**4**	**3**	**2**	**1**	**0 (lsb)**
vcw[7]	vcw[6]	vcw[5]	vcw[4]	vcw[3]	vcw[2]	vcw[1]	vcw[0]

Bit Number	Function	Description	Reset State
7 - 0	Virtual Column Width	In conjunction with the Virtual Frame Column Width MSB Register, forms the 14-bit Virtual Frame Column Width vcw[13:0]. WOI is always top-left justified in Virtual Frame. vcw_d minimim = wcw_d +11	00010011$_b$ 1300 Columns

Table 36: Virtual Frame Column Width LSB (53$_h$)

7.17 SOF and VCLK Delay Registers (54_h and 55_h)

This adjust can be used to vary the sync positions (rising and falling edges) relative to valid pixel data. In this way an acquisition system that uses the sync pulses for display can be shifted to add or avoid image borders. Adjusting the position or length of the SOF or VCLK sync does NOT alter the Frame Rate, the sync signal is simply shifted and overlaps the valid line and pixel data. Moving the rising edge of the SOF will also move the rising edge of the VCLK. This is so that the VCLK sync does not occur before the SOF pulse. The delay adjust is in ½ cycles, it takes two programmed counts to delay the rising edge by one image pixel. These delays are measured from the change of the row address, which is not directly observable except to set the delay to 0.

Address 54_h			**SOF Delay**				**Default $4C_h$**
7 (msb)	**6**	**5**	**4**	**3**	**2**	**1**	**0 (lsb)**
sofd[7]	sofd[6]	sofd[5]	sofd[4]	sofd[3]	sofd[2]	sofd[1]	sofd[0]
Bit Number	**Function**	**Description**					**Reset State**
7 - 0	SOF Delay	Delay = $sofd_d$ * 0.5 MCLK's					01001100_b

Table 37: SOF Delay Register (54_h)

Address 55_h			**VCLK Delay**				**Default 02_h**
7 (msb)	**6**	**5**	**4**	**3**	**2**	**1**	**0 (lsb)**
vckd[7]	vckd[6]	vckd[5]	vckd[4]	vckd[3]	vckd[2]	vckd[1]	vckd[0]
Bit Number	**Function**	**Description**					**Reset State**
7 - 0	VCLK Delay	Delay = $vckd_d$ * 0.5 MCLK's					00000010_b

Table 38: VCLK Delay Register (55_h)

7.18 SOF & VCLK Width Register (56_h)

The SOF & VCLK register moves the falling edge of the sync pulses. The widths can be adjusted for maximum compatibility with the frame capture device. The **sofw** bit adjusts the width of the SOF sync and **vckw** adjusts the width of the VCLK pulse.

Address 56_h			**SOF & VCLK Width**				**Default $0E_h$**
7 (msb)	**6**	**5**	**4**	**3**	**2**	**1**	**0 (lsb)**
x	x	x	x	sofw[1]	sofw[0]	vckw[1]	vckw[0]

Bit Number	**Function**	**Description**	**Reset State**
7 - 4	Unused	Unused	$xxxx_b$
3 - 2	SOF Control	00_b = 1 MCLK Wide 01_b = 8 MCLKs Wide 10_b = 64 MCLKs Wide 11_b = Full Row Wide	11_b
1 - 0	VCLK Control	00_b = 1 MCLK Wide 01_b = 8 MCLKs Wide 10_b = 64 MCLKs Wide 11_b = Full Row Wide	10_b

Table 39: SOF & VCLK Width Register (56_h)

7.19 Readout Direction Register (57_h)

This register allows the user to change the direction of readout of the columns or rows. This can be used to compensate for and orientation of the imager in the optical system. The **rrc** when enabled causes the column data to be readout in the reverse direction as compared to the normal readout direction. The **rrr** when enabled causes the row data to be readout in the reverse direction as compared to the normal readout direction. The normal readout direction of the imager is shown in Figure 2 on page 3.

Address 57_h			**Readout Direction**				**Default 04_h**
7 (msb)	**6**	**5**	**4**	**3**	**2**	**1**	**0 (lsb)**
x	x	x	x	FUO	FUO	rrr	rrc

Bit Number	**Function**	**Description**	**Reset State**
7 - 4	Unused	Unused	$xxxx_b$
3 - 2	FUO	*Factory Use Only*	01_b
1	Reverse Readout Row	0_b = Normal Readout (Bottom to Top) 1_b = Rows Readout in reverse order (Top to Bottom)	0_b
0	Reverse Readout Col	0_b = Normal Readout (Left to Right) 1_b = Cols readout in reverse order (Right to Left)	0_b

Table 40: Readout Direction Register (57_h)

7.20 Internal Timing Control Registers ($5F_h$ and 60_h)

These registers are used to define the size of internal timing pulse widths shA (sample & hold sample) and shB (sample & hold reset). In default, both are 10 MCLKs wide. A maximum of 64 MCLKs can be programmed for the shA delay and another 64 MCLKs for the shB delay. Writing 00h to either register will provide the maximum timing delay of 64 MCLKs.

Address $5F_h$			**Internal Timing Control**				**Default $0A_h$**
7 (msb)	**6**	**5**	**4**	**3**	**2**	**1**	**0 (lsb)**
x	x	shA[5]	shA[4]	shA[3]	shA[2]	shA[1]	shA[0]

Bit Number	**Function**	**Description**	**Reset State**
7 - 6	Unused	Unused	$xxxx_b$
5 - 0	shA	shA[5:0]=000000b=64 MCLKs Wide shA[5:0]=000001b=1d MCLKs Wide shA[5:0]=000010b=2d MCLKs Wide shA[5:0]=000011b=3d MCLKs Wide | | shA[5:0]=111111b=63d MCLKs Wide	001010b

Table 41: Internal Timing Control Register ($5F_h$)

Address 60_h			Internal Timing Control				Default $0A_h$
7 (msb)	**6**	**5**	**4**	**3**	**2**	**1**	**0 (lsb)**
x	x	shB[5]	shB[4]	shB[3]	shB[2]	shB[1]	shB[0]

Bit Number	Function	Description	Reset State
7 - 6	Unused	Unused	$xxxx_b$
5 - 0	shB	shB[5:0]=000000b=64 MCLKs Wide shB[5:0]=000001b=1d MCLKs Wide shB[5:0]=000010b=2d MCLKs Wide shB[5:0]=000011b=3d MCLKs Wide | | shB[5:0]=111111b=63d MCLKs Wide	001010b

Table 42: Internal Timing Control Register (60_h)

7.21 Clamp Control and HCLK Delay Register (64_h)

This register is used to delay the position of the first HCLK, which corresponds to the first valid pixel in each row. The Delay is only useful when the HCLK is not continuous. This delay can be used to compensate for any latency in the users capture device. In addition, this register also allows one to disable the Frame Clamp if desired for specific applications (see Section 3.2).

Address 64_h			Clamp Control and HCLK Delay				Default $5C_h$
7 (msb)	**6**	**5**	**4**	**3**	**2**	**1**	**0 (lsb)**
x	fce[6]	FUO	FUO	FUO	hckd[2]	hckd[1]	hckd[0]

Bit Number	Function	Description	Reset State
7	Unused	Unused	x_b
6	Frame Clamp Enable	0_b = Clamp Disabled 1_b = Clamp Enabled	1_b
5 - 3	FUO	FUO	011_b
2 - 0	HCLK Delay	Syncs rising edge of HCLK to valid data from ADC Delay = ((hckd[d]-4) x 0.5) - 16 MCLKs	100_b

Table 43: Clamp Control and HCLK Delay Register (64_h)

7.22 Encoded Sync Register (65_h)

It is possible to capture the image data without the SOF, VCLK, or HCLK syncs. Once the encoded Syncs are enabled, 4 10bit words are placed into the data stream adding 4 pixel times per row. The inserted codes tells the user when the row starts and what type of row it is. Figure 22 on page 23 illustrates the encoded syncs in a data stream.

The **vcb** bit allows the user to force all the Blanking data coming out of the ADC to be 0. The **vcg** bit allows the user to enable/disable encoded sync data in the output stream (see Table 2 on page 11). The **vcc** bit allows the user to clip the output active pixel data to lie between 1 and 1022 to avoid confusion with the encoded sync data in the output stream.

Address 65_h	**Encoded Sync Control**						**Default 00_h**
7 (msb)	**6**	**5**	**4**	**3**	**2**	**1**	**0 (lsb)**
x	vcb	vsg	vcc	FUO	FUO	FUO	FUO

Bit Number	**Function**	**Description**	**Reset State**
7	Unused	Unused	x_b
6	Blanking	0_b = Dark Pixels Used for Blanking 1_b = H-Blanking and V-Blanking are forced to Dout=0	0_b
5	Encoded Sync Enable	0_b = Normal Readout 1_b = Enable Encoded Syncs in Data Stream	0_b
4	Data Clipping	0_b = Normal Readout 1_b = Pixel Data of 0 and 1023 will be clipped to 1 and 1022	0_b
3 - 0	FUO	Factory Use Only	0000_b

Table 44: Encoded Sync Register (65_h)

7.23 Mod64 Column Offset Correction Register (80_h-BF_h)

The Mod64 Column Offset registers are used to reduce/eliminate collimated fixed pattern noise (FPN). There are 64 registers that can be programmed with individual offset values. They will be applied to all the columns on a single image frame on a Modular 64 basis. i.e. Register 80_h Column offset will be applied to Column 0 , 64, 128..., Register 81_h Column offset will be applied to Column 1, 65, 129..., Register BF_h Column offset will be applied to Column 63, 127, 191...etc.

The Column DOVA stage has only six bits of programmability. Registers 20_h is added to the value in $80_h \rightarrow BF_h$ for that column. The final sum is truncated to $\pm 32_d$.

Address 80-BF_h			**Mod64 Column Offset Correction**				**Default 00_h**
7 (msb)	**6**	**5**	**4**	**3**	**2**	**1**	**0 (lsb)**
x	x	mdd[5]	mdd[4]	mdd[3]	mdd[2]	mdd[1]	mdd[0]

Bit Number	**Function**	**Description**	**Reset State**
7 - 6	Unused	Unused	xx_b
5	Sign	0_b = Positive Offset 1_b = Negative Offset	0_b
4 - 0	Column Offset	Offset = 2.6 * mdd_d (64 step @ 2.6mV/step)	00000_b

Table 45: Mod64 Column Offset Correction Register (80_h-BF_h)

Suggested Mod64 Column Offset Correction Register Programming

There are several Column Offset Correction registers whose default values are not optimal for FPN reduction. These registers and the suggested new values are provided in Table 46 below.

Register No.	Register Name	Default Values	New Values
0 x 9F	Mod64 Column 31 Offset	0 x 0_h	0 x 1_h
0 x A0	Mod64 Column 32 Offset	0 x 0_h	0 x 1_h

Table 46. Suggested Mod64 Register Default Value Changes

8.0 I^2C Compatible Serial Interface

The I^2C is an industry standard which is also compatible with the Motorola bus (called M-Bus) that is available on many microprocessor products. The I^2C contains a serial two-wire half-duplex interface that features bi-directional operation, master or slave modes, and multi-master environment support. The clock frequency on the system is governed by the slowest device on the board. The SDATA and SCLK are the bi-directional data and clock pins, respectively. These pins are open drain and will require a pull-up resistor to VDD of 1.5 KΩ to 10KΩ (see Table 1).

The I^2C is used to write the required user system data into the Program Control Registers in the KAC-1310. The I^2C bus can also read the data in the Program Control Register for verification or test considerations. The KAC-1310 is a slave only device that supports a maximum clock rate (SCLK) of 1/24th MCLK while reading or writing only one register address per I^2C start/stop cycle. The following sections will be limited to the methods for writing and reading data into the KAC-1310 register.

For a complete reference to I^2C, see “The I^2C Bus from Theory to Practice” by Dominique Paret and Carll-Fenger, published by John Wiley & Sons, ISBN 0471962686 or refer to Philip Standard online at: http://www.us2.semiconductors.philips.com/i2c/.

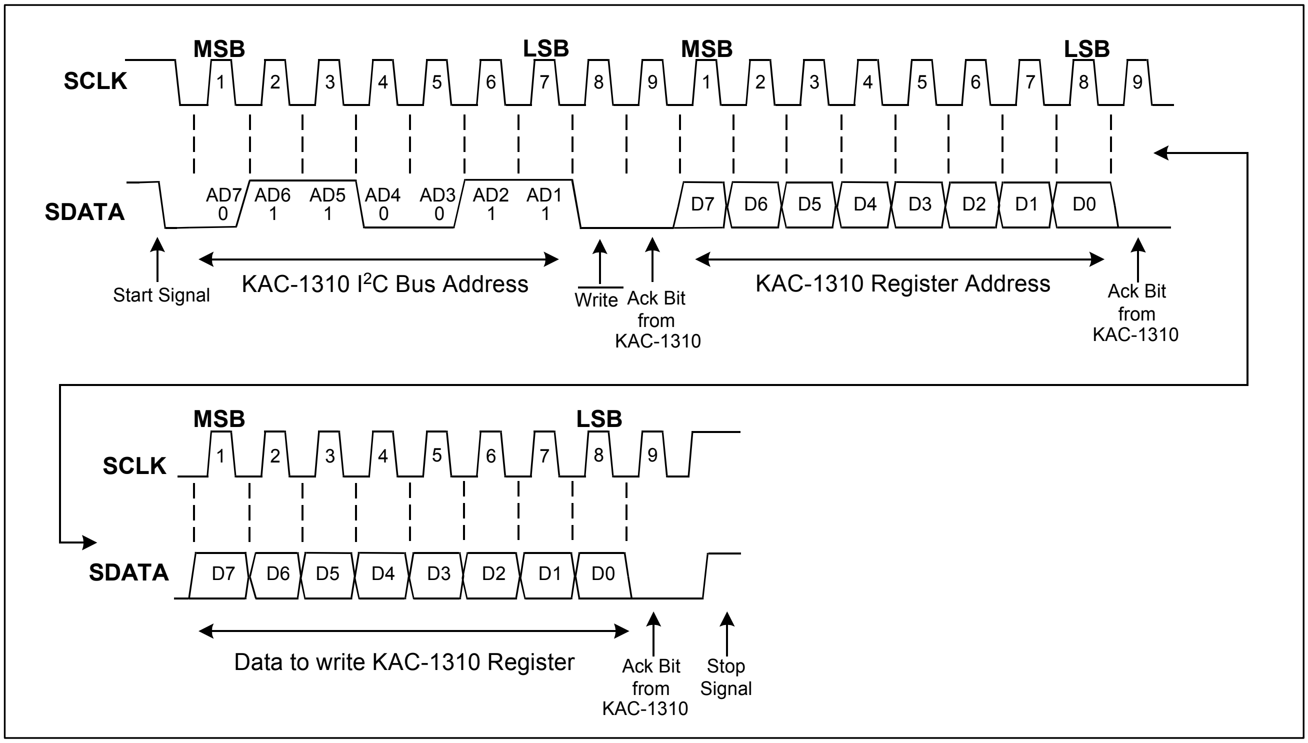


Figure 23: I^2C Bus WRITE Cycle

8.1 KAC-1310 I^{2}C Bus Protocol

The KAC-1310 uses the I^{2}C bus to write or read one register byte per start/stop I^{2}C cycle as shown in Figure 23 and Figure 24. These figures will be used to describe the various parts of the I^{2}C protocol communications as it applies to the KAC-1310. KAC-1310 I^{2}C bus communication is basically composed of following parts: START signal, KAC-1310 slave address (0110011_b) transmission followed by a R/W bit, an acknowledgment signal from the slave, 8-bit data transfer followed by another acknowledgment signal, STOP signal, Repeated START signal, and clock synchronization.

8.2 START Signal

When the bus is free, i.e. no master device is engaging the bus (both SCLK and SDATA lines are at logical “1”), a master may initiate communication by sending a START signal. As shown in Figure 23, a START signal is defined as a high-to-low transition of SDATA while SCLK is high. This signal denotes the beginning of a new data transfer and wakes up all the slaves on the bus.

8.3 Slave Address Transmission

The first byte of a data transfer, immediately after the START signal, is the slave address transmitted by the master. This is a 7-bit calling address followed by a R/W bit. The 7-bit address for the KAC-1310, starting with the MSB (AD7), is 0110011_b. The transmitted calling address on the SDATA line may only be changed while SCLK is low as shown in Figure 23. The data on the SDATA line is valid on the High to Low signal transition on the SCLK line. The R/W bit following the 7-bits tells the slave the desired direction of data transfer: 1 = Read transfer, the slave transitions to a slave transmitter and sends the data to the master; 0 = Write transfer, the master transmits data to the slave.

8.4 Acknowledgment

Only the slave with a calling address that matches the one transmitted by the master will respond by sending back an acknowledge bit. This is done by pulling the SDATA line low at the 9th clock (see Figure 23). If an acknowledgement is not received, many I^{2}C master devices will assume that the slave device is not functioning. No two slaves in the system may have the same address. The KAC-1310 is configured to be a slave only.

8.5 Data Transfer

Once successful slave addressing is achieved, data transfer can proceed between the master and the selected slave in a direction specified by the R/W bit sent by the calling master. Note that for the first byte after a start signal (in Figure 23 and Figure 24), the R/W bit is always a “0” designating a write transfer. This is required since the next data transfer will contain the register address to be read or written. All transfers that come after a calling address cycle are referred to as data transfers, even if they carry sub-address information for the slave device. Each data byte is 8 bits long. Data may be changed only while SCLK is low and must be held stable while SCLK is high as shown in Figure 23. There is one clock pulse on SCLK for each data bit, the MSB being transferred first.

Each data byte has to be followed by an acknowledge bit, which is signaled from the receiving device by pulling the SDATA low at the ninth clock. So one complete data byte transfer needs nine clock pulses. If the slave receiver does not acknowledge the master, the SDATA line must be left high by the slave. The master can then generate a stop signal to abort the data transfer or a start signal (repeated start) to commence a new calling. If the master receiver does not acknowledge the slave transmitter after a byte transmission, it means 'end of data' to the slave, so the slave releases the SDATA line for the master to generate STOP or START signal.

8.6 Stop Signal

The master can terminate the communication by generating a STOP signal to free the bus. However, the master may generate a START signal followed by a calling command without generating a STOP signal first. This is called a Repeated START. A STOP signal is defined as a low-to-high transition of SDATA while SCLK is at logical “1” (see Figure 23). The master can generate a STOP even if the slave has generated an acknowledge bit at which point the slave must release the bus.

8.7 Repeated START Signal

A Repeated START signal is a START signal generated without first generating a STOP signal to terminate the communication. This is used by the master to communicate with another slave or with the same slave in a different mode (transmit/receive mode) without releasing the bus. As shown in Figure 24, page 56, a Repeated START signal is being used during the read cycle and to redirect the data transfer from a write cycle (master transmits the register address to the slave) to a read cycle (slave transmits the data from the designated register to the slave).

8.8 I^2C Bus Clocking and synchronization

Open drain outputs are used on the SCLK outputs of all master and slave devices so that the clock can be synchronized and stretched using wire-AND logic. This means that the slowest device will keep the bus from going faster than it is capable of receiving or transmitting data.

After the master has driven SCLK from High to Low, all the slaves drive SCLK Low for the required period that is needed by each slave device and then releases the SCLK bus. If the slave SCLK Low period is greater than the master SCLK Low period, the resulting SCLK bus signal Low period is stretched. Therefore, synchronized clocking occurs since the SCLK is held low by the device with the longest Low period. Also, this method can be used by the slaves to slow down the bit rate of a transfer. The master controls the length of time that the SCLK line is in the High state. The data on the SDATA line is valid when the master switches the SCLK line from a High to a Low. Slave devices may hold the SCLK low after completion of one byte transfer (9 bits). In such case, it halts the bus clock and forces the master clock into wait states until the slave releases the SCLK line.

8.9 Register Write

Writing the KAC-1310 registers is accomplished with the following I^2C transactions (see Figure 23 page 53):

- Master transmits a START
- Master transmits the KAC-1310 Slave Calling Address with “WRITE” indicated (BYTE=66_h, 102_d, 01100110_b)
- KAC-1310 slave sends acknowledgment by forcing the SDATA Low during the 9th clock, if the Calling Address was received
- Master transmits the KAC-1310 Register Address
- KAC-1310 slave sends acknowledgment by forcing the SDATA Low during the 9th clock after receiving the Register Address
- Master transmits the data to be written into the register at the previously received Register Address
- KAC-1310 slave sends acknowledgment by forcing the SDATA Low during the 9th clock after receiving the data to be written into the Register Address
- The Master transmits STOP to end the write cycle

8.10 Register Read

Reading the KAC-1310 registers is accomplished with the following I^2C transactions (see Figure 24, page 56):

- Master transmits a START
- Master transmits the KAC-1310 Slave Calling Address with “WRITE” indicated (BYTE=66_h, 102_d, 01100110_b)
- KAC-1310 slave sends acknowledgment by forcing the SDATA Low during the 9th clock, if the Calling Address was received
- Master transmits the KAC-1310 Register Address
- KAC-1310 slave sends acknowledgment by forcing the SDATA Low during the 9th clock after receiving the Register Address
- Master transmits a Repeated START
- Master transmits the KAC-1310 Slave Calling Address with “READ” indicated (BYTE = 67_h, 103_d, 01100111_b)
- KAC-1310 slave sends acknowledgment by forcing the SDATA Low during the 9th clock, if the Calling Address was received
- At this point, the KAC-1310 transitions from a “Slave-Receiver” to a “Slave-Transmitter”

- KAC-1310 sends the SCLK and the Register Data contained in the Register Address that was previously received from the master; KAC-1310 transitions to slave-receiver
- Master does not send an acknowledgment (NAK)
- Master transmits STOP to end the read cycle

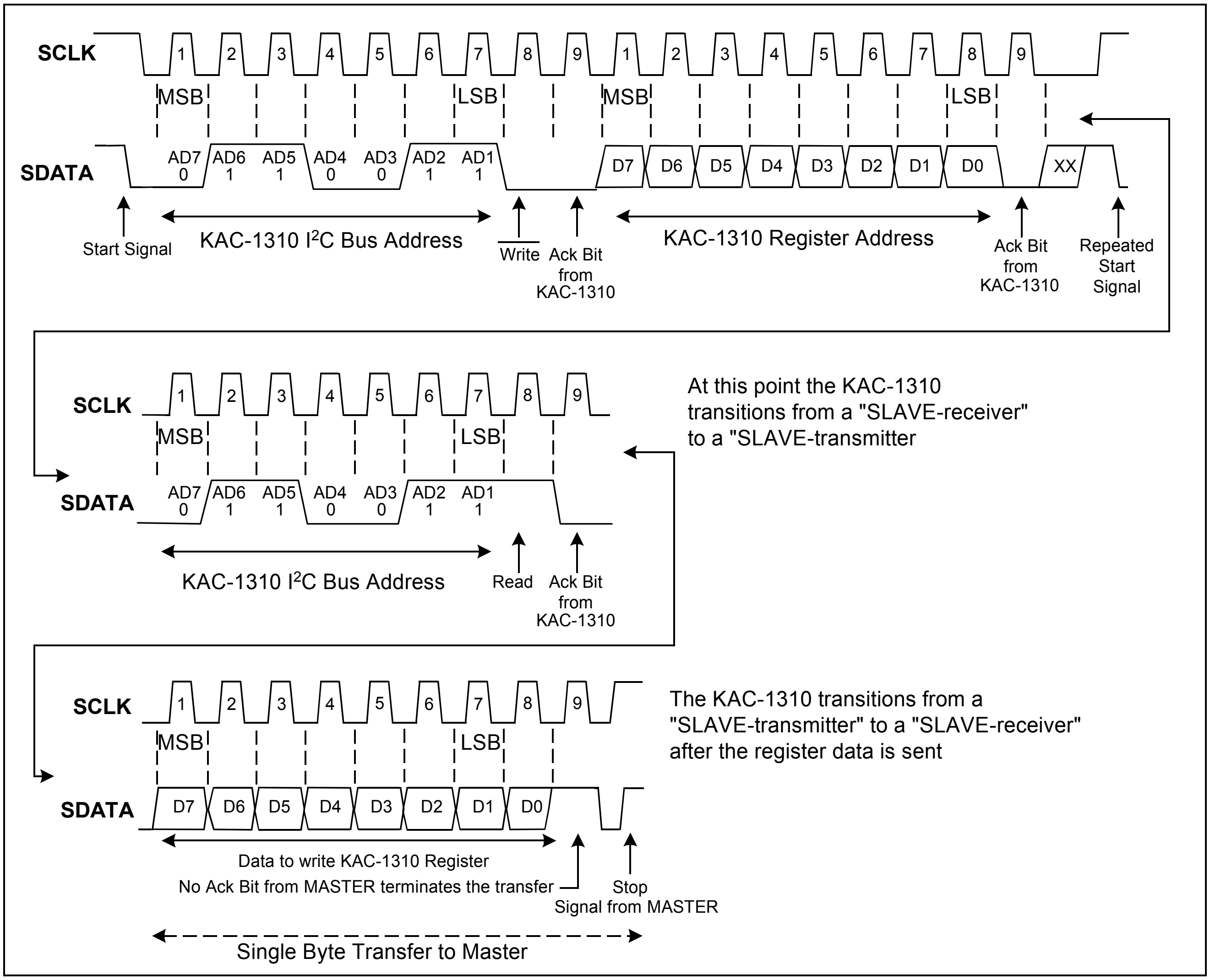


Figure 24: I^2C Bus READ Cycle

9.0 Chip Specifications

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	-0.5 to 3.8	V
V_{in}	DC Input Voltage	-0.5 to (V_{DD} + 0.5)	V
V_{out}	DC Output Voltage	-0.5 to (V_{DD} + 0.5)	V
I_{IO}	DC Current Drain per Pin, Any Single Input or Output	±50	mA
I_{DD}	DC Current Drain, V_{DD} and V_{SS} Pins	±100	mA
T_{STG}	Storage Temperature Range	-65 to +150	°C
T_L	Lead Temperature (10 second soldering)	300	°C

Notes:

- Voltages referenced to VSS
- Maximum Ratings are those values beyond which damage to the device may occur.
- $V_{SS} = AV_{SS} = DV_{SS} = V_{SSO}$ ($DV_{SS} = V_{SS}$ of Digital circuit, $AV_{SS} = V_{SS}$ of Analog Circuit)
- $V_{DD} = AV_{DD} = DV_{DD} = V_{DDO}$ ($DV_{DD} = V_{DD}$ of Digital circuit, $AV_{DD} = V_D$D of Analog Circuit)

Table 47: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_{DD}	DC Supply Voltage, V_{DD} = 3.3V (Nominal)	3.0	3.6	V
T_A	Commercial Operating Temperature	0	40	°C
T_J	Junction Temperature	0	55	°C

Notes:

- All parameters are characterized for DC conditions after thermal equilibrium has been established.
- Unused inputs must always be tied to an appropriate logic level, e.g. either V_{SS} or V_{DD}
- For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS}<(V_{in}$ or $V_{out})< V_{DD}$

Table 48: Recommended Operating Conditions

Symbol	Characteristic	Condition	T_A = 0 °C to 40 °C		Unit
			Min	Max	
V_{IH}	Input High Voltage		2.0	V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		-0.3	0.8	V
I_{in}	Input Leakage Current, No Pull-up Resistor	Vin = V_{DD} or V_{SS}	-5	5	µA
I_{OH}	Output High Current	V_{DD} = Min, V_{OH} Min = 0.8*V_{DD}	-3		mA
I_{OL}	Output Low Current	V_{DD} = Min, V_{OL} Max = 0.4V	3		mA
V_{OH}	Output High Voltage	V_{DD} =Min, I_{OH} = -100mA	V_{DD} - 0.2		V
V_{OL}	Output Low Voltage	V_{DD} = Min, I_{OL} = 100mA		0.2	V
I_{OZ}	3-State Output Leakage Current	Output = High Impedance, Vout = V_{DD} or V_{SS}	-10	10	µA
I_{DD}	Maximum Standby Supply Current	I_{OUT} = 0mA, Vin = V_{DD} or V_{SS}	0	15	mA

V_{DD} = 3.3V + 0.3V; V_{DD} referenced to V_{SS}; Ta = 0 C to 40 C

Table 49: DC Electrical Characteristics

Symbol	Parameter	Condition	Typ	Unit
P_{DYN}	Dynamic Power	13.5 MHz MCLK Clock frequency	250	mW
P_{STDBY}	Standby Power	STDBY Pin Logic High	25	mW
P_{AVG}	Average Power	13.5 MHz Operation (using STDBY)	200	mW

V_{DD} = 3.0V, V_{DD} referenced to V_{SS}, 25 °C

Table 50: Power Dissipation

Symbol	Parameter		Typ	Unit	Notes
N_{sat}	Saturation Signal		40,000	electrons	
QE	Peak Quantum Efficiency	Monochrome no µLens @ 550nm	34	%	1
		Red w/µLens @ 650nm	38	"	"
		Green w/µLens @ 540nm	37	"	"
		Blue w/µLens @ 460nm	20	"	"
		Cyan w/µLens @ 530nm	46	"	"
		Magenta w/µLens @ 650nm	45	"	"
		Yellow w/µLens @ 590nm	46	"	"
PRNU	Photoresponse Non-uniformity	Global	4	% rms	
		Local	1.5	"	2
S	Responsivity	Monochrome no µLens	1.11	V/lux-sec	3
			59,800	e-/lux-sec	"
		Red w/µLens	0.5	V/lux-sec	"
			27,100	e-/lux-sec	"
		Green w/µLens	0.6	V/lux-sec	"
			32,200	e-/lux-sec	"
		Blue w/µLens	0.32	V/lux-sec	"
			17,500	e-/lux-sec	"
		Cyan w/µLens	1.04	V/lux-sec	"
			55,800	e-/lux-sec	"
		Magenta w/µLens	0.81	V/lux-sec	"
			43,600	e-/lux-sec	"
		Yellow w/µLens	1.2	V/lux-sec	"
			64,700	e-/lux-sec	"

Notes:

1. Refers to nominal spectral response values as provided in Figures 3, 4, and 5. QE range is +/- 20%
2. For a 100 x 100 pixel region under uniform illumination with output signal equal to 80% of saturation signal.
3. Measurements assume a 3200K source with Hoya CM500 filter. All values referenced at the floating diffusion node. To calculate values at the sensor outputs, on-chip gain stages should be linearly applied to the given values.

Table 51. Electro-Optical Characteristics

Symbol	Parameter	Typ	Unit	Notes
I_d	Photodiode Dark Current	1 / 4	fA/pixel	4
		6,250 / 25,000	e-/pixel/sec	4
Lag	Pixel Charge Transfer Inefficiency	<1	%	5
X_{ab}	Blooming Margin - shuttered light	200x	X Vsat	6
$n_{e^- \text{total}}$	Total System (equivalent) Noise Floor	70	e^- rms	7
DR	System Dynamic Range	54	dB	9, 12, 13
	Resolution	10	bits	
f_{max}	Maximum MCLK	20	MHz	8
f_{nom}	Nominal MCLK	10	MHz	9
ϕ_{A-X}	Acceptance Angle in Horizontal direction	15	Degrees	11
ϕ_{A-Y}	Acceptance Angle in Vertical direction	27	Degrees	11
	Image Array Size	7.7 x 6.1 (~$^1/_2$")	mm	
	Pixel Size	6.0 x 6.0	µm	
	Frame Rate	0 - 15	FPS	
	Fill Factor	40 / 64	%	10

Notes:

4. Measured at sensor temperatures of 25 °C / 40 °C.
5. Transfer inefficiency of photosite.
6. Xab represents the increase above the saturation-irradiance level (Hsat) that the device can be exposed to before blooming of the pixel will occur.
7. Includes amplifier noise, dark pattern noise and dark current shot noise at 10 MHz data rates.
8. All performance specs are not guanteed at this speed.
9. All Imager specs are held between 1 MHz and 10 MHz
10. Monochrome sensor without microlens / color sensor with microlens
11. Angle at which Responsivity is reduced by 3dB.
12. DR is defined as the standard deviation of temporal noise divided by the mean signal at saturation.
13. Saturation signal is defined as the maximum sensor output achieved while maintaining $\leq$ 2% response non-linearity.

Table 51 Electro-Optical Characteristics Continued…

Symbol	Characteristic	Min	Max	Unit
f_{max}	SCLK maximum frequency	50	1/24 MCLK	KHz[1]
M1	Start condition SCLK hold time	4	-	T_{MCLK}[3]
M2	SCLK low period	8	-	T_{MCLK}
M3	SCLK/SDATA rise time [from $V_{IL} = (0.2)*V_{DD}$ to $V_{IH} = (0.8)*V_{DD}$]	-	0.3	µs[2]
M4	SDATA hold time	4	-	T_{MCLK}[3]
M5	SCLK/SDATA fall time (from Vh = 2.4V to Vl = 0.5V)	-	0.3	µs[2]
M6	SCLK high period	4	-	T_{MCLK}
M7	SDATA setup time	4	-	T_{MCLK}[3]
M8	Start / Repeated Start condition SCLK setup time	4	-	T_{MCLK}
M9	Stop condition SCLK setup time	4	-	T_{MCLK}
C_I	Capacitive for each I/O pin	-	10	pF
Cbus	Capacitive bus load for SCLK and SDATA	-	200	pF
Rp	Pull-up Resistor on SCLK and SDATA	1.5	10	kΩ[4]

Notes:

[1] SCLK frequency maximum limit is 1/24 MCLK frequency.

[2] The capaitive load is 200pF

[3] The unit TMCLK is the period of the input master clock; the frequency of MCLK is assumed 10.0 MHz.

[4] A pull-up resistor to VDD is required on each of the SCLK and SDATA lines; for a maximum bus capacitive load of 200pF, the minimum value of Rp should be selected in order to meet specifications.

I2C is a proprietary Philips interface bus.

Table 52: I^{2}C Compatible Serial Interface Timing Specification

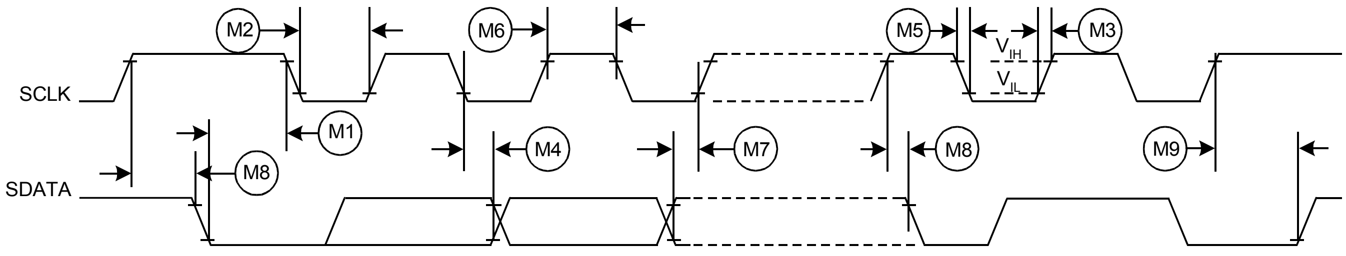


Figure 25: I^{2}C Bus Timing

Symbol	Characteristic	Min	Typ	Max	Unit
f_{max}	MCLK maximum frequency	1	10	20	MHz
t_{htrig}	TRIGGER hold time w.r.t. MCLK	3.5	-	9	ns
t_{sutrig}	TRIGGER setup time w.r.t. MCLK	3.0	-	8.5	ns
t_{dsof}	MCLK to SOF delay time	8	13	21.5	ns
t_{dvclk}	MCLK to VCLK delay time	8.5	13.5	22	ns
t_{drhclk}	Rising edge of MCLK to rising edge fo HCLK delay time	7.5	13	22	ns
t_{dfhclk}	Falling edge of MCLK to falling edge of HCLK delay time	3	5	10.5	ns
t_{dadc}	MCLK to ADC[9:0] delay time	8	13	21.5	ns
t_{dblank}	MCLK to BLANK delay time	8	13	21.5	ns

Table 53: Pixel Data Bus and Sync Timing Specification

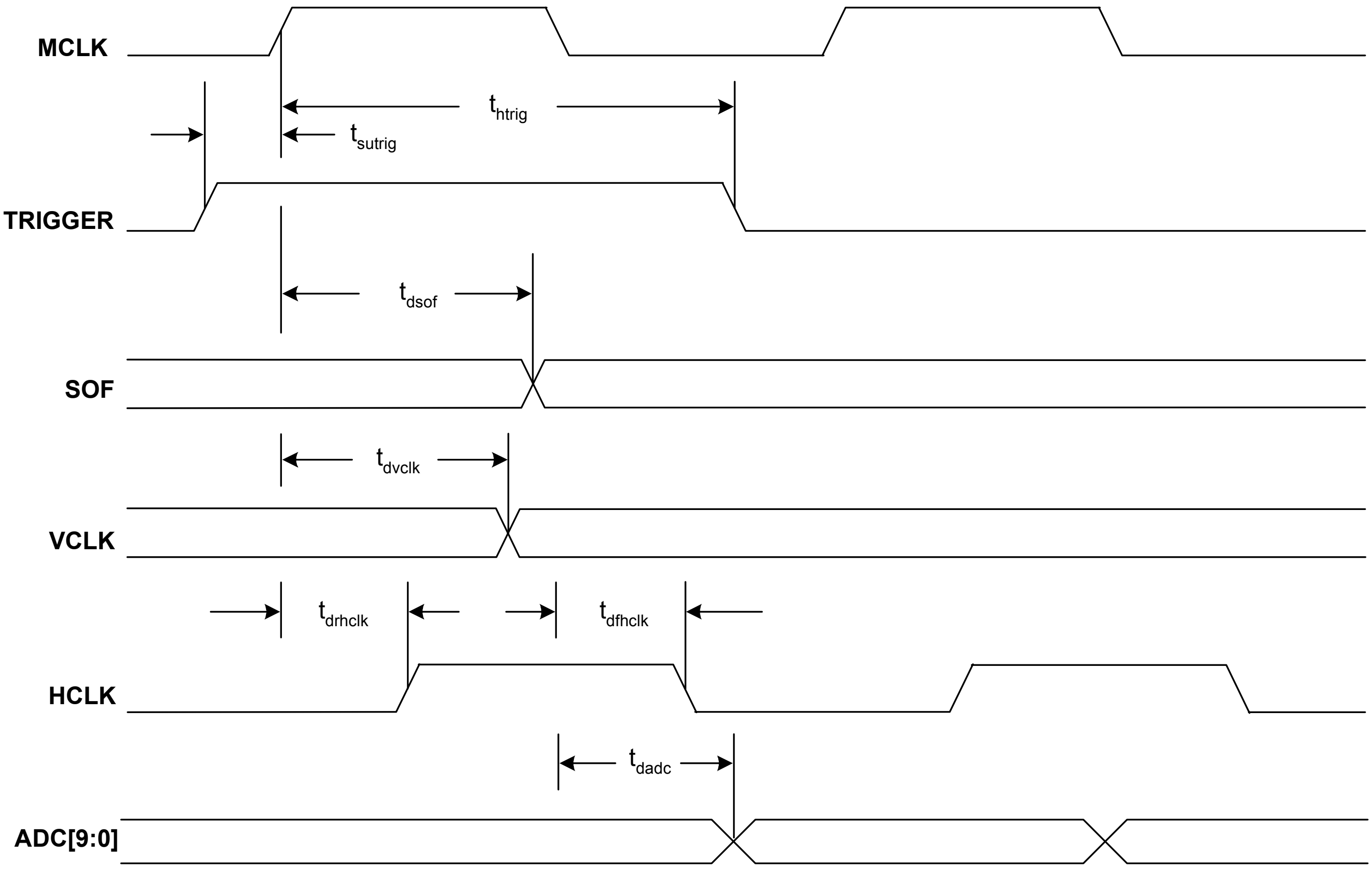
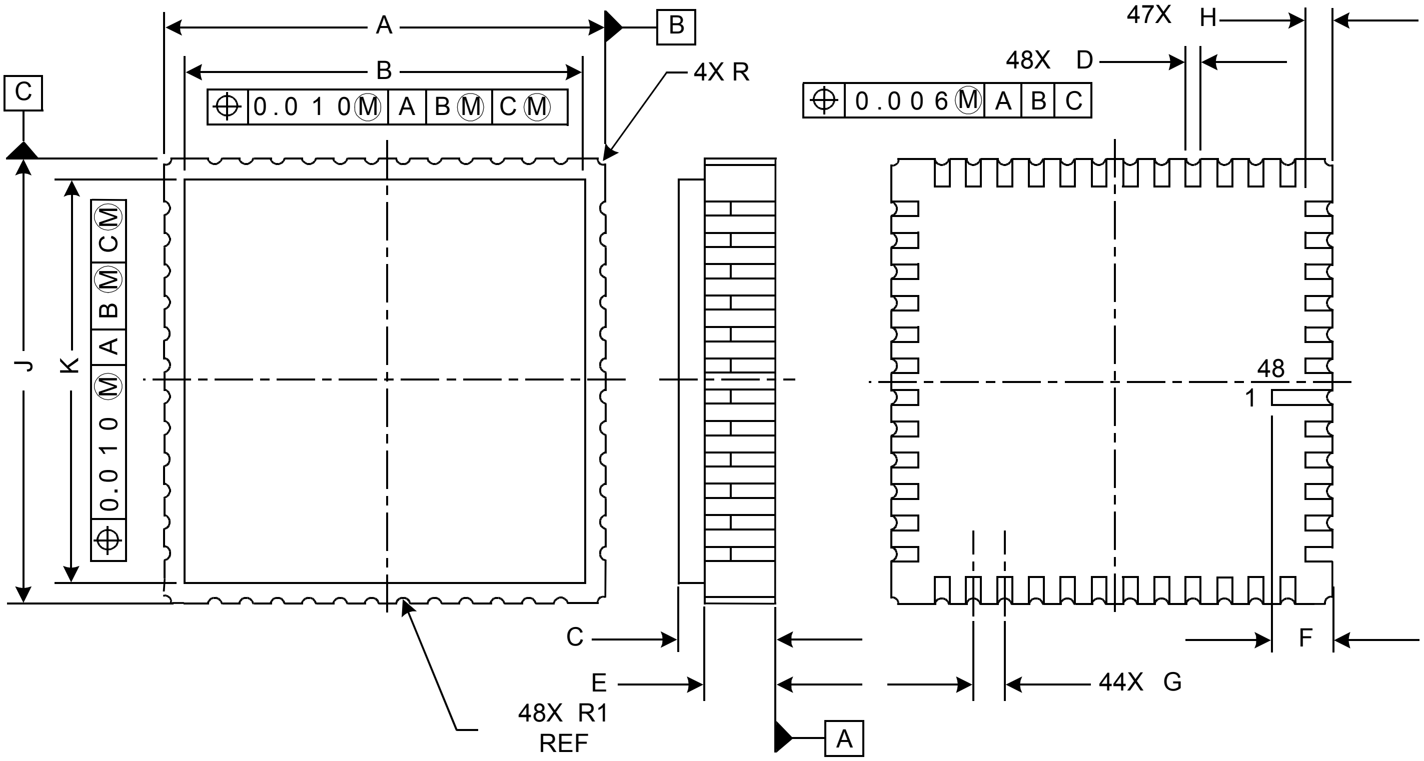


Figure 26: Pixel Data Bus Timing Diagram



Dimension	Minimum (inches)	Nominal (inches)	Maximum (inches)
A	0.555	0.56	0.572
B	0.525	0.54	0.545
C	---	---	0.12
D	0.016	0.02	0.024
E	0.055	0.061	0.067
F	0.075	0.085	0.095
G		0.04 BSC	
H	0.033	0.04	0.047
J	0.555	0.56	0.572
K	0.525	0.54	0.545
R		0.008 REF	
R1		0.028 REF	

Figure 27: 48 Pin Terminal Ceramic Leadless Chip Carrier (Bottom View)

		Metric (mm)			English (mils)		
Dimension	Description	Min	Nominal	Max	Min.	Nominal	Max
A	Glass (Thickness)	0.5	0.55	0.6	19.69	21.65	23.62
B	Cavity (Depth)	0.9906	1.1176	1.2446	39.00	44.00	49.00
C	Die - Si (Thickness)	0.705	0.725	0.745	27.76	28.54	29.33
D	Bottom Layer (Thickness)	0.381	0.4318	0.4826	15.00	17.00	19.00
E	Die Attach - bondline (Thickness)	0.0127	0.0254	0.0508	0.50	1.00	2.00
F	Glass Attach - bondline (Thickness)	0.00635	0.0254	0.0508	0.25	1.00	2.00
G	Imager to Lid - outer surface (d)	0.70115	0.9426	1.1777	27.60	37.11	46.37
H	Imager to Lid - inner surface (d)	0.20115	0.3926	0.5777	7.92	15.46	22.74
J	Imager to seating plane - of pkg	1.0987	1.1822	1.2784	43.26	46.54	50.33
A+B+F+D	Pkg (Th - total)	1.87795	2.1248	2.378	73.93	83.65	93.62
B+D	Base (Th)	1.397	1.5494	1.7018	55.00	61.00	67.00

Reference Notes:

1 mil = 25.4um

1 mm = 39.37 mil

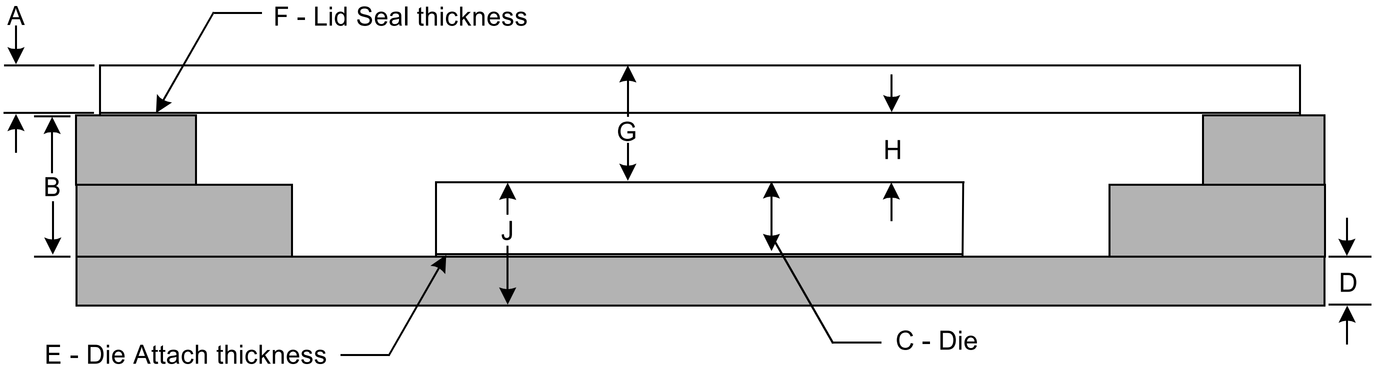


Figure 28: CLCC-IB package vertical Dimensioning

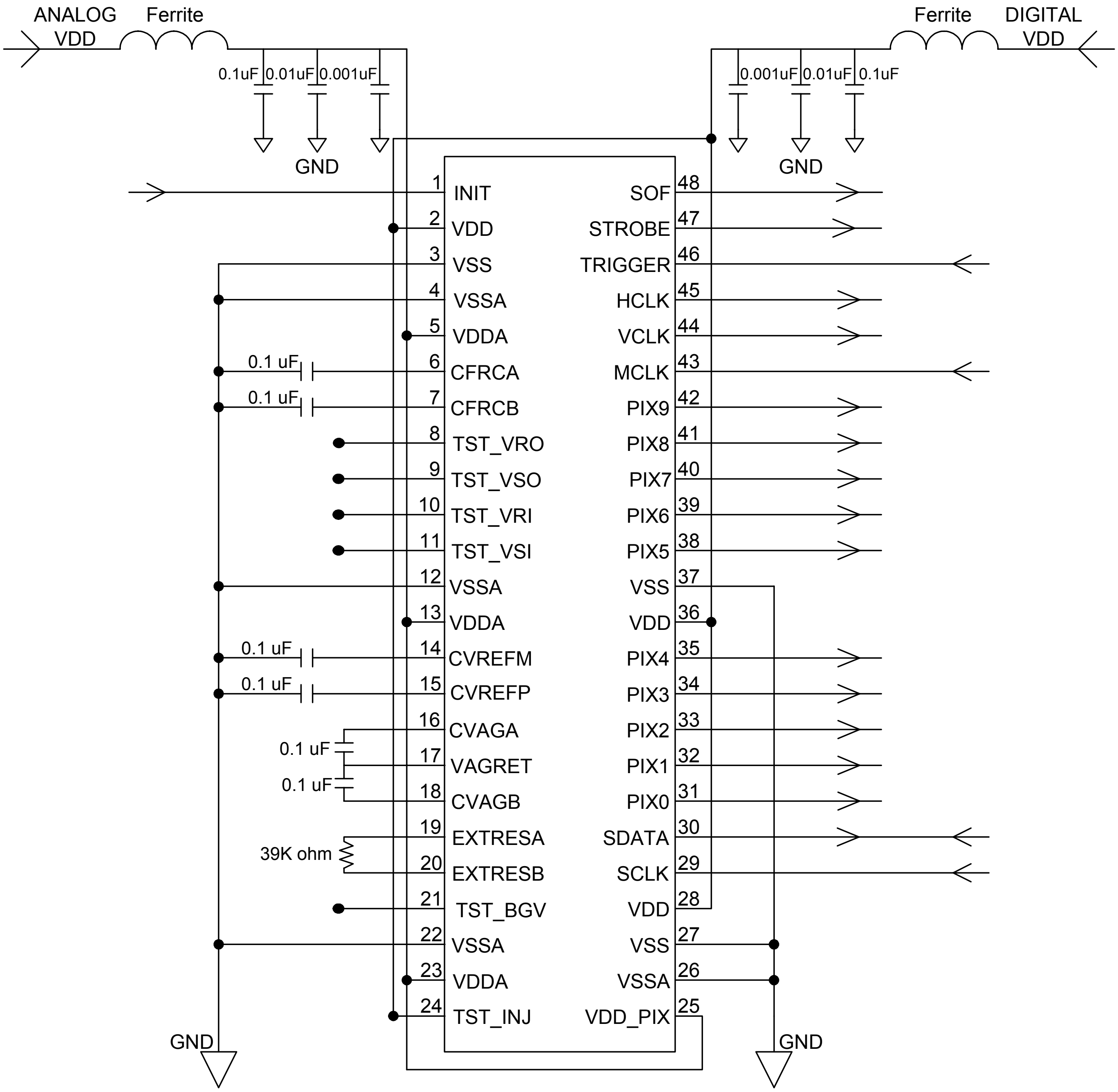


Figure 29: KAC-1310 Pin Connection Schematic

Recommended Hardware for KAC-1310 Sensor Evaluation:

1) Kodak Evaluation Board (for parts list and pricing contact our Sales Office @ http://www.kodak.com/go/imagers)
2) National Instruments Framegrabber PCI-1422 LVDS (http://www.ni.com)
3) Calibre I^{2}C Adapter PCI93 LV (http://www.calibreuk.com)
4) Windows NT or 98 Operating System.

10.0 Reflow Soldering Recommendations

When using a reflow soldering system, the thermal profile shown in Figure 30 below shows the maximum recommended thermal profile. If the temperature and/or time of the soldering process exceed the recommended profile, there is a possibility of damaging the sensor.

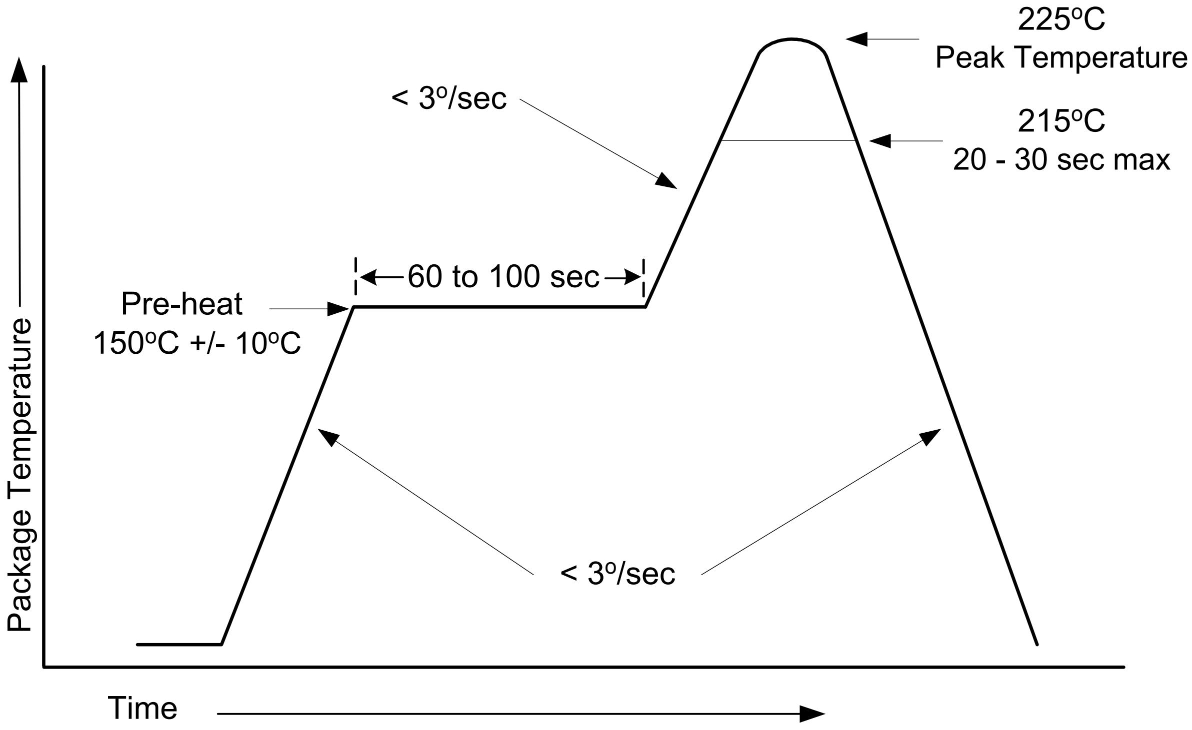


Figure 30: Recommended Soldering Thermal Profile