

AU9382

USB Flash Disk Controller

Technical Reference Manual

Revision 1.0



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Contact Information:

Web site: <http://www.alcormicro.com/>

Taiwan

Alcor Micro Corp.
4F-1, No 200 Kang Chien Rd., Nei Hu,
Taipei, Taiwan, R.O.C.
Phone: 886-2-8751-1984
Fax: 886-2-2659-7723

Santa Clara Office

2901 Tasman Drive, Suite 206
Santa Clara, CA 95054
USA
Phone: (408) 845-9300
Fax: (408) 845-9086

Los Angeles Office

9400 Seventh St., Bldg. A2
Rancho Cucamonga, CA 91730
USA
Phone: (909) 483-9900
Fax: (909) 944-0464

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1.0 Introduction

1.1 Description

The AU9382 is a highly integrated single chip USB flash disk controller. It provides the most cost effective bridge between USB enabled PC and NAND type flash memory. AU9382 can be used as a removable storage disk in enormous data exchange applications between PC, Macintosh, laptop and workstation. It can also be configured as a bootable disk for system repairing .

AU9382 works with 2 NAND type flash memory chips with the combination of popular flash memory types such as 8M, 16M, 32M, 64M and 128M. Additional features include write protection switch, activity LED and password-protected security .

AU9382 integrates 48MHz PLL, 3.3V regulator, power on reset circuit and a power switch for flash memory power control.

1.2 Features

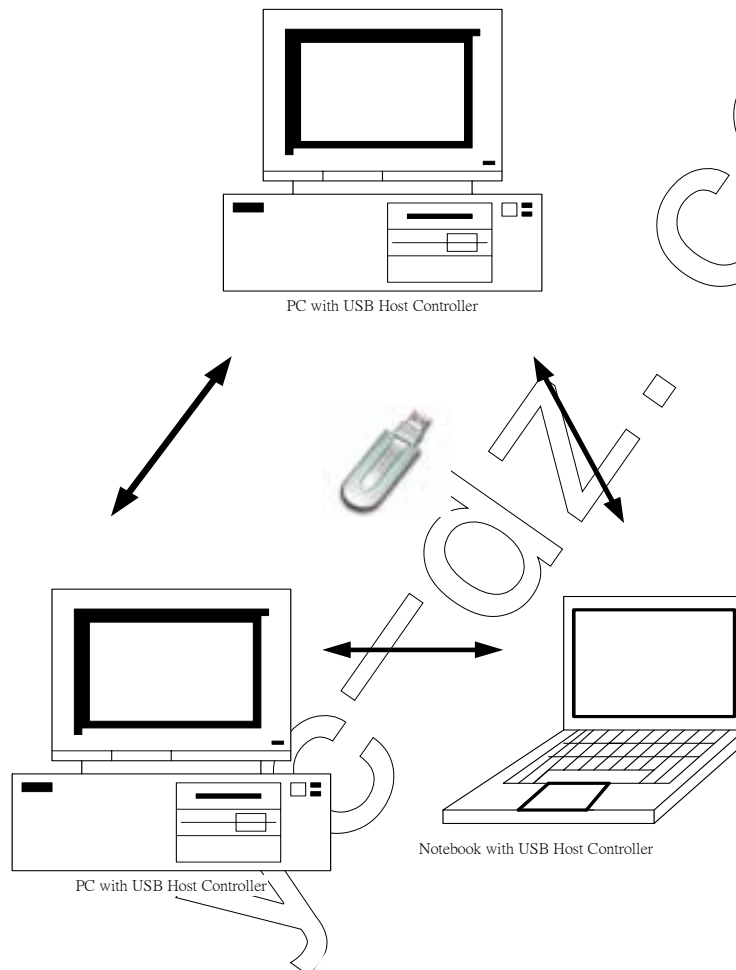
- Fully compliant with USB v1.1 specification and USB Device Class Definition for Mass Storage, Bulk-Transport v1.0
- Work with default driver from Windows ME, Windows 2000, Windows XP, Mac OS 9.1, and Mac OS X. Windows 98se is supported by vendor driver from Alcor.
- Multiple FIFO implementation for concurrent bus operation
- Supports 2 pieces NAND type Flash memory chips; total capacity reaches to 512 M byte when working with 2G bit mono dies chip.
- Support mixed different size combination of NAND type flash chips.
- Vendor ID, product ID and strings can be customized by utility software provided by Alcor Micro
- Can be configured to support dual partitions with dynamic logic disk space allocation.
- Can be configured as “removable” or “HDD” type disk by utility software as customers’ requirement.
- Security function supported with password protection
- LED for bus activity monitoring
- Runs at 12MHz, built-in 48 MHz PLL
- Built-in 3.3V regulator
- Built-in power switch and power management circuit to achieve 500uA suspend current required by USB specification.
- Built-in power on reset circuit

- Dedicated DMA engine to ensure highest throughput in read and write
- Packed in 28-pin SSOP form.

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2.0 Application Block Diagram

Following is the application diagram of a typical flash disk product with AU9382. By connecting the flash disk to a desktop or notebook PC through USB bus, AU9382 is implemented as a bus-powered, full speed USB disk, which can be used as a bridge for data transfer between Desktop PC and Notebook PC.



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3.0 Pin Assignment

The AU9382 is packed in 28-pin SSOP form factor. The figure on the following page shows the signal names for each of the pins on the chip. Accompanying the figure is the table that describes each of the pin signals.

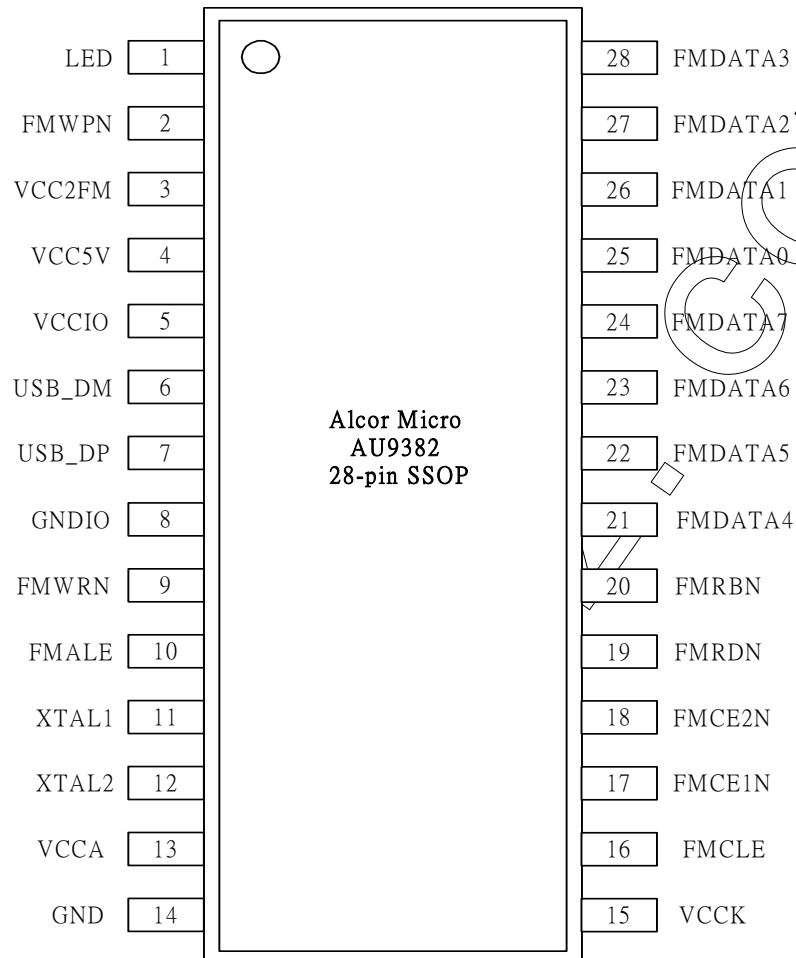
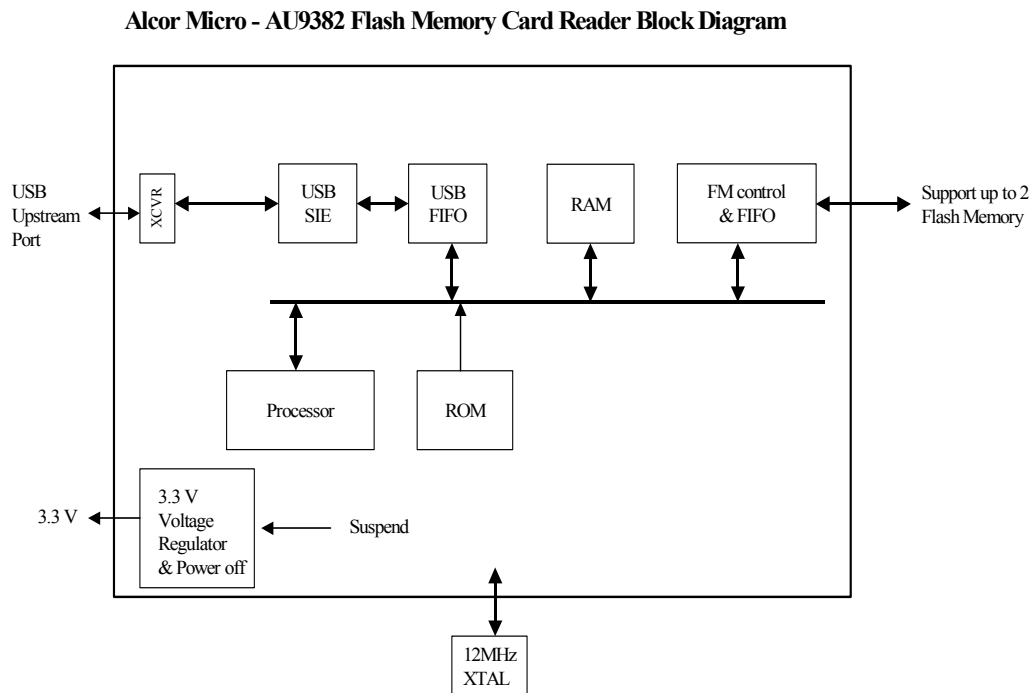


Table 3-1. Pin Descriptions

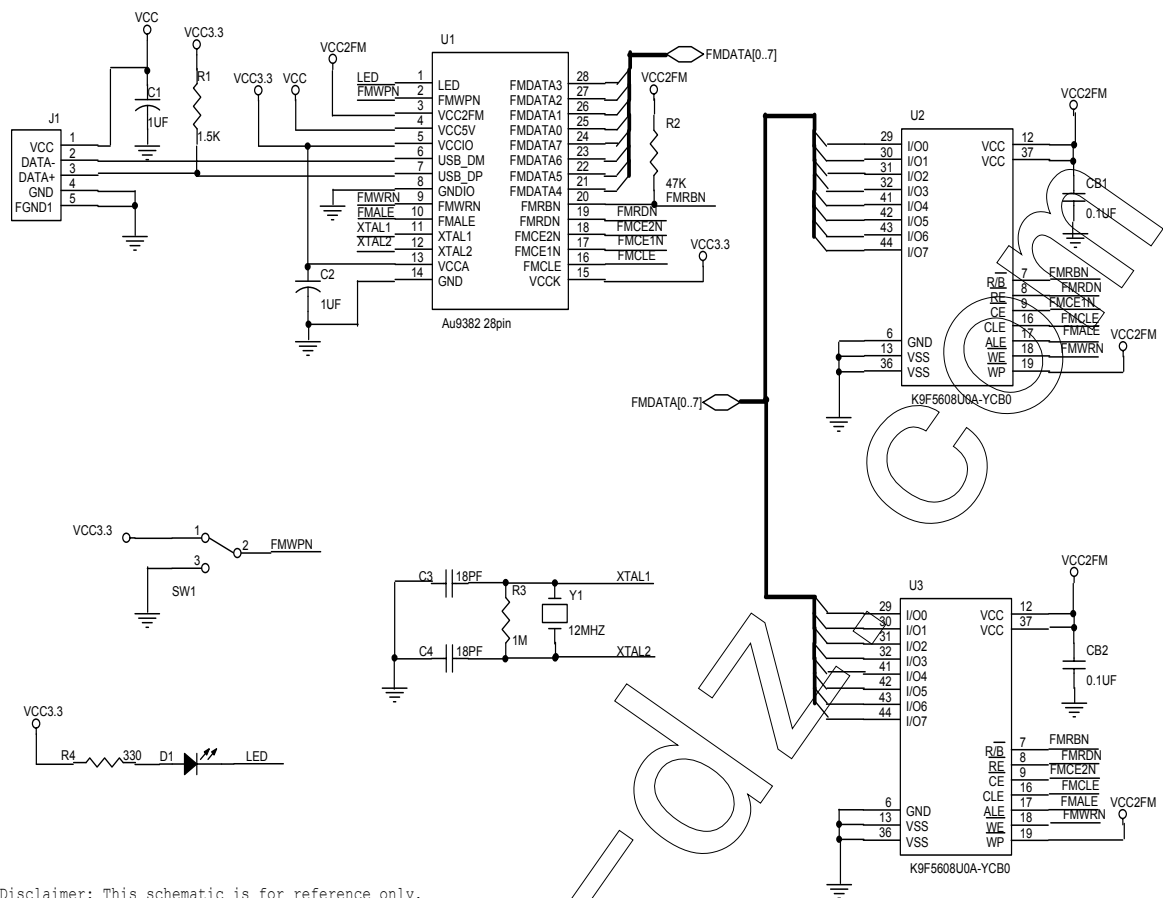
Pin No.	Pin Name	Pin Type	Description
1	LED	O	General Purpose Out, used as activity LED.
2	FMWPN	I	Flash memory write protect. Connected to on board flash memory write protect switch. 0: write protected, 1: no write protection.
3	VCC2FM	PWR	Flash memory power supply, 3.3V. Connect to Flash Memory Vcc.
4	VCC5V	PWR	5V power supply from USB connector.
5	VCCIO	PWR	Internally regulated 3.3V power supply output. It is used to pull up USB_DP externally, as well as being the power supply for VCKK and VCCA.
6	USB_DM	I/O	USB D-.
7	USB_DP	I/O	USB D+.
8	GNDIO	PWR	I/O Ground.
9	FMWRN	O	Flash Memory Write Enable. 0: write enabled, 1: write disabled.
10	FMALE	O	Flash Memory Address Latch Enable. 0: address latch closed, 1: address latch open.
11	XTAL1	I	Crystal Oscillator Input (12MHz).
12	XTAL2	O	Crystal Oscillator Output (12MHz).
13	VCCA	PWR	Analog 3.3V input.
14	GND	PWR	Ground.
15	VCKK	PWR	Core 3.3V Input.
16	FMCLE	O	Flash Memory Command Latch Enable. 0: command latch closed, 1: command latch open.
17	FMCE1N	O	Flash Memory Chip1 Enable. 0: disable, 1: enable.
18	FMCE2N	O	Flash Memory Chip2 Enable. 0: disable, 1: enable.
19	FMRDN	O	Flash Memory Read Enable. 0: read enable, 1: read disable.
20	FMRBN	I	Flash Memory Ready/Busy. 0: busy, 1: ready.
21	FMDATA4	I/O	Flash Memory Data4.
22	FMDATA5	I/O	Flash Memory Data5.
23	FMDATA6	I/O	Flash Memory Data6.
24	FMDATA7	I/O	Flash Memory Data7.
25	FMDATA0	I/O	Flash Memory Data0.
26	FMDATA1	I/O	Flash Memory Data1.
27	FMDATA2	I/O	Flash Memory Data2.
28	FMDATA3	I/O	Flash Memory Data3.

4.0 System Architecture and Reference Design

4.1 AU9382 Block Diagram



4.2 Sample Schematics



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A	Au9382 Flash disk demonstration schematics	1.00
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5.0 Electrical Characteristics

5.1 Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
V _{CC}	Power Supply	4.75	5	5.25	V
V _{IN}	Input Voltage	0		V _{CC}	V
T _{OPR}	Operating Temperature	0		85	°C
T _{STG}	Storage Temperature	-40		125	°C

5.2 General DC Characteristics

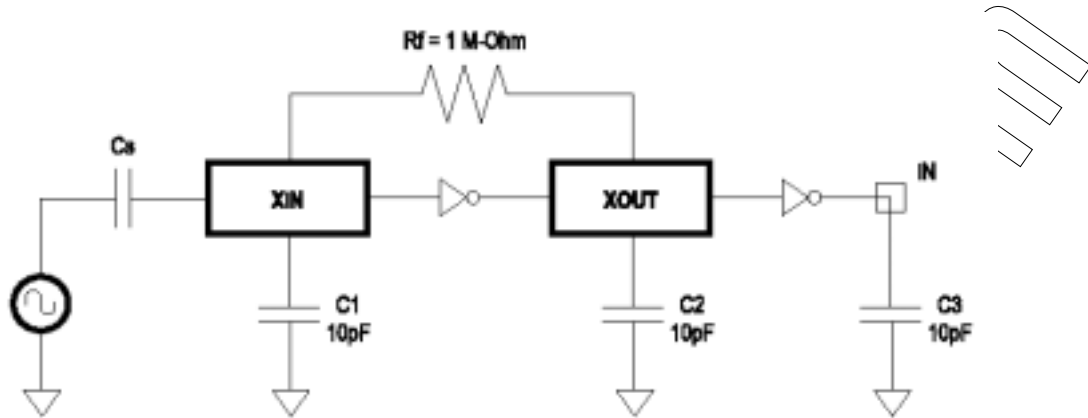
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I _{IL}	Input low current	no pull-up or pull-down	-1		1	μA
I _{IH}	Input high current	no pull-up or pull-down	-1		1	μA
I _{OZ}	Tri-state leakage current		-10		10	μA
C _{IN}	Input capacitance			5		pF
C _{OUT}	Output capacitance			5		pF
C _{BID}	Bi-directional buffer capacitance			5		pF

5.3 DC Electrical Characteristics for 3.3 volts operation

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V _{IL}	Input Low Voltage	CMOS			0.9	V
V _{IH}	Input Hight Voltage	CMOS	2.3			V
V _{OL}	Output low voltage	I _{OL} =4mA, 16mA			0.4	V
V _{OH}	Output high voltage	I _{OH} =4mA, 16mA	2.4			V
R _I	Input Pull-up/down resistance	V _{il} =0 _v or V _{ih} =V _{CC}		10k/200k		KΩ

5.4 Crystal Oscillator Circuit Setup for Characterization

The following setup was used to measure the open loop voltage gain for crystal oscillator circuits. The feedback resistor serves to bias the circuit at its quiescent operating point and the AC coupling capacitor, C_s , is much larger than C_1 and C_2 .



5.5 ESD Test Results

Test Description : ESD Testing was performed on a Zapmaster system using the Human-Body –Model (HBM) and Machine-Model (MM), according to MIL_STD 883 and EIAJ IC_121 respectively.

- Human-Body-Model stress devices by sudden application of a high voltage supplied by a 100 PF capacitor through 1.5 Kohm resistance.
- Machine-Model stresses devices by sudden application of a high voltage supplied by a 200 PF capacitor through very low (0 ohm) resistance

Test circuit & condition

- Zap Interval : 1 second
- Number of Zaps : 3 positive and 3 negative at room temperature
- Criteria : I-V Curve Tracing

Model	Model	S/S	TARGET	Results
HBM	Vdd, Vss, I/C	15	4000V	Pass
MM	Vdd, Vss, I/C	15	200V	Pass

5.6 Latch-Up Test Results

Test Description: Latch-Up testing was performed at room ambient using an IMCS-4600 system which applies a stepped voltage to one pin per device with all other pins open except Vdd and Vss which were biased to 5 Volts and ground respectively.

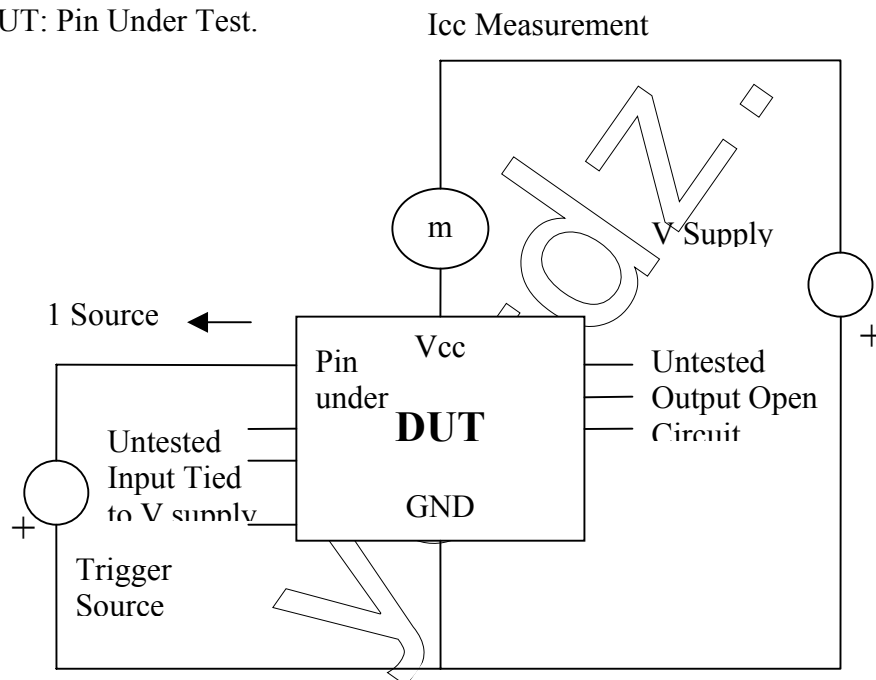
Testing was started at 5.0 V (Positive) or 0 V (Negative), and the DUT was biased for 0.5 seconds.

If neither the PUT current supply nor the device current supply reached the predefined limit (DUT=0 mA, $I_{cc}=100$ mA), then the voltage was increased by 0.1 Volts and the pin was tested again.

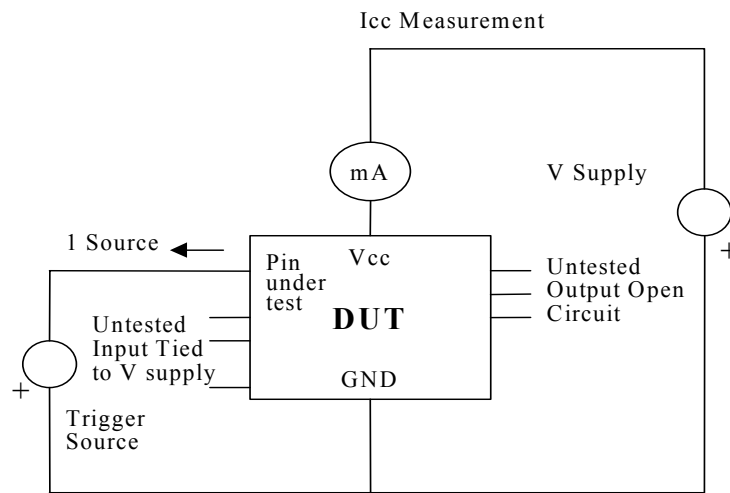
This procedure was recommended by the JEDEC JC-40.2 CMOS Logic standardization committee.

Notes:

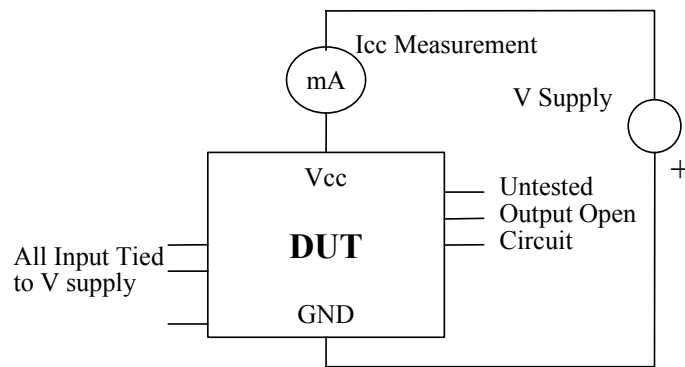
1. DUT: Device Under Test.
2. PUT: Pin Under Test.



Test Circuit : Positive Input/ output Overvoltage /Overcurrent



Test Circuit : Negative Input/ Output Overvoltage /Overcurrent



Supply Voltage test

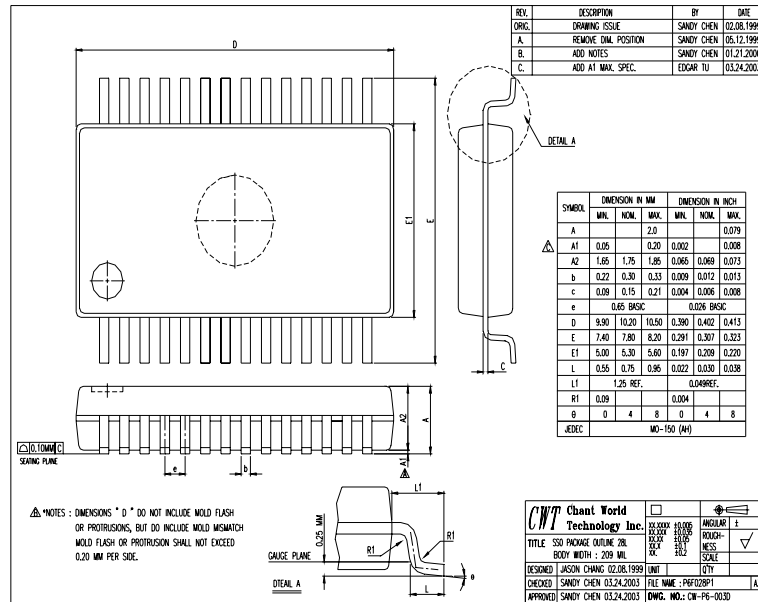
Latch-Up Data

Model	Model	Voltage (v)/ Current (mA)	S/S	Results
Voltage	+	11.0	5	Pass
	-	11.0		
Current	+	200	5	
	-	200		
Vdd-Vxx		9.0	5	Pass

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6.0 Mechanical Information

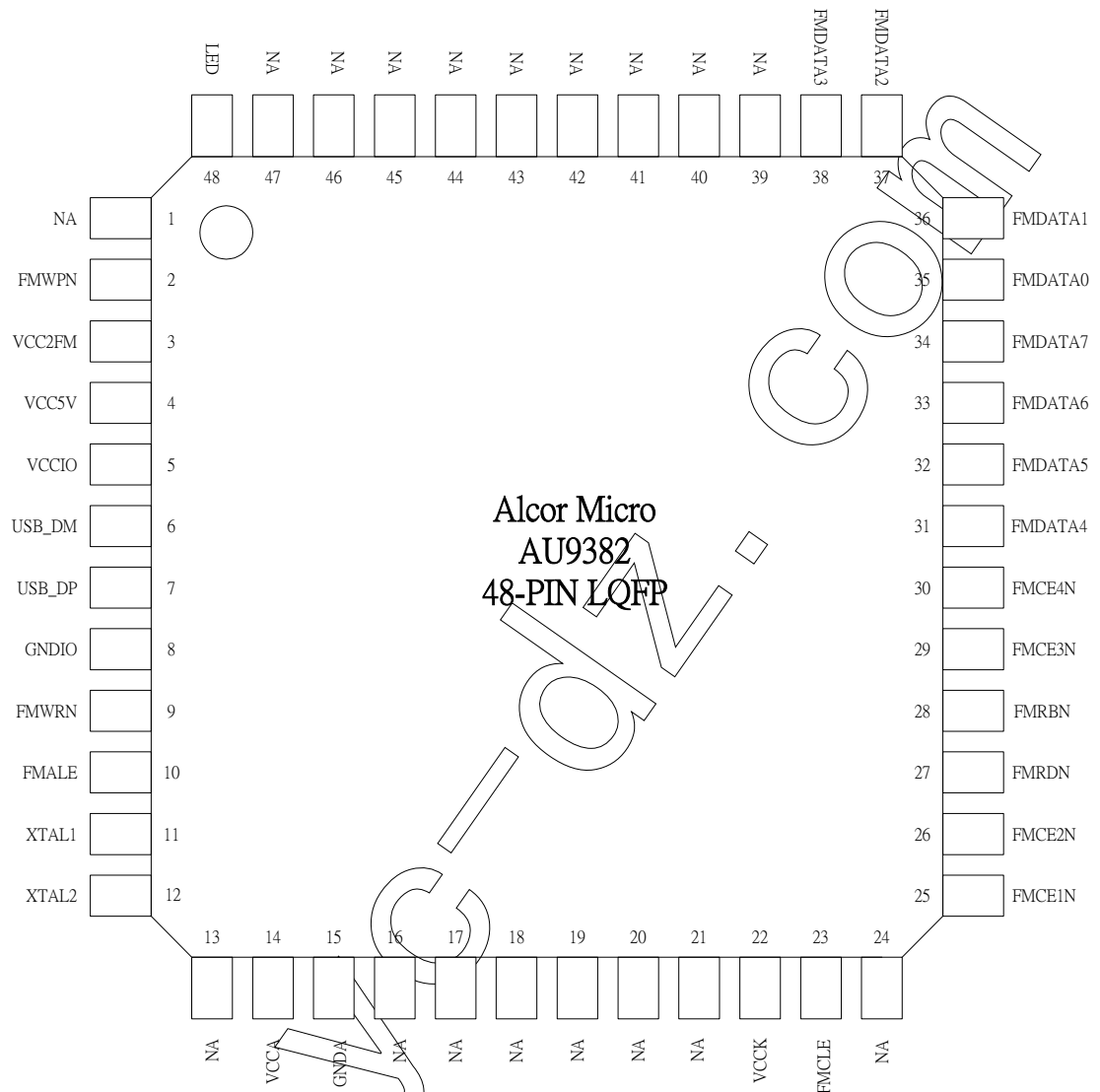
Following diagram shows the dimensions of the AU9382 28-pin SSOP.



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7.0 Appendix---48-PIN LQFP

7.1 48-PIN LQFP Pin Assignment

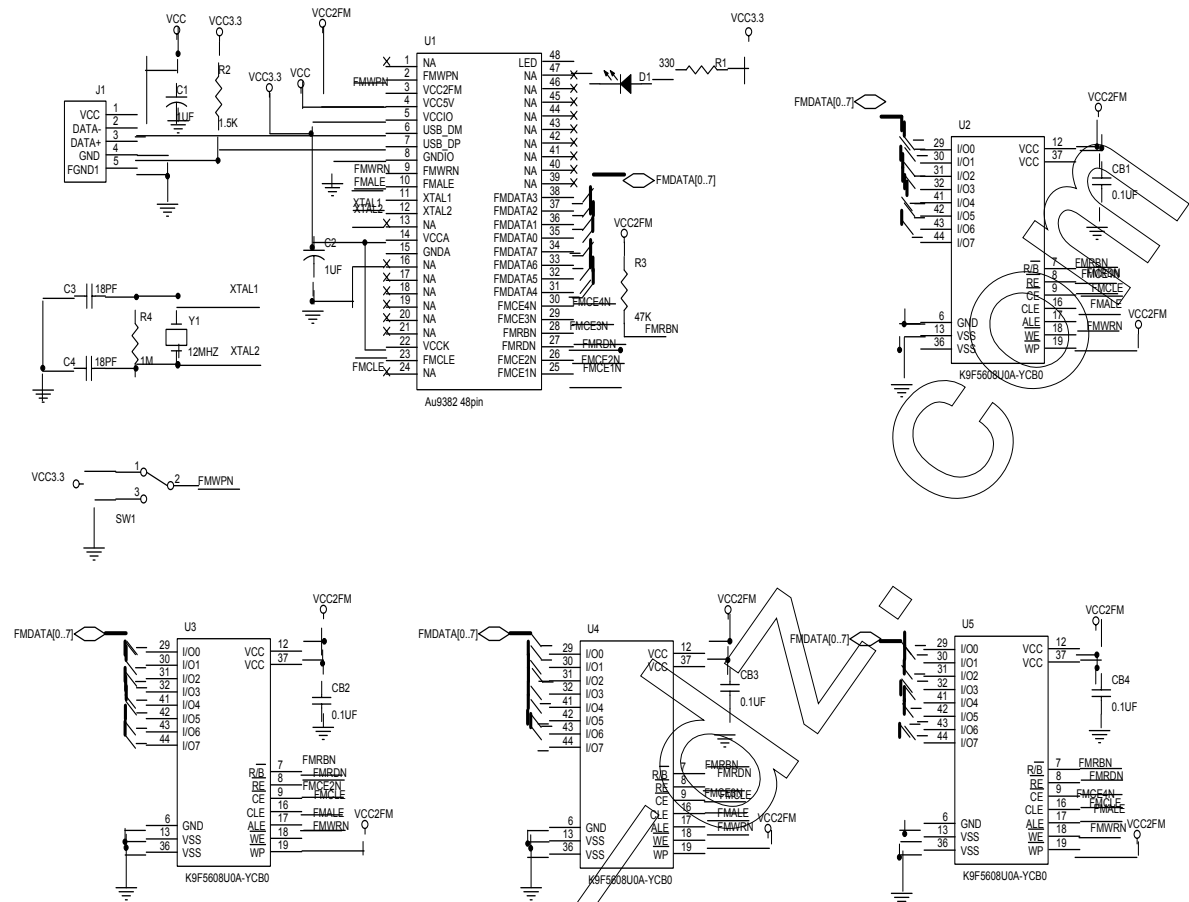


7.2. Pin Descriptions

Pin No.	Pin Name	Pin Type	Description
1	NA		NA
2	FMWPN	I	Connect to Flash Memory Write Protect
3	VCC2FM	O	Connect to Flash Memory Vcc
4	VCC5V	PWR	5V power supply
5	VCCIO	PWR	Regular 3.3V output/ IO 3.3V input
6	USB_DM	I/O	USB D-
7	USB_DP	I/O	USB D+
8	GNDIO	PWR	Ground
9	FMWRN	O	Connect to Flash Memory Write Enable
10	FMALE	O	Connect to Flash Memory Address Latch Enable
11	XTAL1	I	Crystal Oscillator Input (12MHz)
12	XTAL2	O	Crystal Oscillator Output (12MHz)
13	NA		NA
14	VCCA	PWR	Analog 3.3V input
15	GNDA	PWR	Ground
16	NA		
17	NA		
18	NA		
19	NA		
20	NA		
21	NA		
22	VCCK	PWR	Core 3.3V Input
23	FMCLE	O	Connect to Flash Memory Command Latch Enable
24	NA		
25	FMCE1N	O	Connect to Flash Memory Chip1 Enable
26	FMCE2N	O	Connect to Flash Memory Chip2 Enable
27	FMRDN	O	Connect to Flash Memory Read Enable
28	FMRBN	I	Connect to Flash Memory Ready/Busy
29	FMCE3N	O	Connect to Flash Memory Chip3 Enable
30	FMCE4N	O	Connect to Flash Memory Chip4 Enable
31	FMDATA4	I/O	Connect to Flash Memory Data4
32	FMDATA5	I/O	Connect to Flash Memory Data5
33	FMDATA6	I/O	Connect to Flash Memory Data6
34	FMDATA7	I/O	Connect to Flash Memory Data7

35	FMDATA0	I/O	Connect to Flash Memory Data0
36	FMDATA1	I/O	Connect to Flash Memory Data1
37	FMDATA2	I/O	Connect to Flash Memory Data2
38	FMDATA3	I/O	Connect to Flash Memory Data3
39	NA		NA
40	NA		NA
41	NA		NA
42	NA		NA
43	NA		NA
44	NA		NA
45	NA		NA
46	NA		NA
47	NA		NA
48	LED	O	General Purpose Out, used as activity LED

7.3 Schematics



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