

FEATURES

Low Input Offset Voltage 150 μV Max
Low Offset Voltage Drift, Over -55°C to $+125^{\circ}\text{C}$
 1.2 $\text{pV}/^{\circ}\text{C}$ Max
Low Supply Current (Per Amplifier) 725 μA Max
High Open-Loop Gain 5000 V/mV Min
Input Bias Current 3 nA Max
Low Noise Voltage Density 11 $\text{nV}/\sqrt{\text{Hz}}$ at 1 kHz
Stable With Large Capacitive Loads 10 nF Typ
Pin Compatible to LM148, HA4741, RM4156, and LT1014
 with Improved Performance
 Available in Die Form

GENERAL DESCRIPTION

The OP400 is the first monolithic quad operational amplifier that features OP77 type performance. Precision performance no longer has to be sacrificed to obtain the space and cost savings offered by quad amplifiers.

The OP400 features an extremely low input offset voltage of less than 150 μV with a drift of under 1.2 $\mu\text{V}/^{\circ}\text{C}$, guaranteed over the full military temperature range. Open-loop gain of the OP400 is over 5,000,000 into a 10 $\text{k}\Omega$ load, input bias current is under 3 nA , CMR is above 120 dB , and PSRR is below 1.8 $\mu\text{V}/\text{V}$. On-chip zener-zap trimming is used to achieve the low input offset voltage of the OP400 and eliminates the need for offset nulling. The OP400 conforms to the industry-standard quad pinout which does not have null terminals.

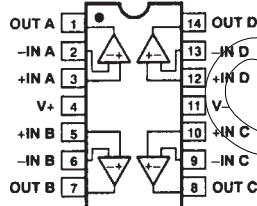
PIN CONNECTIONS

14-PIN CERAMIC DIP

(Y-Suffix)

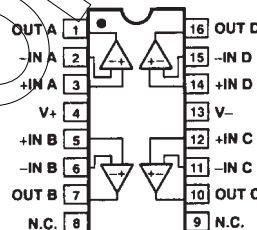
14-PIN PLASTIC DIP

(P-Suffix)



16-PIN SOIC

(S-Suffix)



The OP400 features low power consumption, drawing less than 725 μA per amplifier. The total current drawn by this quad amplifier is less than that of a single OP07, yet the OP400 offers significant improvements over this industry standard op amp. Voltage noise density of the OP400 is a low 11 $\text{nV}/\sqrt{\text{Hz}}$ at 10 Hz , which is half that of most competitive devices.

The OP400 is pin-compatible with the LM148, HA4741, RM4156, and LT1014 operational amplifiers and can be used to upgrade systems using these devices. The OP400 is an ideal choice for applications requiring multiple precision operational amplifiers and where low power consumption is critical.

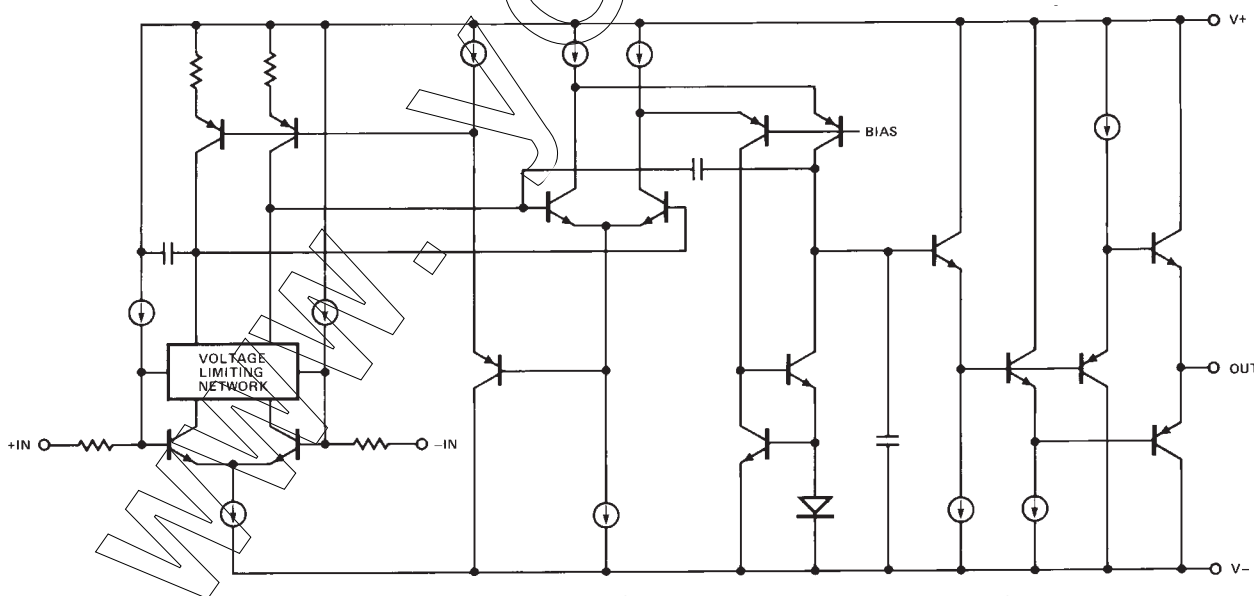


Figure 1. Simplified Schematic (One of Four Amplifiers Is Shown)

REV. C

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OP400—SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ $V_S = \pm 15\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.)

Parameter	Symbol	Conditions	OP400A/E			OP400F			OP400G/H			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{OS}		40		150	60		230	80		300	μV
Long-Term Input Voltage Stability			0.1			0.1			0.1			$\mu\text{V}/\text{mo}$
Input Offset Current	I_{OS}	$V_{CM} = 0\text{ V}$	0.1		1.0	0.1		2.0	0.1		3.5	nA
Input Bias Current	I_B	$V_{CM} = 0\text{ V}$	0.75		3.0	0.75		6.0	0.75		7.0	nA
Input Noise Voltage	$e_{n\text{ p-p}}$	0.1 Hz to 10 Hz	0.5			0.5			0.5			$\mu\text{V p-p}$
Input Noise Voltage Density ¹	e_n	$f_0 = 10\text{ Hz}^1$ $f_0 = 1000\text{ Hz}^1$	22 11	36 18		22 11	36 18		22 11			$\text{nV}/\sqrt{\text{Hz}}$
Input Noise Current	$i_{n\text{ p-p}}$	0.1 Hz to 10 Hz	15			15			15			pA p-p
Input Noise Current Density	i_n	$f_0 = 10\text{ Hz}$	0.6			0.6			0.6			$\text{pA}/\sqrt{\text{Hz}}$
Input Resistance Differential Mode	R_{IN}		10			10			10			M Ω
Input Resistance Common Mode	R_{INCM}		200			200			200			G Ω
Large Signal Voltage Gain	A_{VO}	$V_O = \pm 10\text{ V}$ $R_L = 10\text{ k}\Omega$ $R_L = 2\text{ k}\Omega$	5000 2000	12000 3500		3000 1500	7000 3000		3000 1500	7000 3000		V/mV
Input Voltage Range ³	IVR		± 12	± 13		± 12	± 13		± 12	± 13		V
Common Mode Rejection	CMR	$V_{CM} = 12\text{ V}$	120	140		115	140		110	135		dB
Power Supply Rejection Ratio	PSRR	$V_S = 3\text{ V}$ to 18 V	0.1	1.8		0.1	3.2		0.2	5.6		$\mu\text{V}/\text{V}$
Output Voltage Swing	V_O	$R_L = 10\text{ k}\Omega$ $R_L = 2\text{ k}\Omega$	± 12 ± 11	± 12.6 ± 12.2		± 12 ± 11	± 12.6 ± 12.2		± 12 ± 11	± 12.6 ± 12.2		V
Supply Current Per Amplifier	I_{SY}	No Load	600	725		600	725		600	725		μA
Slew Rate	SR		0.1	0.15		0.1	0.15		0.1	0.15		V/ μs
Gain Bandwidth Product	GBWP	$A_V = 1$	500			500			500			kHz
Channel Separation	CS	$V_O = 20\text{ V p-p}$ $f_0 = 10\text{ Hz}^2$	123	135		123	135		123	135		dB
Input Capacitance	C_{IN}		3.2			3.2			3.2			pF
Capacitive Load Stability		$A_V = 1$ No Oscillations	10			10			10			nF

NOTES

¹Sample tested

²Guaranteed but not 100% tested.

³Guaranteed by CMR test

SPECIFICATIONS (continued)

ELECTRICAL CHARACTERISTICS (@ $V_S = \pm 15\text{ V}$, $-55^\circ\text{C} \leq T_A = 125^\circ\text{C}$ for OP400A, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Offset Voltage	V_{OS}			70	270	μV
Average Input Offset Voltage Drift	TCV_{OS}			0.3	12	$\mu\text{V}/^\circ\text{C}$
Input Offset Current	I_{OS}	$V_{CM} = 0\text{ V}$		0.1	2.5	nA
Input Bias Current	I_B	$V_{CM} = 0\text{ V}$		1.3	5.0	nA
Large Signal Voltage Gain	A_{VO}	$V_O = \pm 10\text{ V}$ $R_L = 10\text{ k}\Omega$ $R_L = 2\text{ k}\Omega$	3000 1000	9000 2300		V/mV
Input Voltage Range*	IVR		± 12	± 12.5		V
Common Mode Rejection	CMR	$V_{CM} = \pm 12\text{ V}$	115	130		dB
Power Supply Rejection Ratio	PSRR	$V_O = 3\text{ V}$ to 18 V		0.2	3.2	$\mu\text{V}/\text{V}$
Output Voltage Swing	V_O	$R_L = 10\text{ k}\Omega$ $R_L = 2\text{ k}\Omega$	± 12 ± 11	± 12.4 ± 12		V
Supply Current Per Amplifier	I_{SY}	No Load		600	775	μA
Capacitive Load Stability		$A_V = 1$ No Oscillations		8		nF

NOTE

*Guaranteed by CMR test

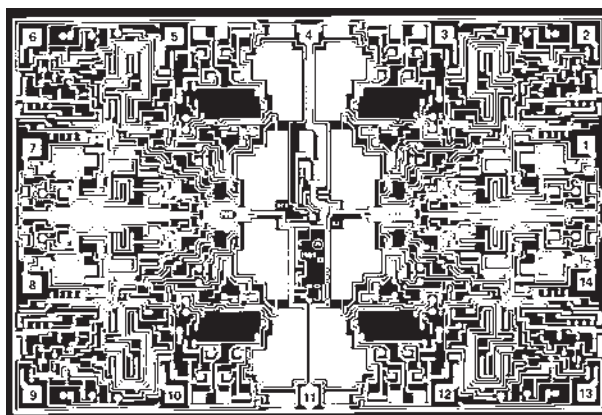
ELECTRICAL CHARACTERISTICS (@ $V_S = \pm 15\text{ V}$, $-25^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ for OP400E/F, $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ for OP400G, $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ for OP400H, unless otherwise noted.)

Parameter	Symbol	Conditions	OP400A/E			OP400F			OP400G/H			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{OS}		60		220	80		350	110		400	μV
Average Input Offset Voltage Drift	TCV_{OS}		0.3		1.2	0.3		2.0	0.6		2.5	$\mu\text{V}/^\circ\text{C}$
Input Offset Current	I_{OS}	$V_{CM} = 0\text{ V}$ E, F, G Grades H Grade	0.1		2.5	0.1		3.5	0.2 0.2		6.0 12.0	nA
Input Bias Current	I_B	$V_{CM} = 0\text{ V}$ E, F, G Grades H Grade	0.1		2.5	0.1		3.5	1.0 1.0		12.0 20.0	nA
Large-Signal Voltage Gain	A_{VO}	$V_{CM} = 0\text{ V}$ $R_L = 10\text{ k}\Omega$ $R_L = 2\text{ k}\Omega$	3000 1500	10000 2700		2000 1000	5000 2000		2000 1000	5000 2000		V/mv
Input Voltage Range	IVR	*	± 12	± 12.5		± 12	± 12.5		± 12	± 12.5		V
Common-Mode Rejection	CMR	$V_{CM} = \pm 12\text{ V}$	115	135		110	135		105	130		dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3\text{ V}$ to $\pm 18\text{ V}$		0.15	3.2		0.15	5.6		0.3	10.0	$\mu\text{V}/\text{V}$
Output Voltage Swing	V_O	$R_L = 10\text{ k}\Omega$ $R_L = 2\text{ k}\Omega$	± 12 ± 11	± 12.4 ± 12		± 12 ± 11	± 12.4 ± 12		± 12 ± 11	± 12.6 ± 12.2		V
Supply Current Per Amplifier	I_{SY}	No Load	600		775	600		775	600		775	μA
Capacitive Load Stability		No Oscillations	10			10			10			nF

NOTE

*Guaranteed by CMR test.

DICE CHARACTERISTICS



DIE SIZE 0.181 × 0.123 inch, 22,263 sq. mils
(4.60 × 3.12 mm, 14.35 sq. mm)

- | | |
|----------|-----------|
| 1. OUT A | 8. OUT C |
| 2. -IN A | 9. -IN C |
| 3. +IN A | 10. +IN C |
| 4. V+ | 11. V- |
| 5. +IN B | 12. +IN D |
| 6. -IN B | 13. -IN D |
| 7. OUT B | 14. OUT D |

WAFER TEST LIMITS (@ $V_S = \pm 15$ V, $T_A = 25^\circ\text{C}$, unless otherwise noted.)

Parameter	Symbol	Conditions	OP400GBC Limit	Unit
Input Offset Voltage	V_{OS}		230	μA Max
Input Offset Current	V_{OS}	$V_{CM} = 0$ V	2	nA Max
Input Bias Current	I_B	$V_{CM} = 0$ V	6	nA Max
Large Signal Voltage Gain	A_{VO}	$V_O = \pm 10$ V $R_L = 10$ k Ω $R_L = 2$ k Ω	3000 1500	V/mV Min
Input Voltage Range*	IVR	*	± 12	V Min
Common Mode Rejection	CMR	$V_{CM} = \pm 12$ V	115	dB Min
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3$ V to ± 18 V	3.2	$\mu\text{V/V}$ Max
Output Voltage Swing	V_O	$R_L = 10$ k Ω $R_L = 2$ k Ω	± 12 ± 11	V Min
Supply Current Per Amplifier	I_{SY}	No Load	725	μA Max

NOTE

*Guaranteed by CMR test.

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±20 V
Differential Input Voltage	±30 V
Input Voltage	Supply Voltage
Output Short-Circuit Duration	Continuous
Storage Temperature Range	
P, Y Package	−65°C to +150°C
Lead Temperature Range (Soldering 60 sec)	300°C
Junction Temperature (T _J)	−65°C to +150°C
Operating Temperature Range	
OP400A	−55°C to +125°C
OP400E, OP400F	−25°C to +85°C
OP400G	0°C to 70°C
OP400H	−40°C to +85°C

Package Type	θ_{JA}^1	θ_{IC}	Units
14-Pin Ceramic DIP (Y)	94	10	°C/W
14-Pin Plastic DIP (P)	76	33	°C/W
16-Pin SOIC (S)	88	23	°C/W

NOTES

- θ_{JA} is specified for worst-case mounting conditions, i.e., θ_{JA} is specified for device in socket for TO, Cerdip, and PDIP packages; θ_{JA} is specified for device soldered to printed circuit board for SOIC package.
- Absolute maximum ratings apply to both dice and packaged parts, unless otherwise noted.

ORDERING INFORMATION

T _A = 25°C V _{OS} Max (mV)	Package		Die	Operating Temperature Range
	CERDIP 14-Lead	Plastic		
150	OP400AY		OP400GBC	MIL
150	OP400EY			IND
230	OP400FY			IND
300		OP400GP		COM
300		OP400GS		COM
300		OP400GS-REEL		COM
300		OP400HP		XIND
300		OP400HS		XIND

NOTE

Burn-in is available on commercial and industrial temperature range parts in CERDIP, PDIP, and TO-can packages.

For Military processed devices, please refer to the standard microcircuit drawing (SMD) available at www.dscc.dla.mil/programs/milspec/default.asp

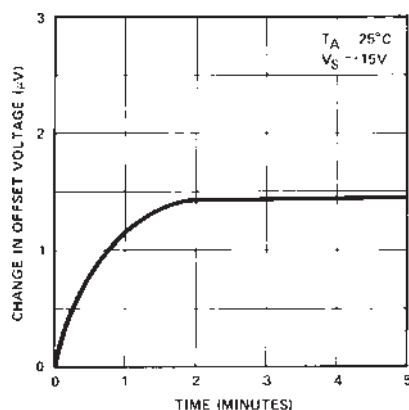
SMD Part Number	ADI Equivalent
5962-8777101M3A	OP400ATCMDA
5962-8777101MCA	OP400AYMDA

CAUTION

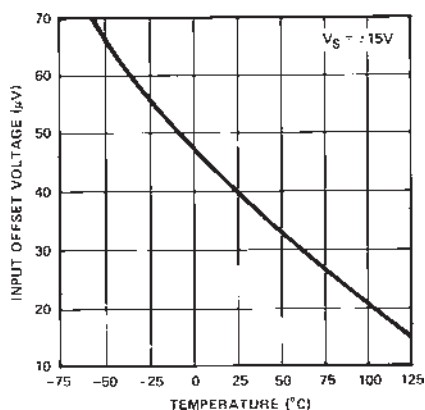
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the OP400 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



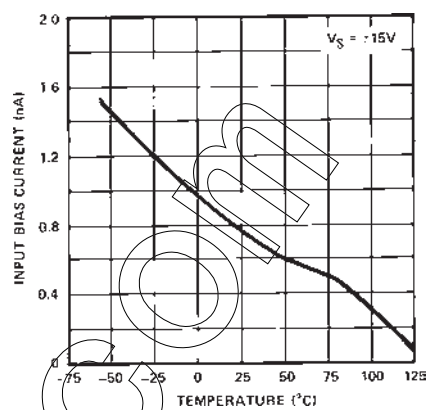
OP400—Typical Performance Characteristics



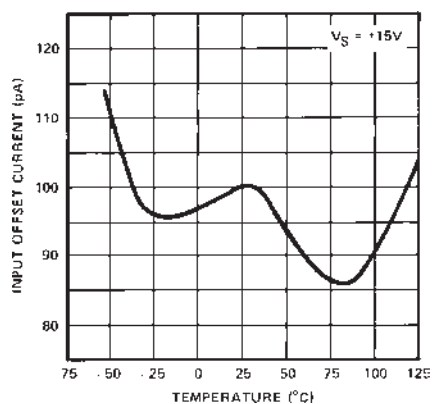
TPC 1. Warm-Up Drift



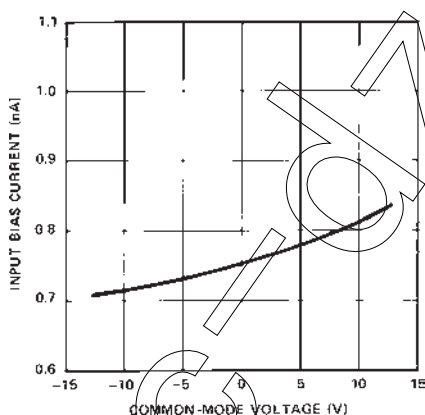
TPC 2. Input Offset Voltage vs. Temperature



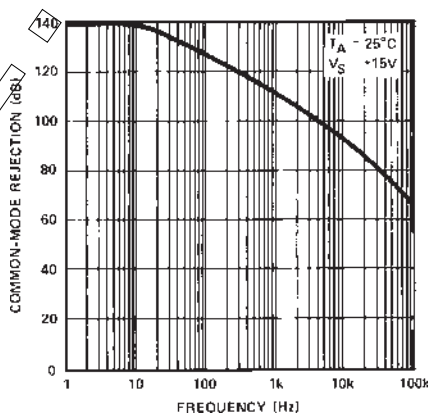
TPC 3. Input Bias Current vs. Temperature



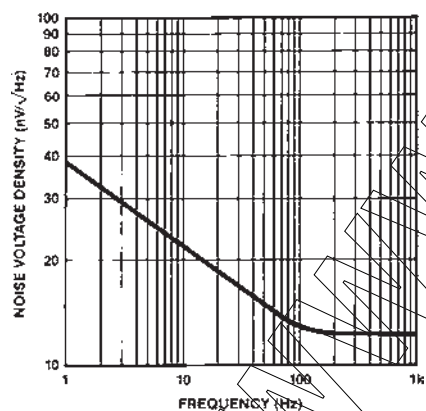
TPC 4. Input Offset Current vs. Temperature



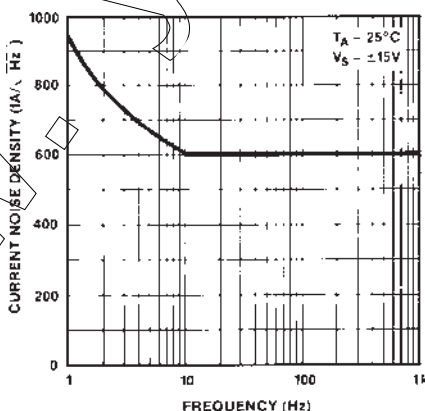
TPC 5. Input Bias Current vs. Common-Mode Voltage



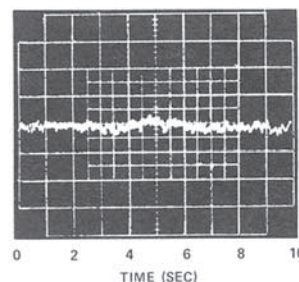
TPC 6. Common-Mode Rejection vs. Frequency



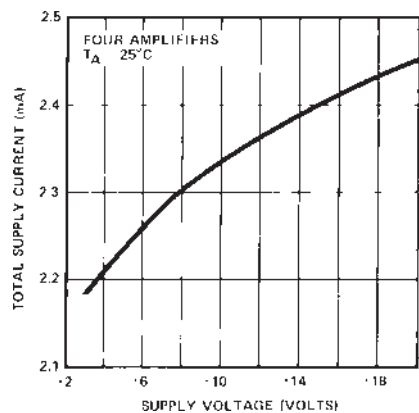
TPC 7. Noise Voltage Density vs. Frequency



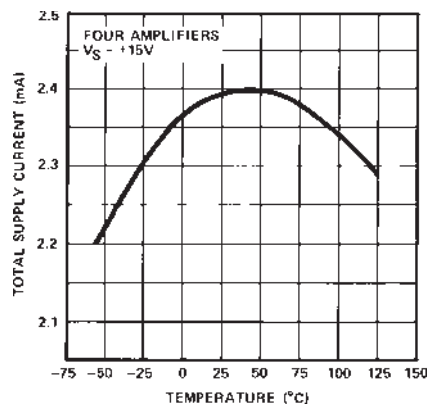
TPC 8. Current Noise Density vs. Frequency



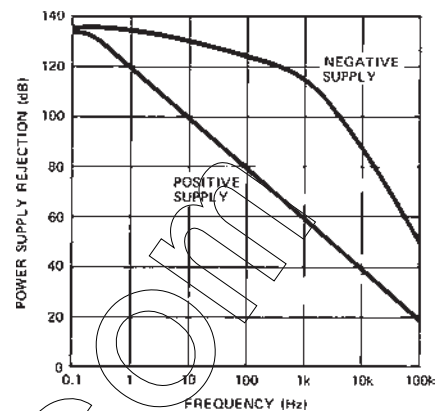
TPC 9. 0.1 Hz to 10 Hz Noise



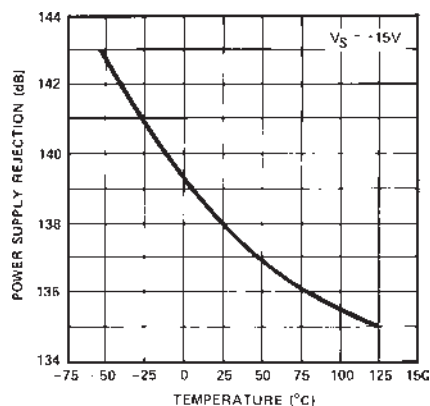
TPC 10. Total Supply Current vs. Supply Voltage



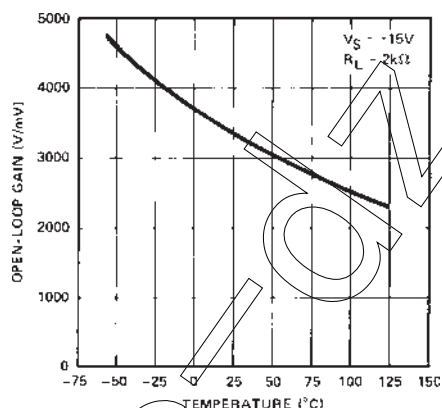
TPC 11. Total Supply Current vs. Temperature



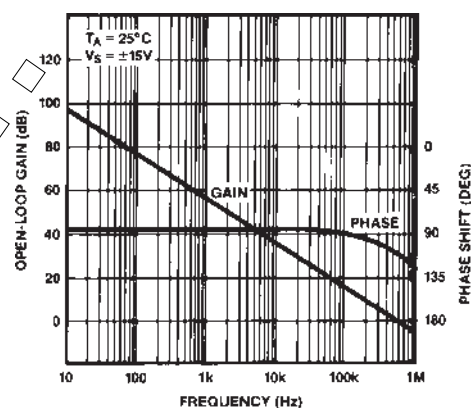
TPC 12. Power Supply Rejection vs. Frequency



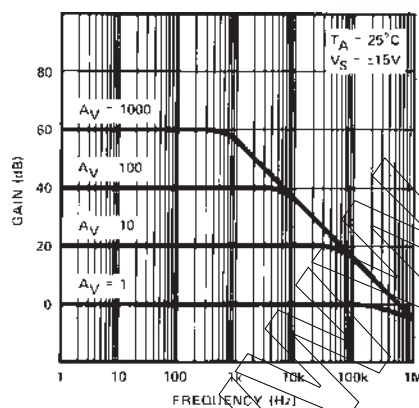
TPC 13. Power Supply Rejection vs. Temperature



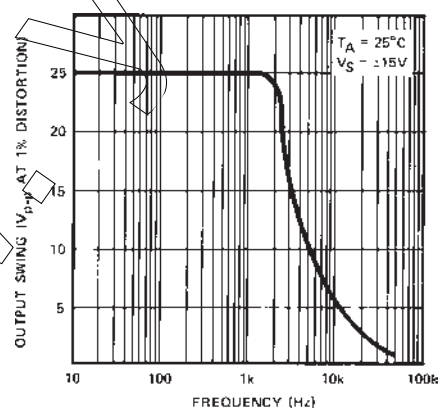
TPC 14. Open-Loop Gain vs. Temperature



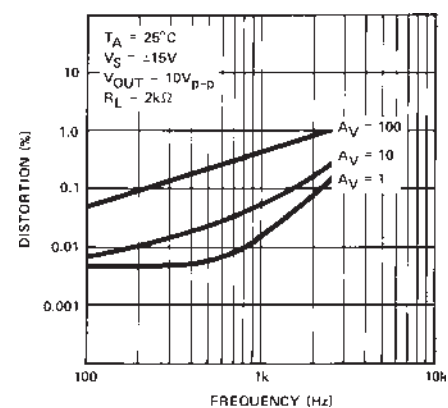
TPC 15. Open-Loop Gain and Phase Shift vs. Frequency



TPC 16. Closed-Loop Gain vs. Frequency

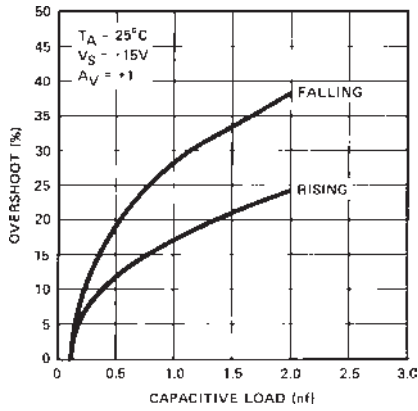


TPC 17. Maximum Output Swing Frequency

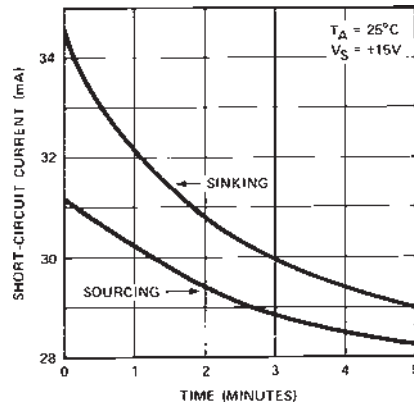


TPC 18. Total Harmonic Distortion vs. Frequency

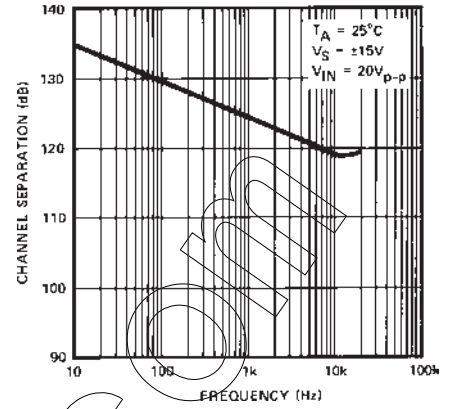
OP400



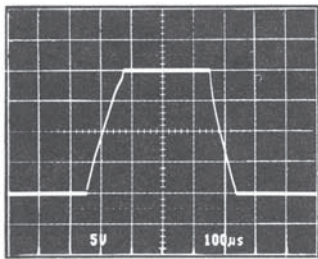
TPC 19. Overshoot vs. Capacitive Load



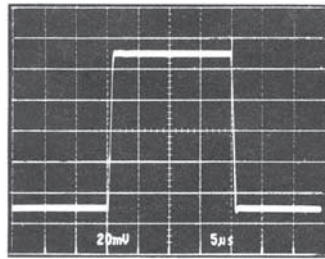
TPC 20. Short Circuit vs. Time



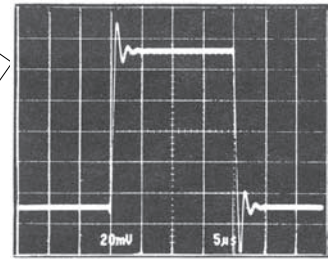
TPC 21. Channel Separation vs. Frequency



TPC 22. Large-Signal Transient Response



TPC 23. Small-Signal Transient Response



TPC 24. Small-Signal Transient Response $C_{LOAD} = 1\text{ nF}$

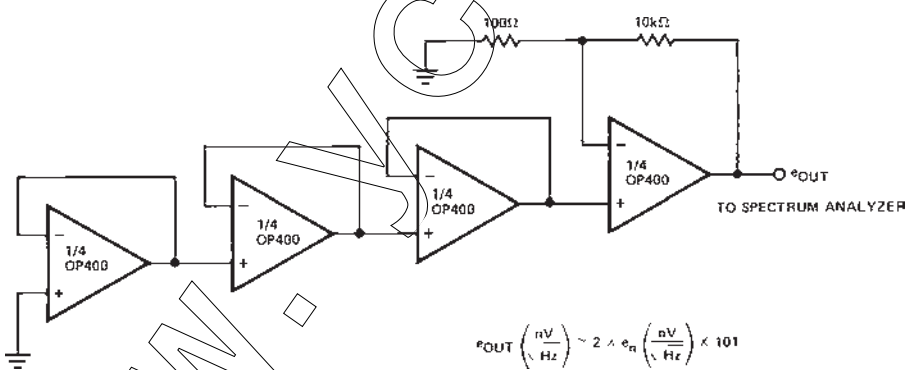


Figure 2. Noise Test Schematic

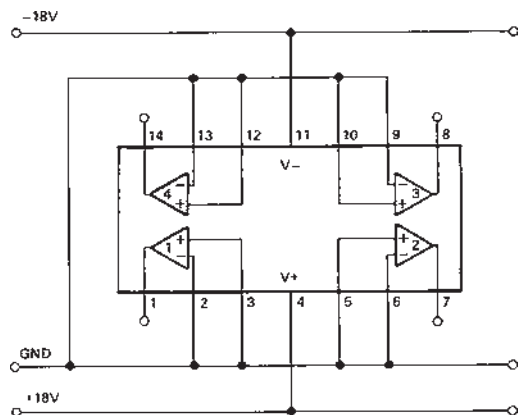


Figure 3. Burn-In Circuit

APPLICATIONS INFORMATION

The OP400 is inherently stable at all gains and is capable of driving large capacitive loads without oscillating. Nonetheless, good supply decoupling is highly recommended. Proper supply decoupling reduces problems caused by supply line noise and improves the capacitive load driving capability of the OP400.

Total supply current can be reduced by connecting the inputs of an unused amplifier to $-V$. This turns the amplifier off, lowering the total supply current.

APPLICATIONS

Dual Low-Power Instrumentation Amplifier

A dual instrumentation amplifier that consumes less than 33 mW of power per channel is shown in Figure 1. The linearity of the instrumentation amplifier exceeds 16 bits in gains of 5 to 200 and is better than 14 bits in gains from 200 to 1000. CMRR is above 115 dB ($G = 1000$). Offset voltage drift is typically $0.4 \mu\text{V}/^\circ\text{C}$ over the military temperature range which is comparable to the best monolithic instrumentation amplifiers. The bandwidth of the low-power instrumentation amplifier is a function of gain and is shown in Table I.

Table I. Gain Bandwidth

Gain	Bandwidth
5	150 kHz
10	67 kHz
100	7.5 kHz
1000	500 Hz

The output signal is specified with respect to the reference input, which is normally connected to analog ground. The reference input can be used to offset the output from -10 V to $+10 \text{ V}$ if required.

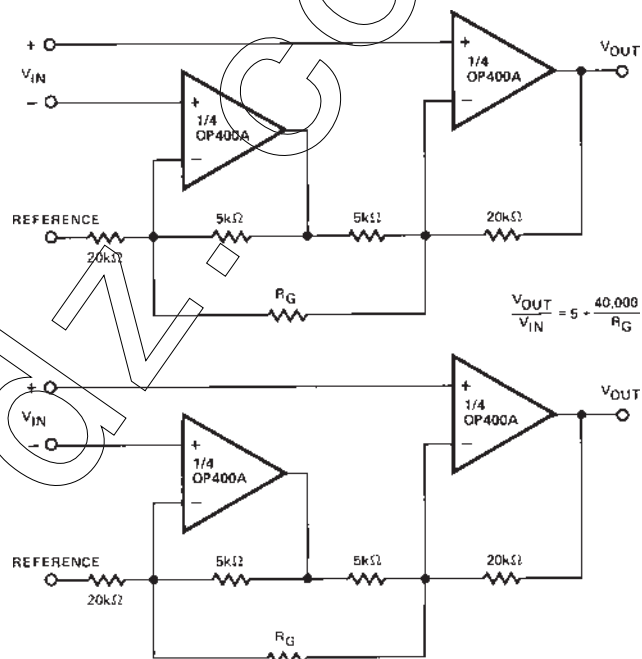


Figure 4. Dual Low Power Instrumentation Amplifier

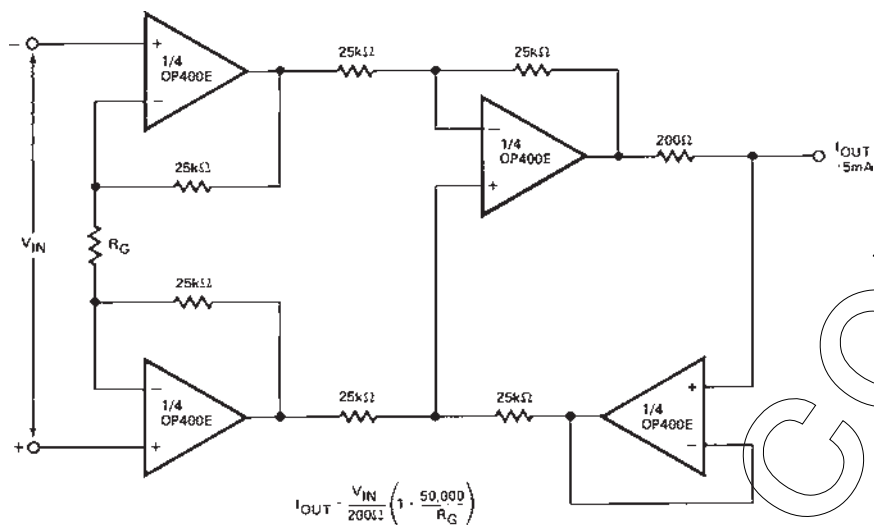


Figure 5. Bipolar Current Transmitter

BIPOLAR CURRENT TRANSMITTER

In the circuit of Figure 5, which is an extension of the standard three op amp instrumentation amplifier, the output current is proportional to the differential input voltage. Maximum output current is ± 5 mA with voltage compliance equal to ± 10 V when using ± 15 V supplies. Output impedance of the current transmitter exceeds $3 \text{ M}\Omega$ and linearity is better than 16 bits with gain set for a full scale input of $\pm 100 \mu\text{V}$.

DIFFERENTIAL OUTPUT INSTRUMENTATION AMPLIFIER

The output voltage swing of a single-ended instrumentation amplifier is limited by the supplies, normally at ± 15 V, to a maximum of 24 V p-p. The differential output instrumentation amplifier of Figure 6 can provide an output voltage swing of 48 V p-p when operated with ± 15 V supplies. The extended output swing is due to the opposite polarity of the outputs. Both outputs will swing 24 V p-p but with opposite polarity, for a total output voltage swing of 48 V p-p. The reference input can be used to set a common-mode output voltage over the range ± 10 V. PSRR of the amplifier is less than $1 \mu\text{V}/\text{V}$ with CMRR ($G = 1000$) better than 115 dB. Offset voltage drift is typically $0.4 \mu\text{V}/^\circ\text{C}$ over the military temperature range.

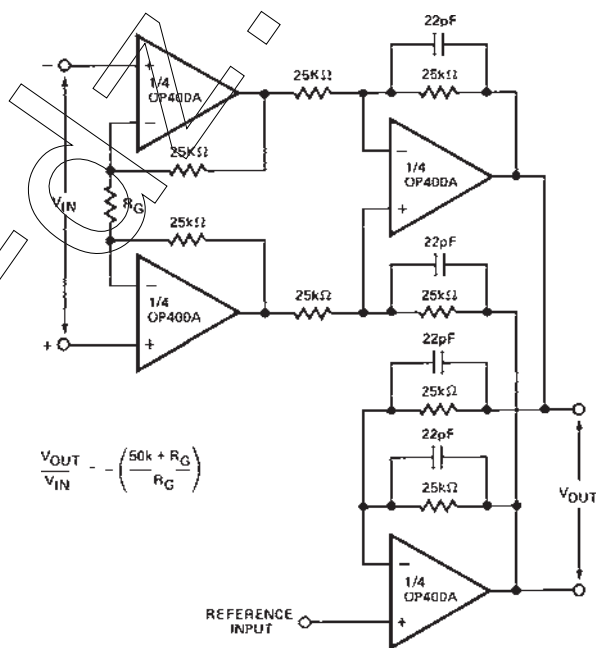


Figure 6. Differential Output Instrumentation Amplifier

MULTIPLE OUTPUT TRACKING VOLTAGE REFERENCE

Figure 7 shows a circuit that provides outputs of 10 V, 7.5 V, 5 V, and 2.5 V for use as a system voltage reference. Maximum output current from each reference is 5 mA with load regulation

under 25 $\mu\text{V}/\text{mA}$. Line regulation is better than 15 $\mu\text{V}/\text{V}$ and output voltage drift is under 20 $\mu\text{V}/^\circ\text{C}$. Output voltage noise from 0.1 Hz to 10 Hz is typically 75 μV p-p from the 10 V output and proportionately less from the 7.5 V, 5 V, and 2.5 V outputs.

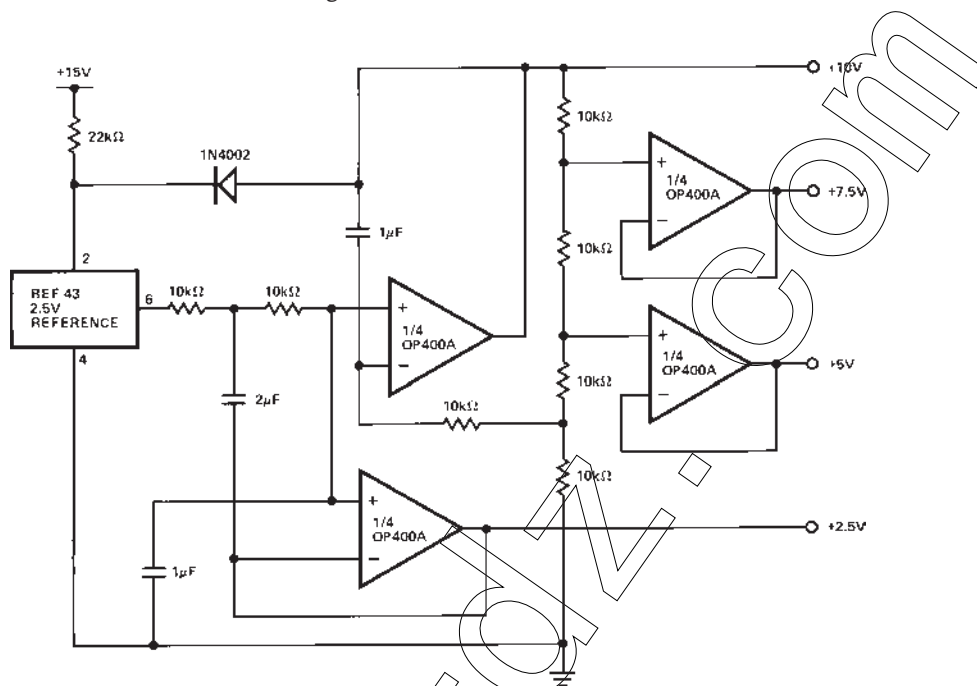
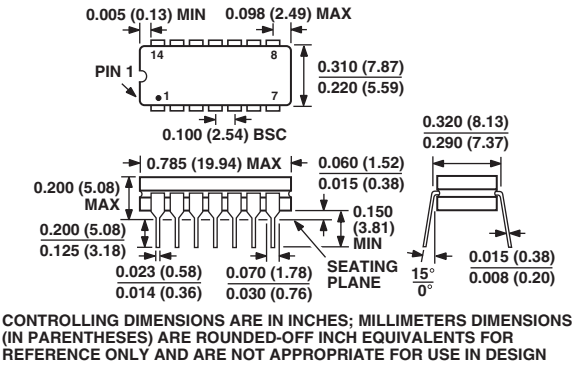


Figure 7. Multiple-Output Tracking Voltage Reference

OUTLINE DIMENSIONS

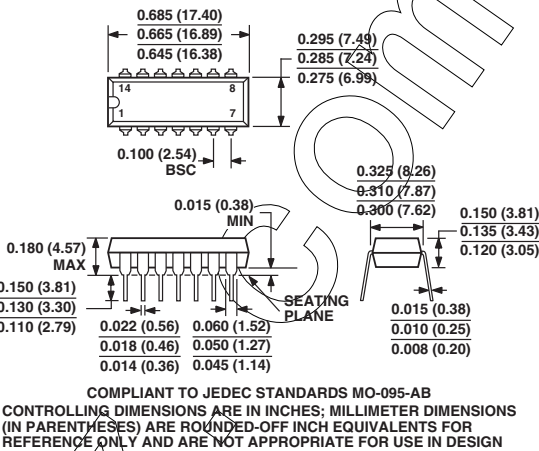
14-Lead Ceramic Dual In-Line Package [CERDIP]
(Q-14)
[Y-Suffix]

Dimensions shown in inches and (millimeters)



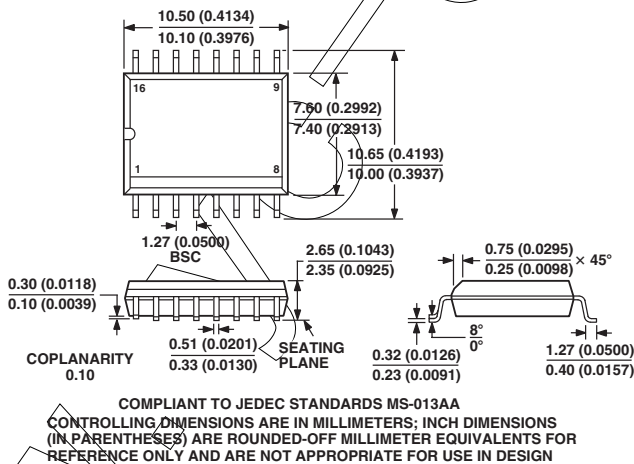
14-Lead Plastic Dual In-Line Package [PDIP]
(N-14)
[P-Suffix]

Dimensions shown in inches and (millimeters)



16-Lead Standard Small Outline Package [SOIC]
Wide Body
(R-16)
[S-Suffix]

Dimensions shown in millimeters and (inches)



Revision History

Location	Page
6/03—Data Sheet changed from REV. B to REV. C.	
Edits to SPECIFICATIONS	2
10/02—Data Sheet changed from REV. A to REV. B.	
Addition of ABSOLUTE MAXIMUM RATINGS	5
Edits to OUTLINE DIMENSIONS	12
4/02—Data Sheet changed from REV. 0 to REV. A.	
Edits to FEATURES	1
Edits to ORDERING INFORMATION	1
Edits to PIN CONNECTIONS	1
Edits to GENERAL DESCRIPTIONS	1, 2
Edits to PACKAGE TYPE	2