PAS5101CS CMOS 1.3MEGA DIGITAL IMAGE SESNSOR

General Description

The PAS5101CS is a highly integrated CMOS active-pixel image sensor that has resolution of 1280(H) x 1024 (V). To have an excellent image quality, the PAS5101CS output 10-bits RGB raw data though a parallel data bus. It is available in 24-pin CSP.

The PAS5101CS can be programmed to set the exposure time for different luminance condition via I2C™ serial control bus. By programming the internal register sets, it performs on-chip frame rate adjustment, offset correction DAC, programmable gain control, 10-bits ADC, 10-bits output companding, interpolated sub-sampling and defect compensation.

Features

- 1.3Mega resolution, ~1/3" Lens.
- Bayer RGB color filter array.
- 10-bits parallel RGB raw data output.
- On-Chip 10-bits pipeline A/D converter.
- On-Chip programmable gain amplifier
  - 4-bits color gain amplifier.
  - 4-bits global gain amplifier.
- Digital gain stage.
- Continuous variable frame time.
- Continuous variable exposure time.
- I2C™ interface.
- 20mA power dissipation (15fps / 2.5v).
- < 10uA low power-down dissipation.
- Window-of-Interest (WOI).
- Sub-sampling.
- Defect compensation.
- Lens shading compensation.
- Pin-to-pin compatible to OV9640.

Key Specification

Supply Voltage	2.5v ~ 3.3v
Resolution	1280 (H) x 1024 (V)
Array Diagonal	5.9mm (~1/3" Optic)
Pixel Size	3.6 μm x 3.6 μm
Max. Frame Rate	~15 fps @ 1.3Mega
Max. System Clock	Up to 48MHz
Max. Pixel Clock	Up to 24MHz
Color Filter	RGB Bayer Pattern
Exposure Time	~ Frame time to Line time
Scan Mode	Progressive
Sensitivity	TBD
S/N Ratio	TBD
Chief Ray Angle	20° ~ 24°
Package Type	24-pin CSP

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1. Pin Assignment

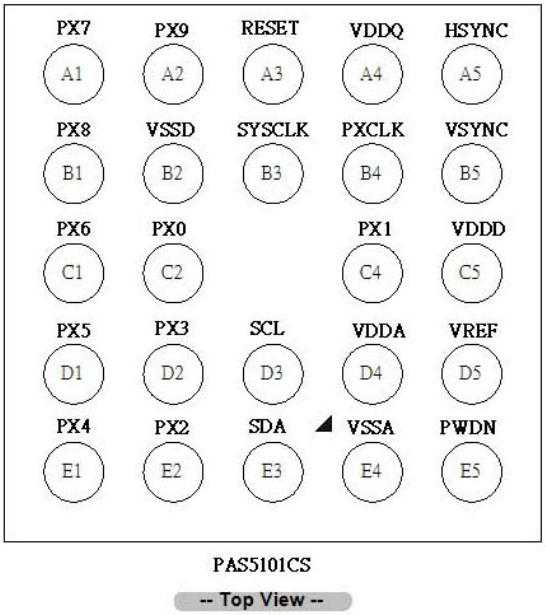

Figure 1.1 Shows the PAS5101CS pin diagram

Pin No.	Name	Type	Description
E4	VSSA	GND	Analog ground.
D4	VDDA	PWR	Analog power, 2.5V
E5	PWDN	IN	Power Down (chip power down if high).
D5	VREF	IN	Internal voltage reference.
C5	VDDD	PWR	Nc, Internal Regulator 1.8V.
B5	VSYNC	OUT	Vertical synchronization signal.
A5	HSYNC	OUT	Horizontal synchronization signal.
B4	PXCLK	OUT	Pixel clock output.
A4	VDDQ	PWR	Sensor VDD, 2.5V ~ 3.3V.
B3	SYSCLK	IN	System clock input.
A3	RESET	IN	Resets all registers to their default values (chip reset if high .)
B2	VSSD	GND	Digital ground.
A2	PX9	OUT	Digital data out.
B1	PX8	OUT	Digital data out.
A1	PX7	OUT	Digital data out.
C1	PX6	OUT	Digital data out.
D1	PX5	OUT	Digital data out.
E1	PX4	OUT	Digital data out.
D2	PX3	OUT	Digital data out.
E2	PX2	OUT	Digital data out.
C4	PX1	OUT	Digital data out.

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C2	PX0	OUT	Digital data out.
D3	SCL	IN	I2C clock.
E3	SDA	I/O	I2C data. Internal pull high resister is 10KΩ.

2. Sensor Array Format & Output Timing

2.1. Physical Sensor Array Format

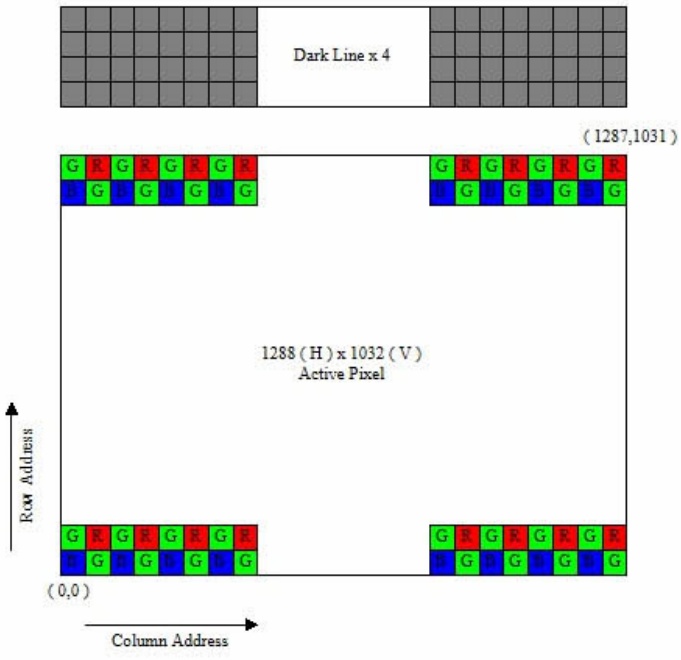

Figure 2.1 Physical Sensor Array Format

2.2. Output Timing

1.3Mega mode (1288 x 1032) pixel readout:

H_Start[9:0] = 0, V_Start[8:0] = 0, H_Size[9:0] = 1287, V_Size[8:0]= 1035,

LPF[7:0] = 1035, Nov_Size_By4[7:0] = 63,

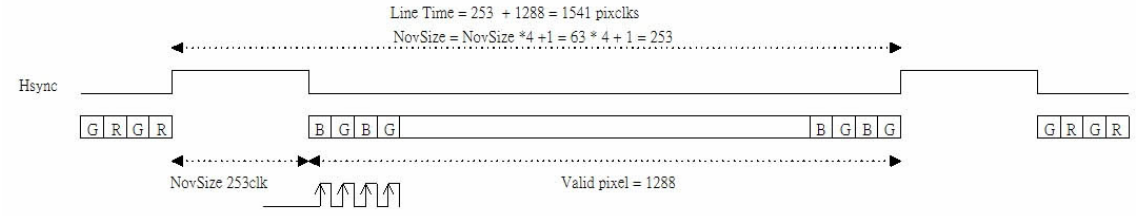

Figure 2.2 Inter-line timing

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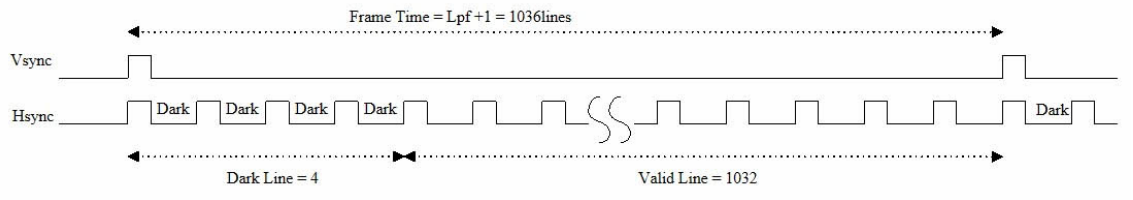

Figure 2.3 Inter-frame timing

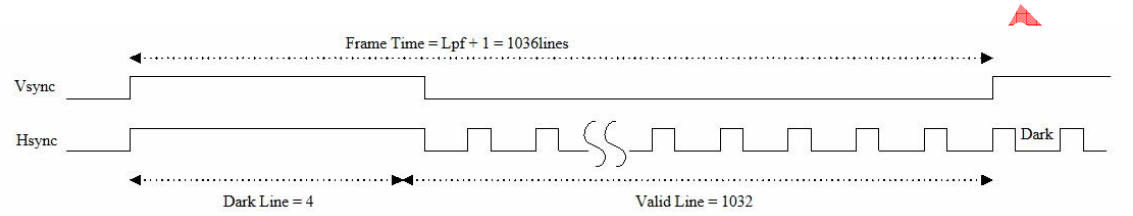

Figure 2.4 Inter-frame timing @ Dark masked

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3. Block Diagram & Function Description

3.1. Block Diagram

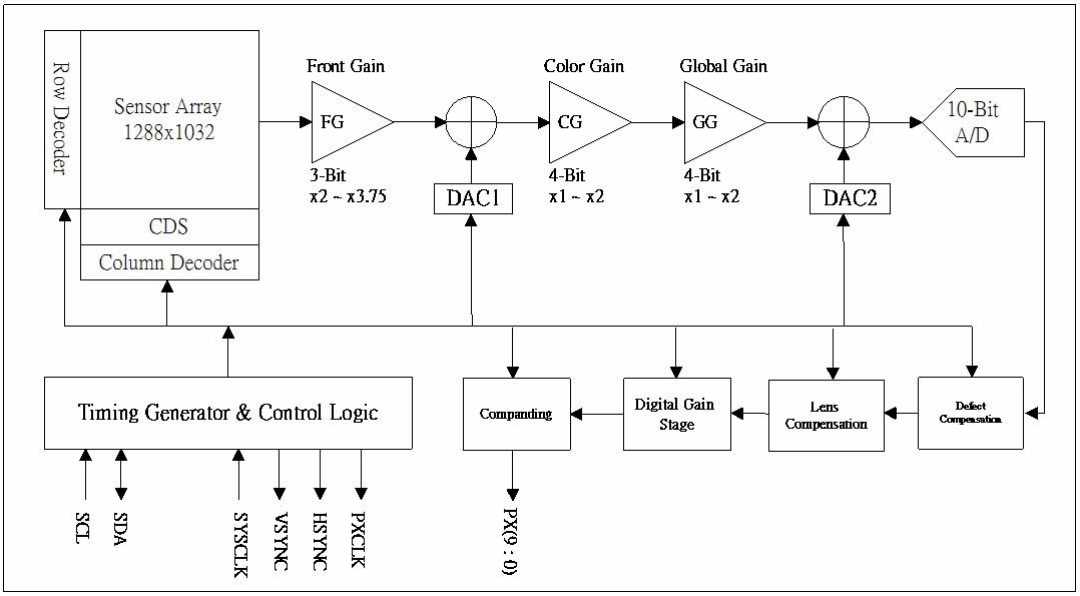

Figure 3.1 Shows the PAS5101CS sensor block diagram

The PAS5101CS is a 1/3" CMOS imaging sensor with 1280 (H) x 1024 (V) physical pixels. The active region of sensor array is 1288 (H) x 1032 (V) as shown in Figure 3.1. The sensor array is cover with Bayer pattern color filters and μ-lens. The first pixel location (0,0) is programmable in 2 direction (X and Y) and the default value is at the left-down side of sensor array.

After a programmable exposure time, the image is sampled first with CDS (Correlated Double Sampling) block to improve S/N ration and reduce fixed pattern noise.

Three analog gain stages are implemented before signal transferred by the 10-bits A/D converter. The front gain stage (FG) can be programmed to fit the saturation level of sensor to the full-range input of ADC. The programmable color gain stage (CG) is used to balance the luminance response difference between B/G/R. The global gain stage (GG) is programmed to adapt the gain to the image luminance.

The fine gained signal will be digitized by the on-chip 10-bits A/D converter. After the image data has been digitized, further alteration to the signal can be applied before the data is output.

3.2. Defect Compensation

The defect compensation block can detect the possible defect pixel and replace it with average output of like-colored pixels on either side of defective pixel. There is no limitation in the capability of defect number. This function is also Enable / Disable by user.

3.3. Companding Curves

The companding function is used to simulate the gamma curve and do non-linear transformation before the data is output. There are 4 curves selected by setting register Compand_Sel as shown in Figure 3.2 and this function is also Enable / Disable by user.

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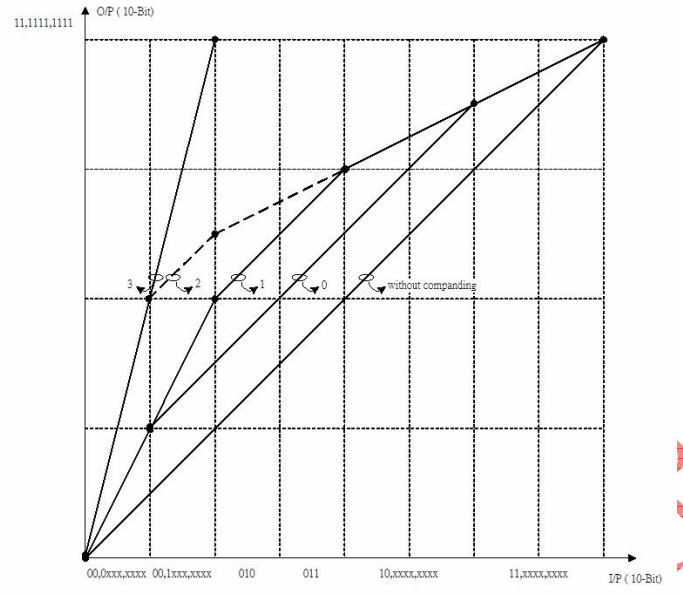

Figure 3.2 Companding curves program by Compand_EnH and Compand_Sel

3.4. Power Down Mode

The PAS5101CS can be power down by setting register "SW_PwrDn" or by enable PWDN pin. PAS5101CS supports two power down modes :

- Software Power Down : Set register "SW_PwrDn" = 0x01 to power down all the internal block except I2C™.
- Hardware Power Down : Pull PWDN pin to high to power down the chip. The chip will go into standby mode.

3.5. Reset Mode

The PAS5101CS can be reset by setting "SW_Reset" or by enable Reset pin. PAS5101CS supports two reset modes :

- Software Reset : Set register "SW_Reset" = 0x01 to reset all the I2C™ registers. It's only reset the register value not reset full chip.
- HardwareReset : Pull Reset pin to high to reset the full chip.

3.6. Window-of-Interest (WOI)

Users are allowed to define window size as well as window location in PAS5101CS. The location of window can be anywhere in the pixel array. Window size and window location is defined by register "H_Start", "V_Start", "V_Size" and "H_Size"; The "H_Start" defines the starting column while "V_Start" defines the starting rom of the window; The "H_Size" define the column width of the window and "V_Size" defines the row depth of the window.

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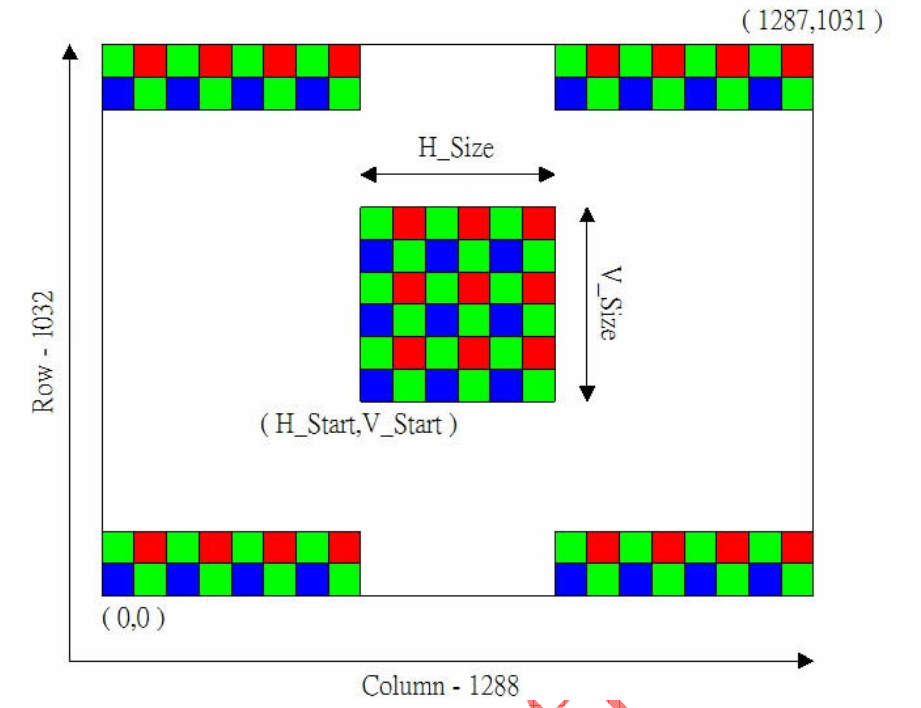

Figure 3.3

3.7.1. Output timing of WOI

Hardware windowing VGA (640x480) pixels readout (With 4 dark lines):

H_Start[9:0] = 0, V_Start[8:0] = 0, H_Size[9:0] = 639, V_Size[8:0]= 483,
LPF[7:0] = 483, Nov_Size_By4[7:0] = 63,

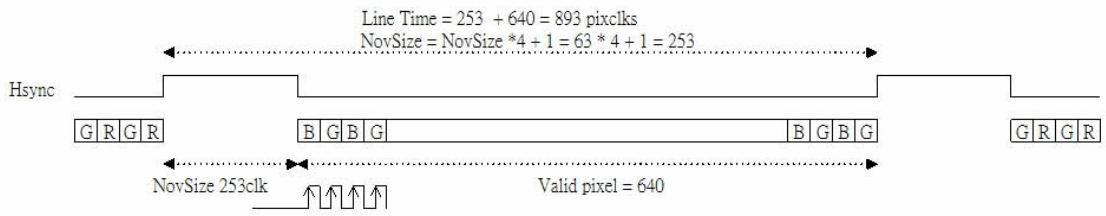

Figure 3.4 Inter-line timing of W.O.I

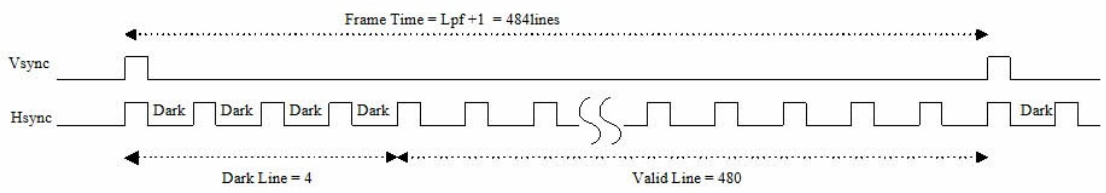

Figure 3.5 Inter-frame timing of W.O.I

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3.7. Sub-Sampling

PAS5101CS can be programmed to output image in VGA、 QVGA and QQVGA size. In the VGA sub-sampling mode, both vertical and horizontal pixels are sub-sampling at 1/2; In QVGA sub-sampling mode, both vertical and horizontal pixels are sub-sampling at 1/4; While in QQVGA sub-sampling mode, sub-sampling at 1/8. By programming Skip_Analog and Skip_Digital, The maximum sub-sampling rate is 1/32 (Skip_Analog + Skip_Digital).

3.7.1. Skip_Analog

Sub-sampling (Skip_Analog) to VGA (640x480) pixels readout (With 4 dark lines):

H_Start[9:0] = 0, V_Start[8:0] = 0, H_Size[9:0] = 1287, V_Size[8:0]= 1035,
LPF[7:0] = 519, Nov_Size_By4[7:0] = 63, Skip_Analog = 1 (sub-sampling 1/2)

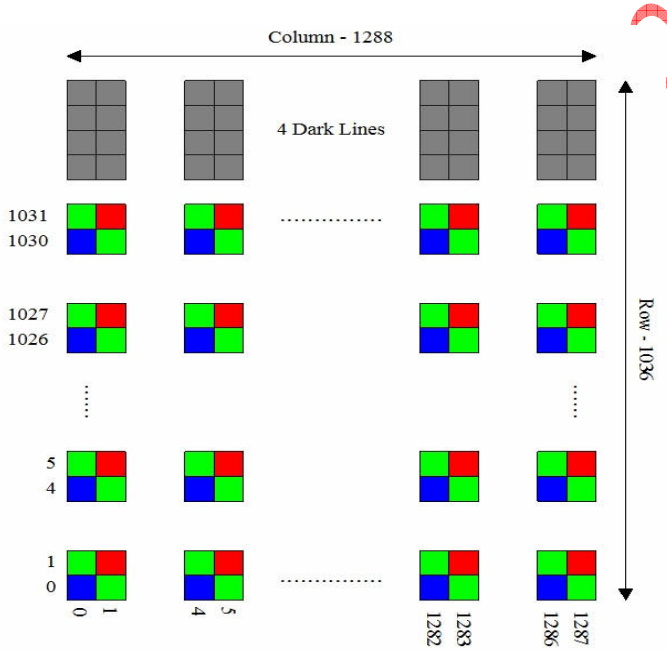

Figure 3.6

Valid pixel = (H_Size + 1) / Skip_Analog = 1288 / 2 = 644

Valid line = ((((V_Siez + 1) – 4) / Skip_Analog) + 4) = ((((1035 + 1) – 4) / 2) + 4) = 520

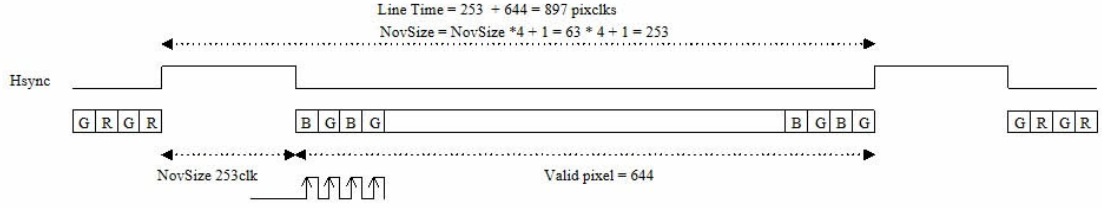

Figure 3.7 Inter-line timing of W.O.I

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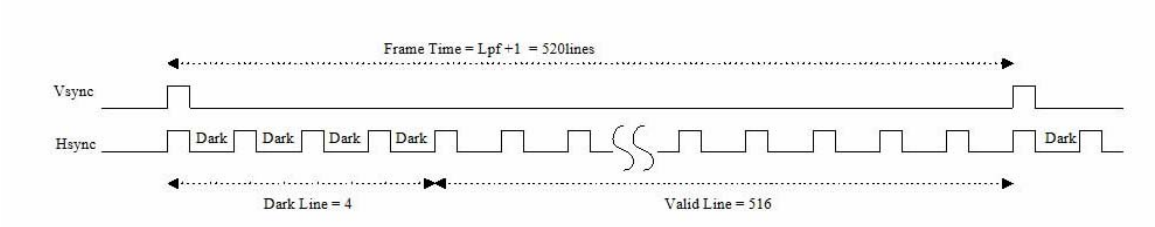

Figure 3.8 Inter-frame timing of W.O.I

3.7.2. Skip_Digital

Sub-sampling (Skip_Digital) to VGA (640x480) pixels readout (With 4 dark lines):

H_Start[9:0] = 0, V_Start[8:0] = 0, H_Size[9:0] = 1287, V_Size[8:0]= 1035,
LPF[7:0] = 1036, Nov_Size_By4[7:0] = 63, Skip_Digital = 1

Valid pixel = (H_Size + 1) / Skip_Digital = 1288 / 2 = 644
Valid line = (V_Siez + 1) / Skip_Digital = (1035 + 1) / 2 = 518

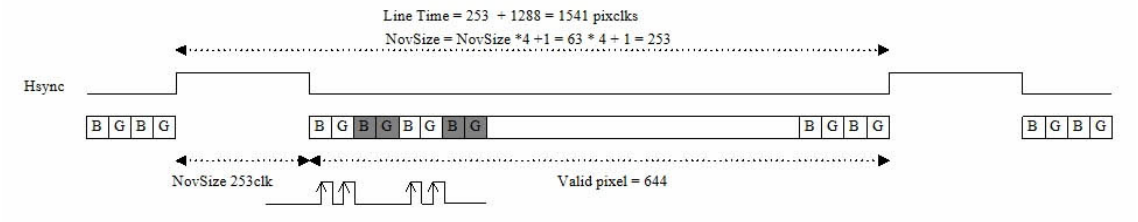

Figure 3.9 Inter-line timing

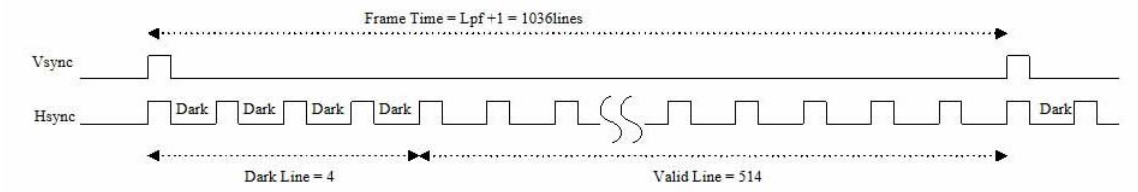

Figure 3.10 Inter-frame timing

4. I2C™ Bus

PAS5101CS supports I2C bus transfer protocol and is acting as slave device. The 7 bits unique slave address is "1000000" and supports receiving / transmitting speed up to 400KHz.

4.1. I2C Bus Overview

- Only two wires SDA (serial data) and SCL (serial clock) carry information between the devices connected to the I2C bus. Normally both SDA and SCL lines are open collector structure and pull high by external pull-up resistors.
- Only the master can initiates a transfer (start), generates clock signals, and terminates a transfer (stop).
- Start and stop condition : A high to low transition of the SDA line while SCA is high defines a start condition. A low to high transition of the SDA line while SCA is high defines a stop condition. Please refer to Figure 4.1.
- Valid data : The data on the SDA line must be stable during the high period of the SCA clock. Within each byte, MSB is always transferred first. Read / Write control bit is the LSB of the first byte. Please refer to Figure 4.2.
- Both the master and slave can transmit and receive data from the bus.
- Acknowledge : The receiving device should pull down the SDA line during high period of the SCL clock line when a complete byte was transferred by transmitter. In the case of a master received data from a slave, the master does not generate an acknowledgment on the last byte to indicate the end of a master read cycle.

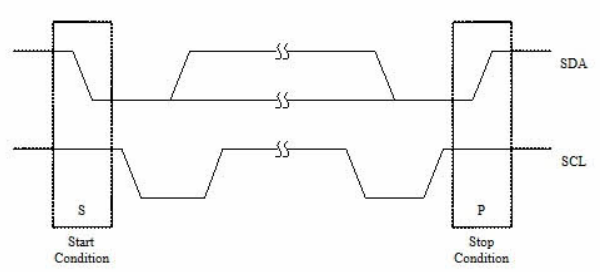

Figure 4.1 Start and Stop conditions

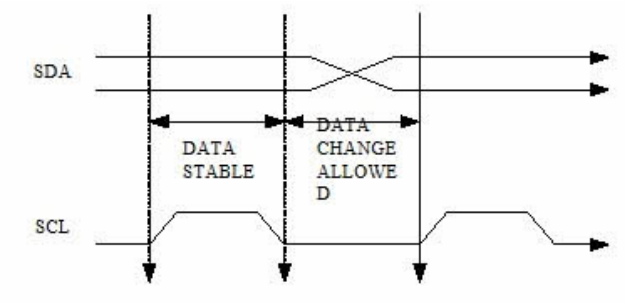

Figure 4.2 Valid Data

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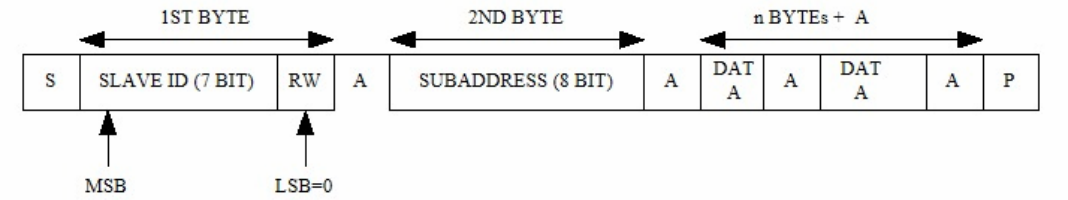
4.2. Data Transfer Format

4.2.1. Master transmits data to salve (write cycle)

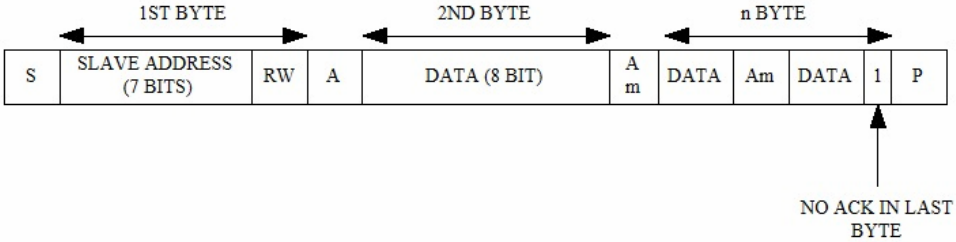
- S : Start.
- A : Acknowledge by salve.
- P : Stop.
- RW : The LSB of 1ST byte to decide whether current cycle is read or write cycle. RW = 1 – Read cycle, RW = 0 – Write cycle.
- SUBADDRESS : The address values of PAS5101CS internal control registers. (Please refer to PAS5101CS register description)



During write cycle, the master generates start condition and then places the 1st byte data that are combined slave address (7 bits) with a read / write control bit to SDA line. After slave (PAS5101CS) issues acknowledgment, the master places 2nd byte (Sub Address) data on SDA line. Again follow the PAS5101CS acknowledgment, the master places the 8 bits data on SDA line and transmit to PAS5101CS control register (address was assigned by 2nd byte). After PAS5101CS issue acknowledgment, the master can generate a stop condition to end of this write cycle. In the condition of multi-byte write, the PAS5101CS sub-address is automatically increment after each DATA byte transferred. The data and A cycles is repeat until last byte write. Every control registers value inside PAS5101CS can be programming via this way.

4.2.2. Slave transmits data to master (read cycle)

- The sub-address was taken from previous write cycle.
- The sub-address is automatically increment after each byte read.
- Am : Acknowledge by master.
- Note there is no acknowledgment from master after last byte read.



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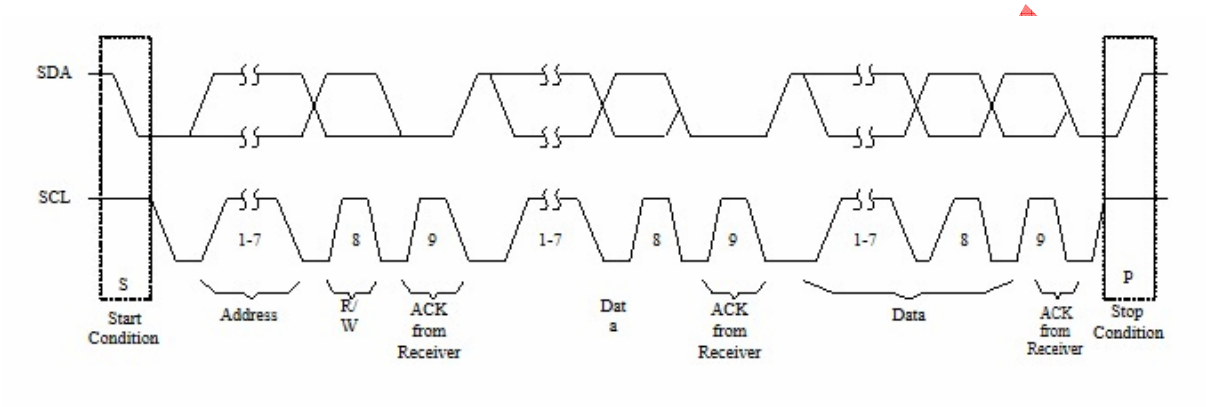
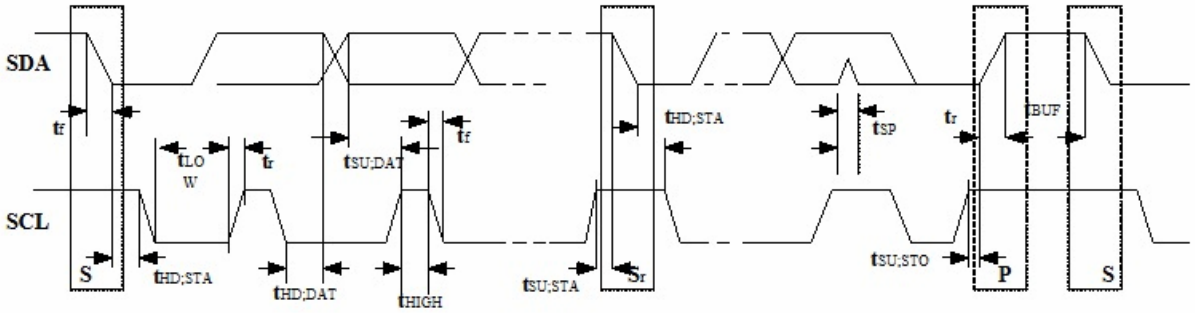
During read cycle, the master generates start condition and then place the 1st byte data that are combined slave address (7 bits) with a read / write control bit to SDA line. After issue acknowledgment, 8 bits DATA was also placed on SDA line by PAS5101CS. The 8 bits data was read from PAS5101CS internal control register that address was assigned by previous write cycle. Follow the master acknowledgment, the PAS5101CS place the next 8 bits data (address is increment automatically) on SDA line and then transmit to master serially. The DATA and Am cycles is repeat until the last byte read. After last byte read, Am is no longer generated by master but instead by keep SDA line high. The slave (PAS5101CS) must releases SDA line to master to generate STOP condition.



4.3. I2C™ Bus Timing



4.4. I2C™ Bus Timing Specification

Parameter	Symbol	Standard Mode		Unit
		Min.	Max	
SCL clock frequency.	f_{scl}	10	400	KHz
Hold time (repeated) Start condition. After this period, the first clock pulse is generated.	$t_{HD:STA}$	4.0	-	μs
Low period of the SCL clock.	t_{LOW}	4.7	-	μs
High period of the SCL clock.	t_{HIGH}	0.75	-	μs
Set-up time for a repeated START condition.	$t_{SU;STA}$	4.7	-	μs

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Data hold time. For I2C-bus device.	$t_{HD;DAT}$	0	3.45	μs
Data set-up time.	$t_{SU;DAT}$	250	-	ns
Rise time of both SDA and SCL signals.	t_r	30	N.D.	ns (notel)
Fall time of both SDA and SCL signals.	t_f	30	N.D.	ns (notel)
Set-up time for STOP condition.	$t_{SU;STO}$	4.0	-	μs
Bus free time between a STOP and START.	t_{BUF}	4.7	-	μs
Capacitive load for each bus line.	C_b	1	15	pF
Noise margin at LOW level for each connected device. (Including hysteresis)	V_{nL}	0.1 VDD	-	V
Noise margin at HIGH level for each connected device. (including hysteresis)	V_{nH}	0.2 VDD	-	V

Note : It depends on the “high” period time of SCL.

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5. Specifications

Absolute Maximum Ratings

Ambient Storage Temperature		-40℃ ~ +125℃
Supply Voltage (with respect to ground)	V_{DDD}	3V
	V_{DDA}	3V
	V_{DDQ}	4V
All Input / Output Voltage (with respect to ground)		-0.3V to V_{DDQ} +1V
Lead temperature, Surface-mount process		+230℃
ESD rating, Human Body model		2000V

DC Electrical Characteristics (Ta = 0℃ ~ 70℃)

Symbol	Parameter	Min.	Typ.	Max.	Unit
Type : POWER					
V_{DDA}	DC supply voltage – Analog	2.4	2.5	2.6	V
V_{DDD}	DC supply voltage – Digital		1.8		V
V_{DDQ}	DC supply voltage – I/O	2.4		3.3	V
I_{DD}	Operating Current (~ 15fps / 2.5v)		20		mA
I_{PWDN}	Power Down Current		10		μA
Type : IN & I/O Reset and System Clock					
V_{IH}	Input Voltage HIGH	0.7 x V_{DDQ}			V
V_{IL}	Input Voltage LOW			0.3 x V_{DDQ}	V
C_{IN}	Input Capacitor			10	pF
Type : OUT & I/O for PX 0 : 7, PXCLK, H/VSYNC & SDA, load 10pF, 1.2KΩ, 2.5V					
V_{OH}	Output Voltage HIGH	0.9 x V_{DDQ}			V
V_{OL}	Output Voltage LOW			0.1 x V_{DDQ}	V

AC Operating Condition

Symbol	Parameter	Min.	Typ.	Max.	Unit
Sysclk	Master clock frequency			48	MHz
Pxclk	Pixel clock output frequency			24	MHz

Sensor Characteristics

Parameter		Typ.	Unit
Sensitivity		TBD	V/Lux-sec
Signal to Noise Ratio		TBD	dB
Dynamic Range		TBD	dB
Temperature Range	Operation	-10 ~ +70	℃
	Stable Image	0 ~ +50	

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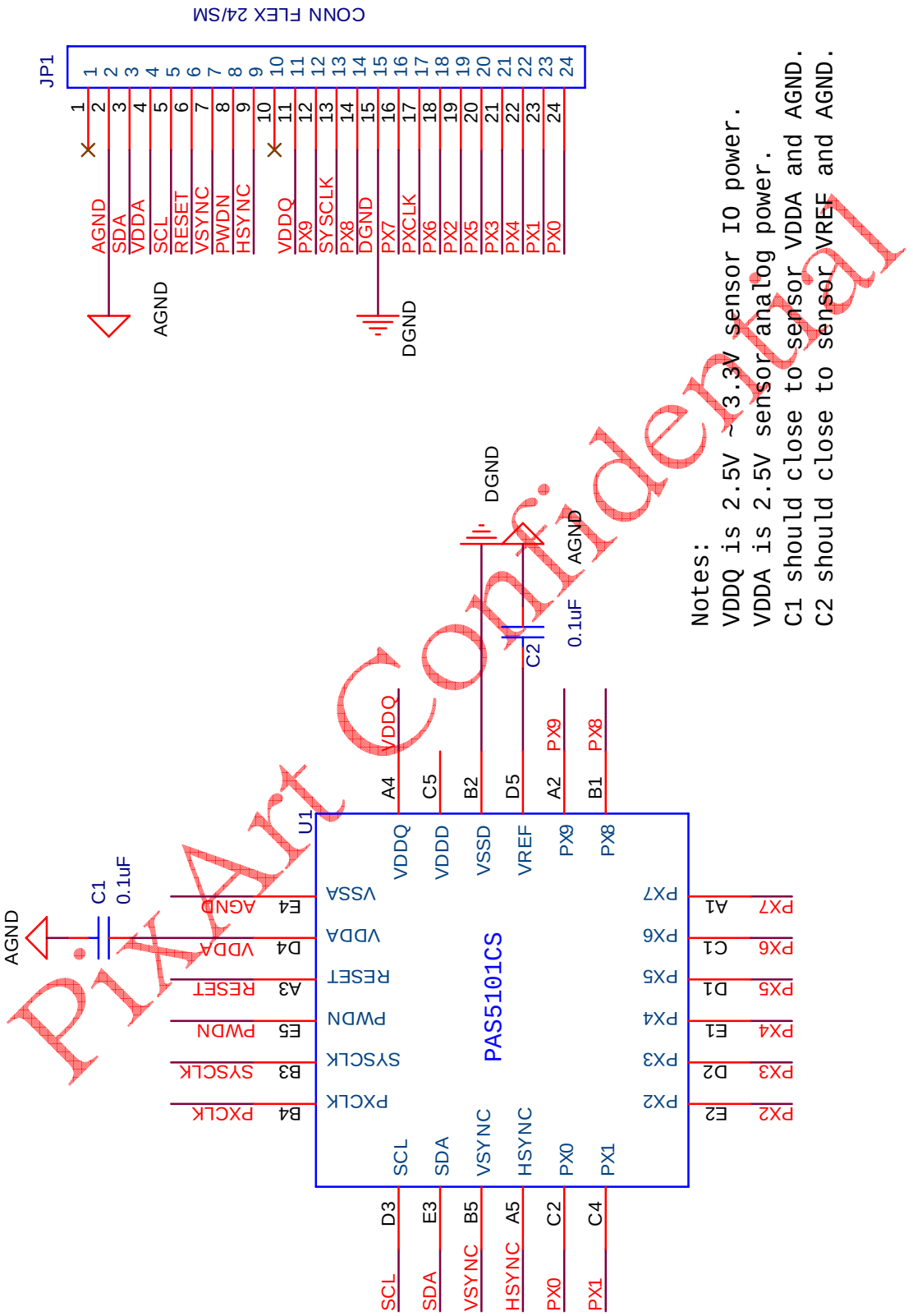
6. Reference Circuit Schematic



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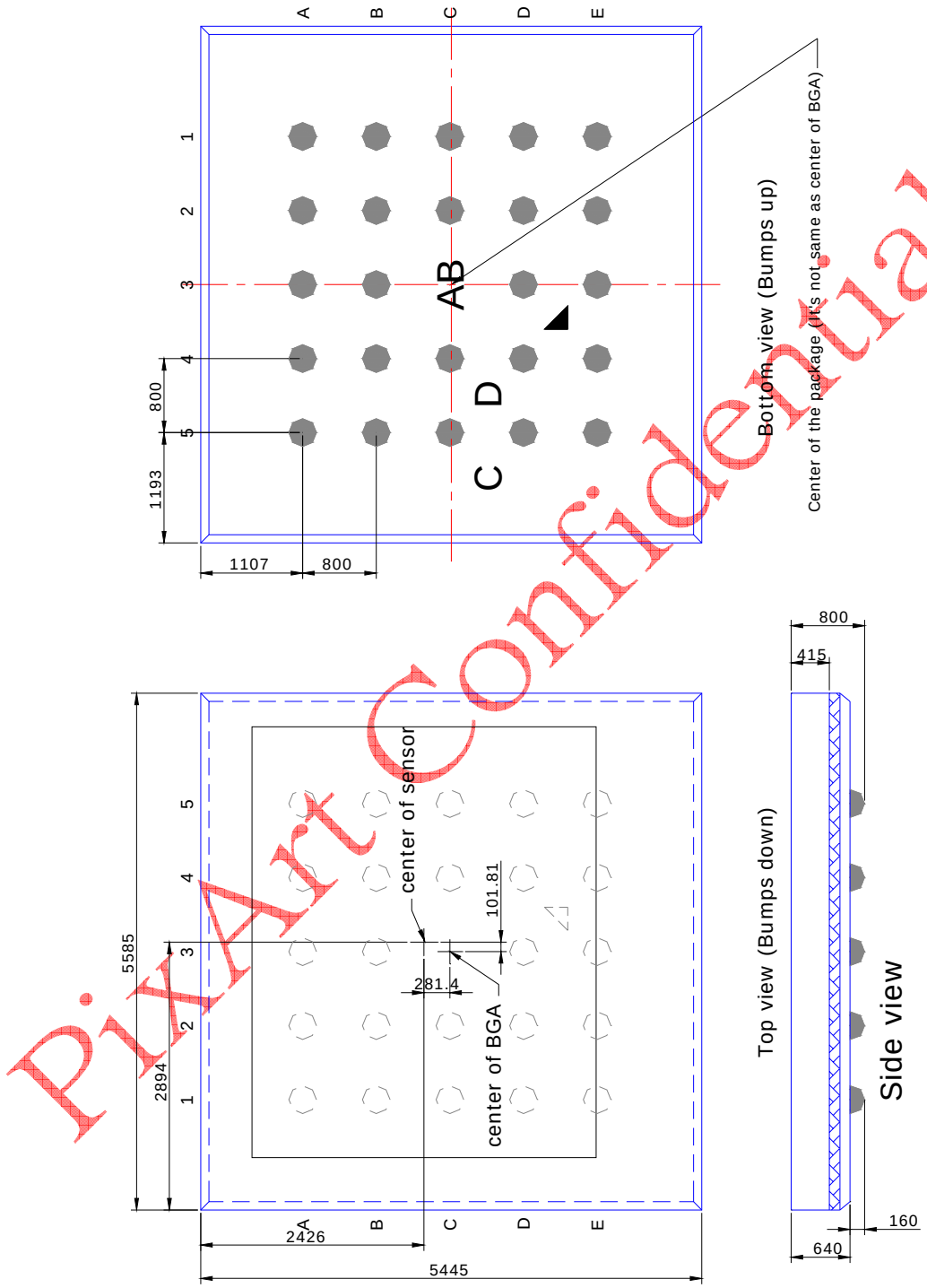
7. Package Information



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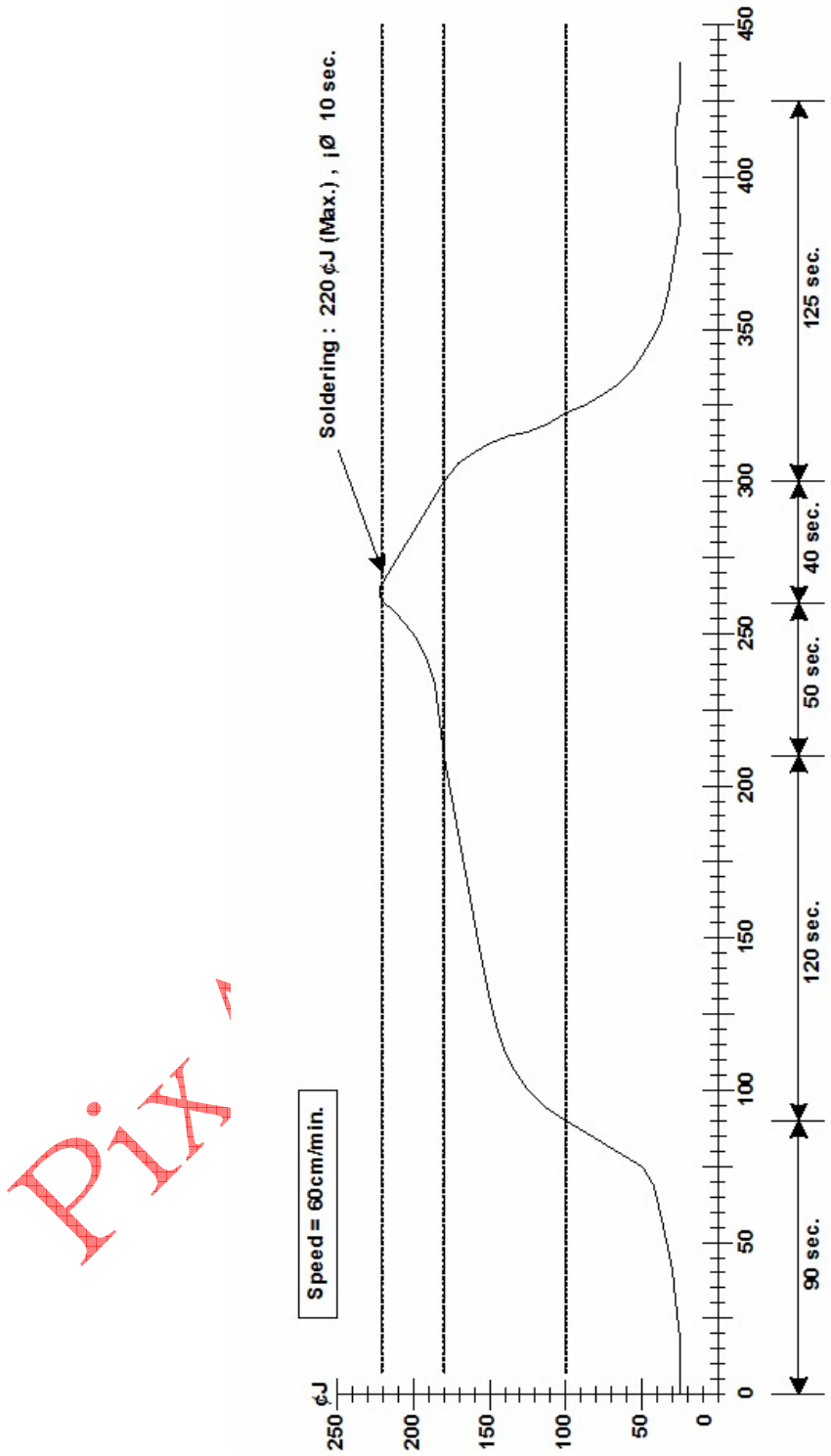
8. Reflow Profile for Non Lead-Free



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9. Lens & Holder

9.1. LarGan 40-900L

9.2. LarGan 40-519C

9.3. MaxEmil SS-4828GA

9.4. 久禾 PEH-0116-03AA

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