OV3610 Color CMOS QXGA (3.1 MPixel) CAMERACHIP™

General Description

The OV3610 (color) CAMERACHIPS™ are high performance 3.1 mega-pixel CMOS image sensors for digital still image and video/still camera products.

The device incorporates a 2048 x 1536 (QXGA) image array and an on-chip 10-bit A/D converter capable of operating at up to 7.5 frames per second (fps) in QXGA mode. Proprietary sensor technology utilizes advanced algorithms to cancel Fixed Pattern Noise (FPN), eliminate smearing, and significantly reduce blooming. The control registers allow for flexible control of timing, polarity, and CAMERACHIP operation, which in turn, allows the engineer a great deal of freedom in product design.

Features

- Optical black level calibration
- Line optical black level output capability
- Video or snapshot operations
- Programmable/Auto Exposure and Gain Control
- Programmable/Auto White Balance Control
- Horizontal and vertical sub-sampling
- High frame rate output
- Programmable image windowing
- Variable frame rate control
- On-chip R/G/B Channel and Luminance Average Counter
- Internal/External frame synchronization
- SCCB slave interface
- Power-on reset and power-down modes

Ordering Information

Product	Package
OV03610-C00A (Color, QXGA, XGA, HF)	CLCC-48

Applications

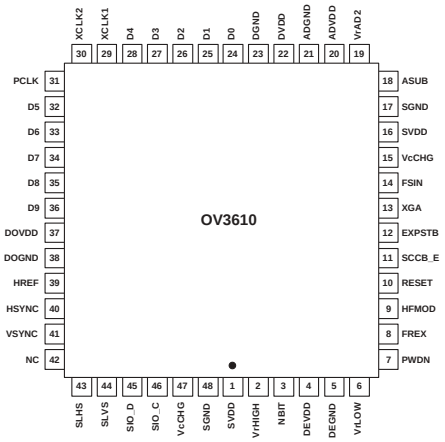
- Digital still cameras
- PC camera/dual mode
- Video conference
- Machine vision
- Security cameras
- Biometrics

Key Specifications

Array Size	**QXGA**	2048 x 1536
	XGA	1024 x 768
	DV	1024 x 510
	HF	1024 x 190
Power Supply		3.3VDC / 1.8VDC (± 5%)
Power Requirements	**Active**	< 40 mA
	Standby	< 10 µA
Electronics Exposure	**QXGA**	Up to 1548:1
	XGA	Up to 778:1
	DV	Up to 520:1
	HF	Up to 198:1
Output Format		10-bit digital RGB Raw data
Lens Size		1/2"
Maximum Image Transfer Rate	**QXGA**	7.5 fps[a]
	XGA	20 fps[b]
	DV	30 fps[b]
	HF	78 fps[b]
Sensitivity		0.9 v/Lux-sec
S/N Ratio		40 dB
Dynamic Range		60 dB (due to ADC limitations)
Scan Mode		Progressive
Pixel Size		3.18 µm x 3.18 µm
Dark Current		30 mV/s
Fixed Pattern Noise		<0.03% of $V_{PEAK-TO-PEAK}$
Image Area		6.51 mm x 4.88 mm
Package Dimensions		.560 in. x .560 in.

a. At 27 MHz system clock
b. At 24 MHz system clock

Figure 1 OV3610 Pin Diagram



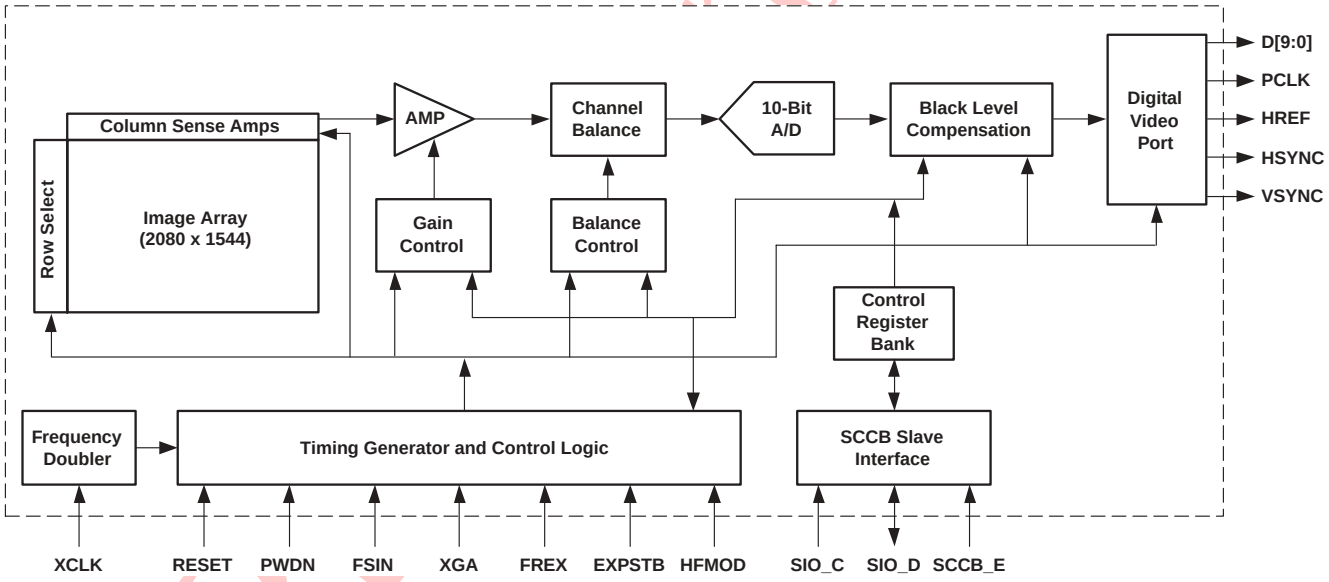
Preliminary

Functional Description

Figure 2 shows the functional block diagram of the OV3610 image sensor. The OV3610 includes:

- Image Sensor Array (2080 x 1544 resolution)
- Analog Amplifier
  - Gain Control
- Channel Balance
  - Balance Control
- 10-Bit A/D Converter
- Black Level Compensation
- Timing Generator and Control Logic
  - Frame Exposure Mode Timing
  - Frame Rate Timing
  - Frame Rate Adjust
- SCCB Interface
- Channel Average Calculator

Figure 2 Functional Block Diagram

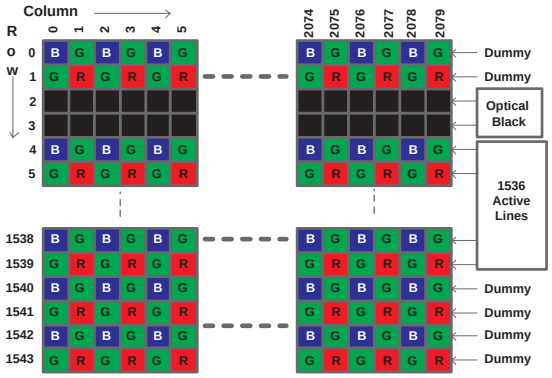


Preliminary

Image Sensor Array

The OV3610 sensor is a 1/2-inch CMOS imaging device. The sensor contains 3,211,520 pixels. Figure 3 shows the color filter layout.

Figure 3 Sensor Array Region Color Filter Layout



The color filters are in a Bayer pattern. The primary color BG/GR array is arranged in line-alternating fashion. Of the 3,211,520 pixels, 3,145,728 are active. The other pixels are used for black level calibration and interpolation.

The sensor array design is based on a field integration read-out system with line-by-line transfer and an electronic shutter with a synchronous pixel read-out scheme.

Analog Amplifier

When the column sample/hold circuit has sampled one row of pixels, the pixel data will shift out one-by-one into an analog amplifier.

Gain Control

The amplifier gain can either be programmed by the user or controlled by the internal automatic gain control circuit (AGC).

Channel Balance

The amplified signals are then balanced with a channel balance block. In this block, the Red/Blue channel gain is increased or decreased to match Green channel luminance level. The adjustment range is ±48 dB.

Balance Control

Channel balance can be done manually by the user or by the internal automatic white balance (AWB) controller.

10-Bit A/D Converter

The balanced signal is then digitized by the on-chip 10-bit ADC. It can operate at 12 MHz and is fully synchronous to the pixel clock. The actual conversion rate is determined by the frame rate.

Black Level Compensation

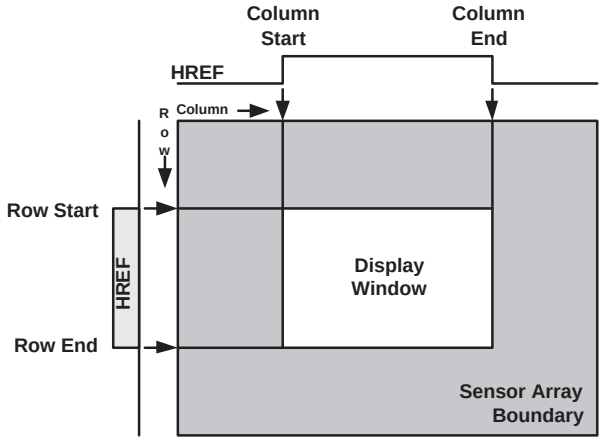
After the pixel data has been digitized, black level calibration can be applied before the data is output. The black level calibration block subtracts the average signal level of optical black pixels to compensate for the dark current in the pixel output. Black level calibration can be disabled by the user.

Windowing

The OV3610 allows the user to define window size or region of interest (ROI), as required by the application. Window size setting (in pixels) ranges from 2 x 4 to 2048 x 1536 (QXGA) or 2 x 2 to 1024 x 768 (XGA), 1024 x 510 (DV), and 1024 x 190 (HF). Note that modifying window size or window position does not alter the frame or pixel rate. The windowing control merely alters the assertion of the HREF signal to be consistent with the programmed horizontal and vertical ROI. The default window size is 2048 x 1536. Refer to Figure 4 and registers HREFST, HREFEND, VSTRT, VEND, and COMM for details. The maximum output window size is 2054 columns by 1540 rows.

Note that after writing to register COMH (0x12) to change the sensor mode, registers related to the sensor's cropping window will be reset back to their default values.

Figure 4 Windowing



Preliminary

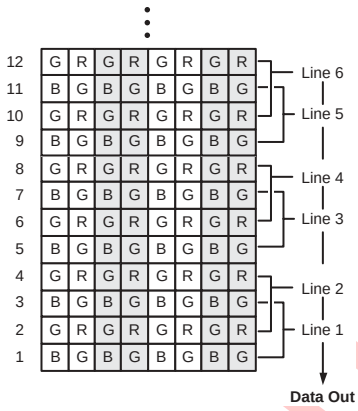
Sub-sampling Mode

The OV3610 supports three sub-sampling modes. Each sub-sampling mode has different resolution and maximum frame rate. These modes are described in the following sections.

XGA mode

The OV3610 can be programmed to output in 1024 x 768 (XGA) sized images for applications where higher resolution image capture is not required. In this mode, the OV3610 averages the B and G pixels (see Figure 5) in lines 1 and 3 to output line 1, G and R pixels in lines 2 and 4 to output line 2, B and G pixels in lines 5 and 7 to output line 3, G and R pixels in lines 6 and 8 to output line 4, etc.

Figure 5 XGA Sub-Sampling Mode



Digital Video Mode

The OV3610 can also operate at a higher frame rate in digital video (DV) mode. In this mode, the OV3610 averages the B and G pixels (see Figure 6) of lines 1 and 3 to output line 1, G and R pixels of lines 4 and 6 to output line 2, B and G pixels of lines 7 and 9 to output line 3, etc.

High Frame Rate Mode

The OV3610 image array sensor can also operate at a High Frame rate (HF) mode. In this mode, the OV3610 averages the B and G pixels (see Figure 7) in lines 1 and 5 to output line 1, G and R pixels of lines 10 and 14 to output line 2, B and G pixels of lines 17 and 21 to output line 3, G and R pixels of lines 26 and 30 to output line 4, etc.

This mode enables up to 78 fps output using a 24 MHz system clock so it is effective for high frame rate application.

Figure 6 Digital Video Sub-Sampling Mode

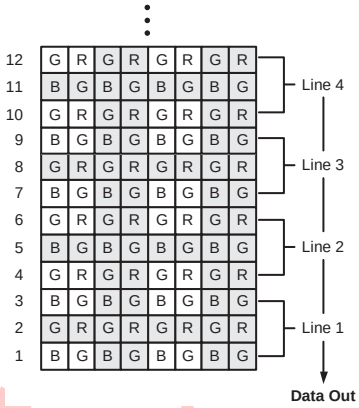
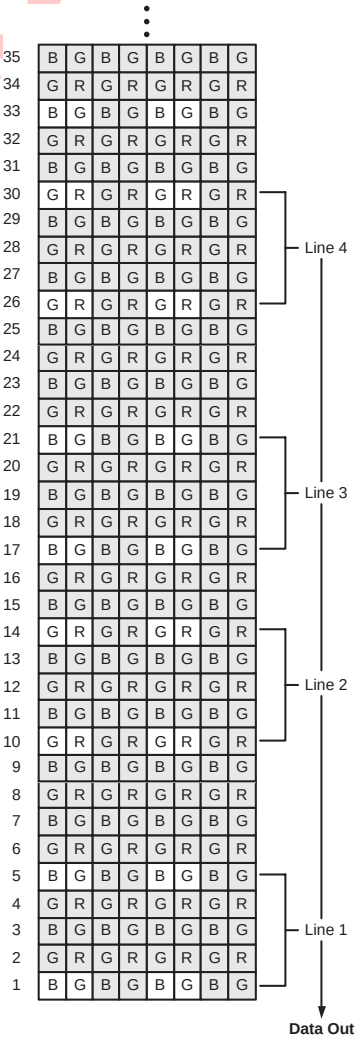


Figure 7 High Frame Rate Sub-Sampling Mode



Preliminary

Timing Generator and Control Logic

In general, the timing generator controls the following:

- Frame Exposure Mode Timing
- Frame Rate Timing
- Frame Rate Adjust

Frame Exposure Mode Timing

The OV3610 supports frame exposure mode. Typically, the frame exposure mode must work with the aid of an external shutter.

The frame exposure pin, FREX (pin 8), is the frame exposure mode enable pin and the EXPSTB pin (pin 12) serves as the sensor's exposure start trigger. There are two ways to set Frame Exposure mode:

- Control both FREX and EXPSTB pins - Frame Exposure mode can be set by pulling both FREX and EXPSTB pins high at the same time (see Figure 21).
- Control FREX only and keep EXPSTB low - In this case, the pre-charge time is tline and sensor exposure time is the period after pre-charge until the shutter closes (see Figure 20).

When the external master device asserts the FREX pin high, the sensor array is quickly pre-charged and stays in reset mode until the EXPSTB pin is pulled low (sensor exposure time can be defined as the period between EXPSTB low to shutter close). After the FREX pin is pulled low, the video data stream is then clocked to the output port in a line-by-line manner. After completing one frame of data output, the OV3610 will output continuous live video data unless in single frame transfer mode. Figure 20, Figure 21, Figure 22, and Figure 23 show detailed timing of the Frame Exposure mode. Table 10 shows the timing specifications for this mode.

When the OV3610 is working in frame exposure mode, every line is sampled at different times causing different dark current levels line-by-line. To eliminate the dark current difference, the OV3610 provides line optical black pixel output. The difference in dark current can be calibrated line-by-line.

For frame exposure mode, register AEC (0x10) must be set to 0xFF and register GAIN (0x00) should be no larger than 0x10 (maximum 2x gain).

Frame Rate Timing

Default frame timing is illustrated in Figure 16, Figure 17, and Figure 19. Refer to Table 1 for the actual pixel rate at different frame rates.

Table 1 Frame/Pixel Rates in QXGA Mode

Frame Rate (fps)	7.5	6.67	3.33	1.67
PCLK (MHz)	27	24	12	6

Frame Rate Adjust

The OV3610 offers three methods for frame rate adjustment:

- Clock prescaler: (see "CLKRC" on page 21)
  By changing the system clock divide ratio, the frame rate and pixel rate will change together. This method can be used for dividing the frame/pixel rate by: 1/2, 1/3, 1/4 … 1/64 of the input clock rate.
- Line adjustment: (see "COML" on page 26 and see "FRARL" on page 26)
  By adding a dummy pixel timing in each line after active pixel output, the frame rate can be changed while leaving the pixel rate as is.
- Vertical sync adjustment:
  By adding dummy line periods to the vertical sync period (see "ADDVSL" on page 27 and see "ADDVSH" on page 27), the frame rate can be altered while the pixel rate remains the same.

Note that the total number of pixels per line should be less than 4096.

SCCB Interface

The OV3610 provides an on-chip SCCB serial control port that allows access to all internal registers, for complete control and monitoring of OV3610 operation.

Refer to *OmniVision Technologies Serial Camera Control Bus (SCCB) Specification* for detailed usage of the serial control port.

Preliminary

Slave Operation Mode

The OV3610 can be programmed to operate in slave mode (default is master mode).

When used as a slave device, the OV3610 uses input pins, SLHS and SLVS, for use as horizontal and vertical synchronization input triggers supplied by a master device. The master device must provide the following signals:

1. System clock MCLK to XCLK1 pin
2. Horizontal sync MHSYNC to SLHS pin
3. Vertical frame sync MVSYNC to SLVS pin

See Figure 8 for slave mode connections and Figure 9 for detailed timing considerations.

Figure 8 Slave Mode Connection

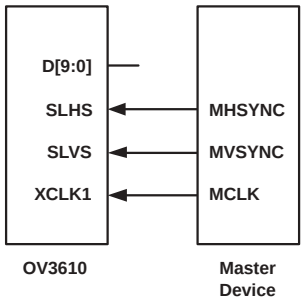
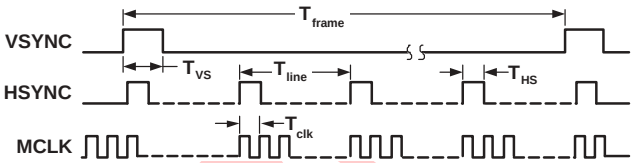


Figure 9 Slave Mode Timing



NOTE:

1) $T_{HS} > 6\ T_{clk}$, $Tvs > T_{line}$
2) $T_{line} = 2320 \times T_{clk}$ (QXGA); $T_{line} = 1536 \times T_{clk}$ (XGA)
3) $T_{frame} = 1550 \times T_{line}$ (QXGA); $T_{frame} = 780 \times T_{line}$ (XGA)

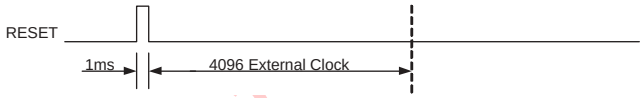
Channel Average Calculator

The OV3610 provides average output level data for the R/G/B channels along with frame-averaged luminance level. Access to the data is provided via the SCCB interface.

Reset

The RESET pin (pin 10) is active high. There is an internal pull-down (weak) resistor in the sensor so the default status of the RESET pin is low.

Figure 10 RESET Timing Diagram



There are two ways for a sensor reset:

1. Hardware reset - Pulling the RESET pin high and keeping it high for at least 1 ms. As shown in Figure 10, after a reset has been initiated, the sensor will be most stable after the period shown as 4096 External Clock.
2. Software reset - Writing 0x80 to register 0x12 (see "COMH" on page 22) for a software reset. If a software reset is used, a reset operation done twice is recommended to make sure the sensor is stable and ready to access registers. When performing a software reset twice, the second reset should be initiated after the 4096 External Clock period as shown in Figure 10.

Power Down Mode

The PWDN pin (pin 7) is active high. There is an internal pull-down (weak) resistor in the sensor so the default status of the PWDN pin is low.

Figure 11 PWDN Timing Diagram

Two methods of power-down or standby operation are available with the OV3610.

- Hardware power-down may be selected by pulling the PWDN pin (pin 7) high (+3.3VDC). When this occurs, the OV3610 internal device clock is halted and all internal counters are reset. The current draw is less than 10 µA in this standby mode.
- Software power-down can be effected by setting the COMC[4] register bit high. Standby current will be less then 1 mA when in software power-down. All register content is maintained in standby mode.

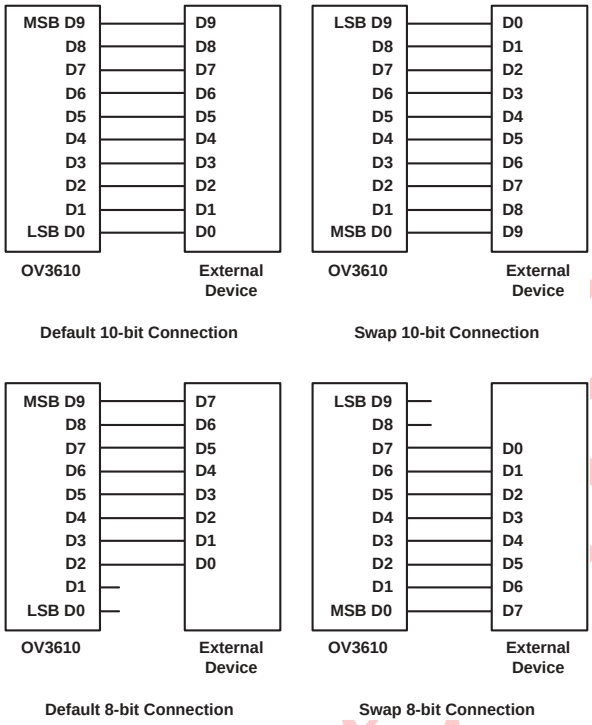
Preliminary

Digital Video Port

MSB/LSB Swap

The OV3610 has a 10-bit digital video port. The MSB and LSB can be swapped with the control registers. Figure 12 shows some examples of connections with external devices.

Figure 12 Connection Examples



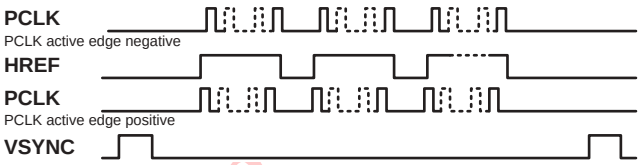
Line/Pixel Timing

The OV3610 digital video port can be programmed to work in either master or slave mode.

In both master and slave modes, pixel data output is synchronous with PCLK (or MCLK if port is a slave), HREF, and VSYNC. The default PCLK edge for valid data is the negative edge but may be programmed using register COMK[4] for the positive edge. Basic line/pixel output timing and pixel timing specifications are shown in Figure 15 and Table 9.

Also, PCLK output can be programmed using register COMK[5] to be gated by the active video period defined by the HREF signal. See Figure 13 for details.

Figure 13 PCLK Output Only at Valid Pixels



The specifications shown in Table 9 apply for DVDD = +1.8 V, DOVDD = +3.3 V, T_A = 25°C, sensor working at 6.67 fps in QXGA resolution, external loading = 30 pF.

Pixel Output Pattern

Table 2 shows the output data order from the OV3610. The data output sequence following the first HREF and after VSYNC is: $B_{0,0}$ $G_{0,1}$ $B_{0,2}$ $G_{0,3}$... $B_{0,2046}$ $G_{0,2047}$. After the second HREF the output is $G_{1,0}$ $R_{1,1}$ $G_{1,2}$ $R_{1,3}$... $G_{1,2046}$ $R_{1,2047}$..., etc.

Table 2 Data Pattern

R/C	0	1	2	3	. . .	2046	2047
0	$B_{0,0}$	$G_{0,1}$	$B_{0,2}$	$G_{0,3}$	. . .	$B_{0,2046}$	$G_{0,2047}$
1	$G_{1,0}$	$R_{1,1}$	$G_{1,2}$	$R_{1,3}$	. . .	$G_{1,2046}$	$R_{1,2047}$
2	$B_{2,0}$	G_2	$B_{2,2}$	$G_{2,3}$	. . .	$B_{2,2046}$	$G_{2,2047}$
3	$G_{3,0}$	$R_{3,1}$	$G_{3,2}$	$R_{3,3}$	. . .	$G_{3,2046}$	$R_{3,2047}$
. .					. .		
1534	$B_{1534,0}$	$G_{1534,1}$	$B_{1534,2}$	$G_{1534,3}$		$B_{1534,2046}$	$G_{1534,2047}$
1535	$G_{1535,0}$	$R_{1535,1}$	$G_{1535,2}$	$R_{1535,3}$		$G_{1535,2046}$	$R_{1535,2047}$

If the OV3610 is programmed to output XGA resolution data, horizontal and vertical sub-sampling will occur (see "XGA mode" on page 4 for details on XGA sub-sampling).

Preliminary

Pin Description

Table 3 Pin Description

Pin Number	Name	Pin Type	Function/Description
01	SVDD	Power	3.3 V supply for the sensor array
02	VrHIGH	Analog	Sensor high reference - connect to ground using a 0.1 µF capacitor
03	NBIT	Analog	Sensor bit line reference - connect to ground using a 0.1 µF capacitor
04	DEVDD	Power	3.3 V supply for the sensor array decoder
05	DEGND	Power	Ground for sensor array decoder
06	VrLOW	Analog	Sensor low reference - connect to ground using a 0.1 µF capacitor
07	PWDN	Input (0)[a]	Power down mode enable, active high
08	FREX	Input (0)	Snapshot trigger - use to activate a snapshot sequence
09	HFMOD	Input (0)	High Frame rate (HF) mode ON/OFF selection 0: HF mode OFF 1: HF mode ON
10	RESET	Input (0)	Chip reset, active high
11	SCCB_E	Input (0)	SCCB interface enable signal, active low
12	EXPSTB	Input (0)	Snapshot Exposure Start Trigger 0: Sensor starts exposure (only effective in snapshot mode) 1: Sensor stays in reset mode
13	XGA	Input (0)	Sensor Resolution Selection 0: QXGA resolution (2048 x 1536) 1: XGA resolution (1024 x 768)
14	FSIN	Input (0)	Frame synchronization input
15	VcCHG	Analog	Sensor reference - bypass to ground using a 1 µF capacitor
16	SVDD	Power	3.3 V supply for sensor array - must short with pin 01 on PCB.
17	SGND	Power	Ground for sensor array - must short with pin 48 on PCB.
18	ASUB	Power	Analog ground (substrate)
19	VrAD2	Analog	A/D converter reference - bypass to ground using a 0.1 µF capacitor
20	ADVDD	Power	3.3 V supply for A/D converter
21	ADGND	Power	A/D converter ground
22	DVDD	Power	1.8 V supply for digital circuits
23	DGND	Power	Digital ground
24	D0	Output	Video port output bit[0]
25	D1	Output	Video port output bit[1]
26	D2	Output	Video port output bit[2]
27	D3	Output	Video port output bit[3]

Preliminary

Table 3 Pin Description (Continued)

Pin Number	Name	Pin Type	Function/Description
28	D4	Output	Video port output bit[4]
29	XCLK1	Input	Crystal clock input
30	XCLK2	Output	Crystal clock output
31	PCLK	Output	Pixel clock output
32	D5	Output	Video port output bit[5]
33	D6	Output	Video port output bit[6]
34	D7	Output	Video port output bit[7]
35	D8	Output	Video port output bit[8]
36	D9	Output	Video port output bit[9]
37	DOVDD	Power	3.3 V supply for digital video port
38	DOGND	Power	Digital video port ground
39	HREF	Output	Horizontal reference output
40	HSYNC	Output	Horizontal synchronization output
41	VSYNC	Output	Vertical synchronization output
42	NC	—	No connection
43	SLHS	Input (0)	Slave mode horizontal synchronization input, active high
44	SLVS	Input (0)	Slave mode vertical synchronization input, active high
45	SIO_D	I/O	SCCB serial interface data I/O
46	SIO_C	Input	SCCB serial interface clock input
47	VcCHG	Analog	Sensor reference. Internal connect with pin 15. Bypass to ground using a 1 µF capacitor
48	SGND	Power	Ground for sensor array

a. Input (0) represents an internal pull-down resistor.

Preliminary

Electrical Characteristics

Table 4 Operating Conditions

Parameter	Min	Max	Unit
Operating temperature	0	40	°C
Storage temperature	-40	125	°C
Operating humidity	TBD	TBD	
Storage humidity	TBD	TBD	

Table 5 DC Characteristics (0°C < T_A < 85°C, Voltages referenced to GND)

Symbol	Parameter	Min	Typ	Max	Unit
Supply					
V_{DD-A}	Supply voltage (DEVDD, ADVDD, AVDD, SVDD)	3.0	3.3	3.6	V
V_{DD-IO}	Supply voltage (DOVDD)	3.0	3.3	3.6	V
V_{DD-C}	Supply voltage (DVDD)	1.71	1.8	1.89	V
I_{DD-A}	Supply current (QXGA at 7.5 fps)		20		mA
I_{DD-IO}	Supply current (V_{DD-IO} = 3 V at 7.5 fps without digital I/O loading)		15		mA
I_{DD-C}	Supply current (V_{DD-C} = 1.8 V at 7.5 fps in QXGA resolution)		1		mA
Digital Inputs					
V_{IL}	Input voltage LOW			0.8	V
V_{IH}	Input voltage HIGH	2			V
C_{IN}	Input capacitor			10	pF
Digital Outputs (standard loading 25 pF, 1.2 KΩ to 3 V)					
V_{OH}	Output voltage HIGH	2.4			V
V_{OL}	Output voltage LOW			0.6	V
SCCB Inputs					
V_{IL}	SIO_C and SIO_D	-0.5	0	1	V
V_{IH}	SIO_C and SIO_D	2.5	3.3	V_{DD} + 0.5	V

Preliminary

Table 6 AC Characteristics (T_A = 25°C, V_{DD} = 3V)

Symbol	Parameter	Min	Typ	Max	Unit
ADC Parameters					
B	Analog bandwidth		12		MHz
DLE	DC differential linearity error		0.5		LSB
ILE	DC integral linearity error		1		LSB
	Settling time for hardware reset			<1	ms
	Settling time for software reset			<1	ms
	Settling time for XGA/QXGA mode change			<1	ms
	Settling time for register setting			<300	ms

Table 7 Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
Oscillator and Clock Input					
f_{OSC}	Frequency (XCLK1, XCLK2)	8	24	48	MHz
t_r, t_f	Clock input rise/fall time			2	ns
	Clock input duty cycle	45	50	55	%

Preliminary

Timing Specifications

Figure 14 SCCB Timing Diagram

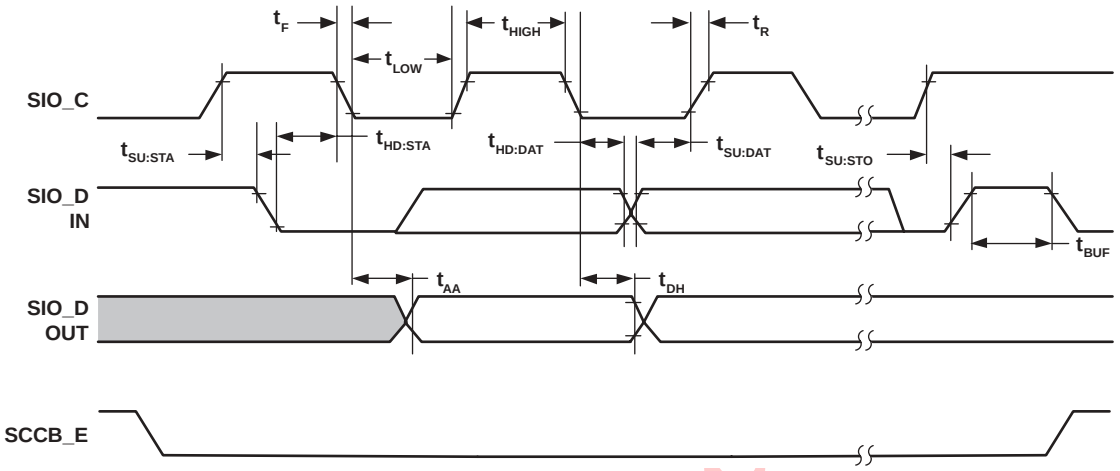


Table 8 SCCB Timing Specifications

Symbol	Parameter	Min	Typ	Max	Unit
f_{SIO_C}	Clock Frequency			400	KHz
t_{LOW}	Clock Low Period	1.3			µs
t_{HIGH}	Clock High Period	600			ns
t_{AA}	SIO_C low to Data Out valid	100		900	ns
t_{BUF}	Bus free time before new START	1.3			µs
$t_{HD:STA}$	START condition Hold time	600			ns
$t_{SU:STA}$	START condition Setup time	600			ns
$t_{HD:DAT}$	Data-in Hold time	0			µs
$t_{SU:DAT}$	Data-in Setup time	100			ns
$t_{SU:STO}$	STOP condition Setup time	600			ns
t_{R}, t_{F}	SCCB Rise/Fall times			300	ns
t_{DH}	Data-out Hold time	50			ns

Preliminary

Figure 15 QXGA, XGA, and HF Mode Line/Pixel Output Timing

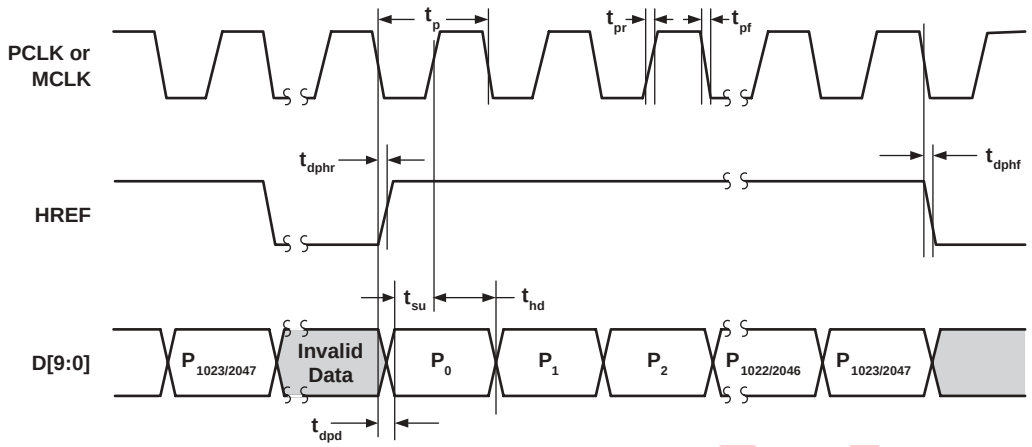


Figure 16 QXGA Frame Timing

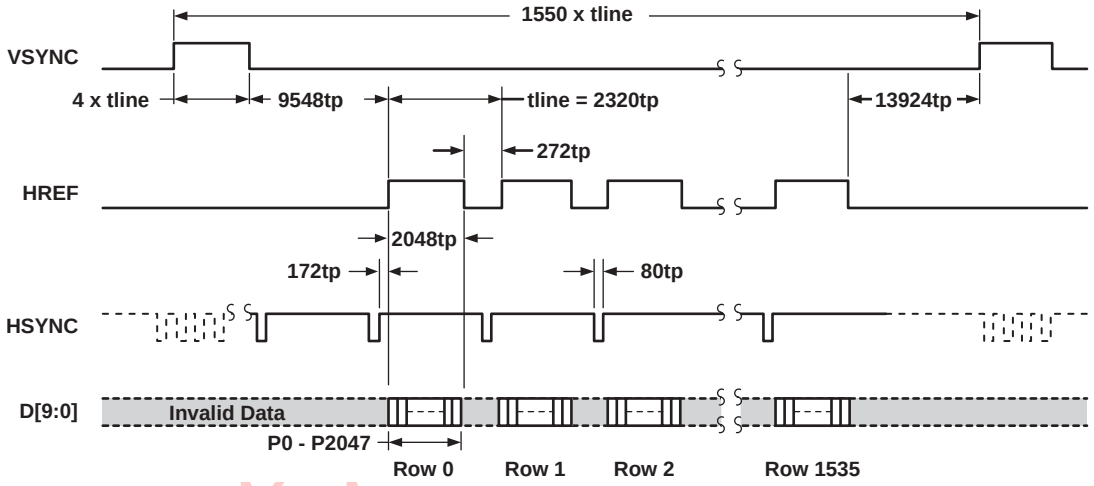


Figure 17 XGA Frame Timing

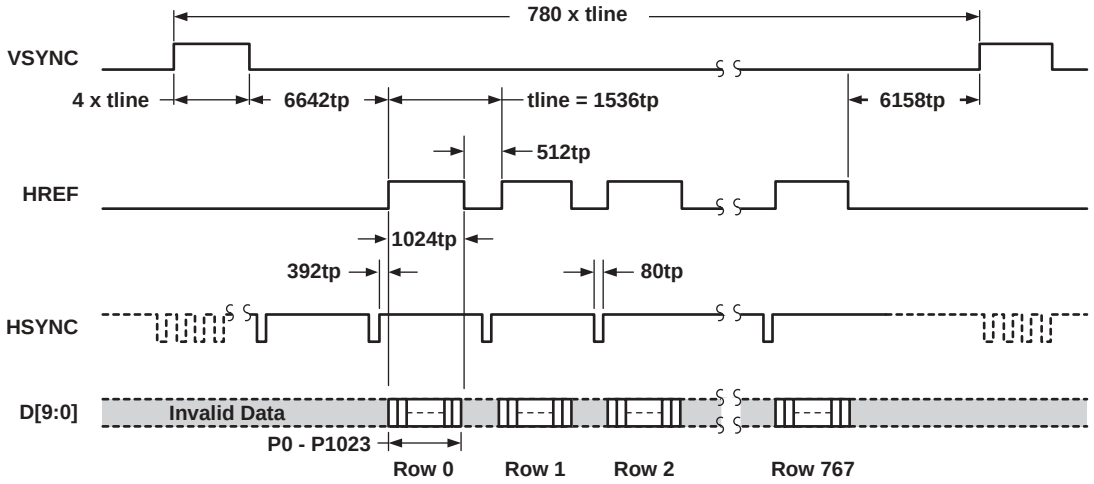


Figure 18 DV Mode Frame Timing

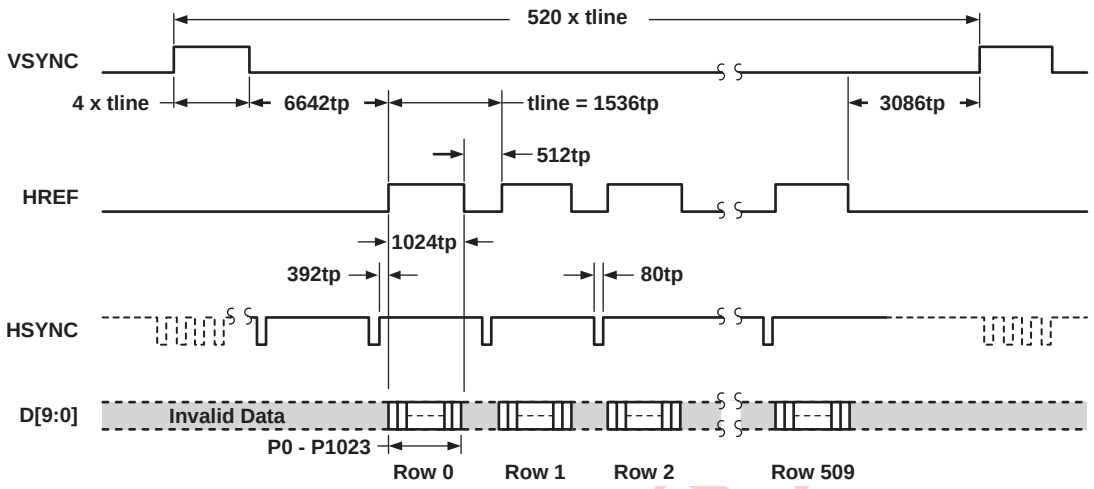


Figure 19 HF Mode Frame Timing

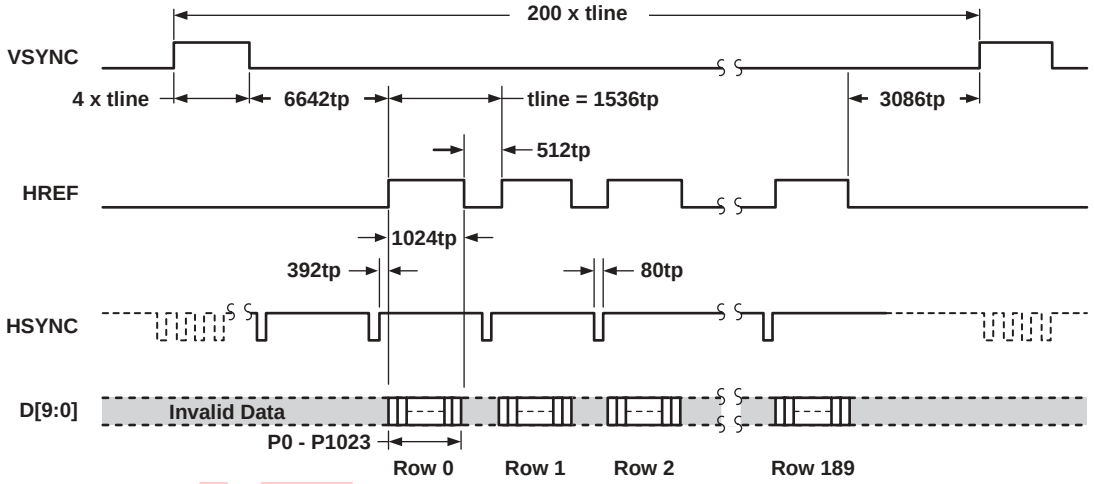


Table 9 Pixel Timing Specification

Symbol	Parameter	Min	Typ	Max	Unit
t_p	PCLK period		41.67		ns
t_{pr}	PCLK rising time		10		ns
t_{pf}	PCLK falling time		5		ns
t_{dphr}	PCLK negative edge to HREF rising edge	0		5	ns
t_{dphf}	PCLK negative edge to HREF negative edge	0		5	ns
t_{dpd}	PCLK negative edge to data output delay	0		5	ns
t_{su}	Data bus setup time	15			ns
t_{hd}	Data bus hold time	8			ns

Figure 20 Frame Exposure Mode Timing with EXPSTB Staying Low

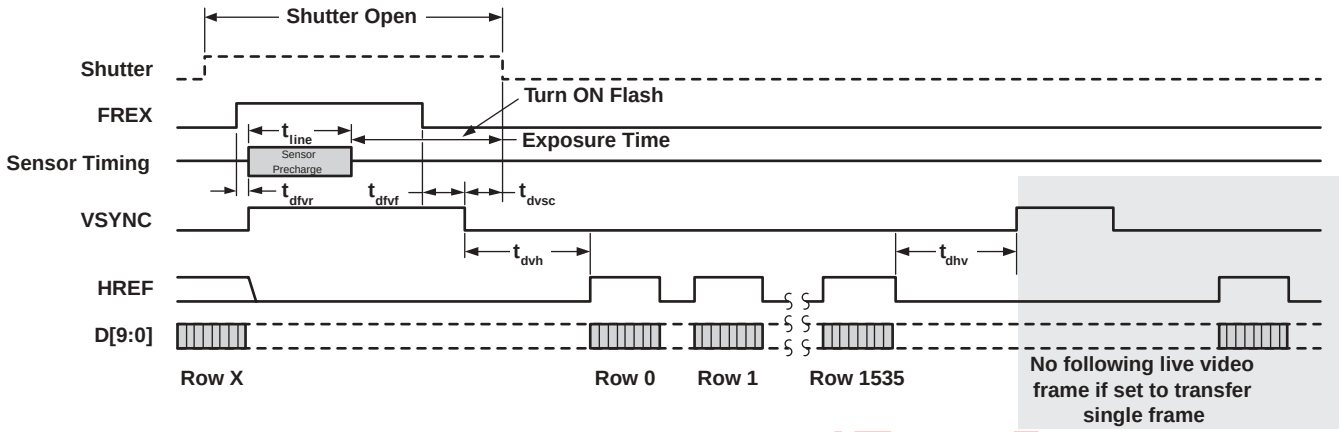
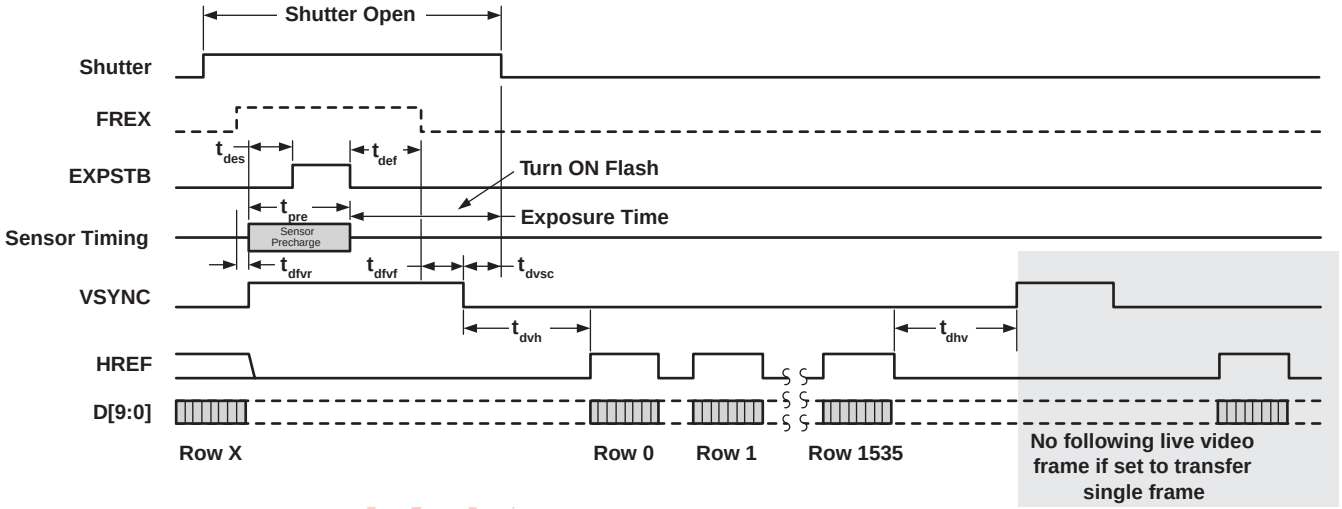


Figure 21 Frame Exposure Mode Timing with EXPSTB Asserted



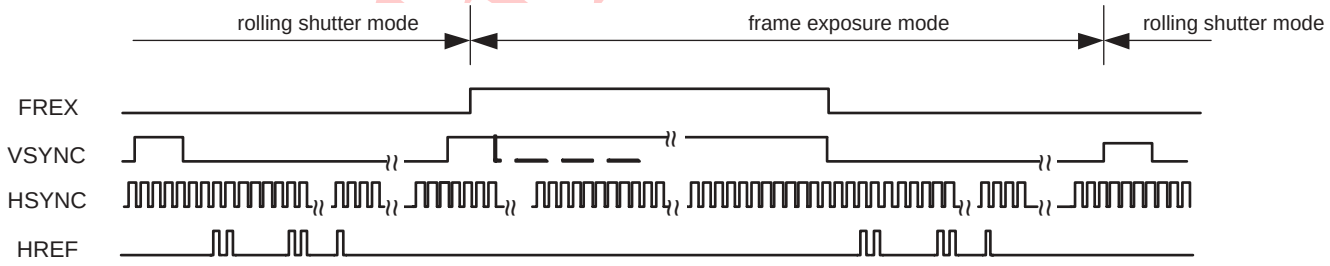
Pre

Table 10 Frame Exposure Timing Specifications

Symbol	Min	Typ	Max	Unit
tline		2320 (QXGA)		tp
		1536 (XGA)		tp
tvs		4		tline
tdfvr	8		9	tp
tdfvf			4	tline
tdvsc			2	tline
tdhv		13924 (QXGA)		tp
		3096 (XGA)		tp
tdvh		9548 (QXGA)		tp
		9704 (XGA)		tp
tdhso	0			ns
tdef	20			tp
tdes			2300 (QXGA)	tp
			1500 (XGA)	tp

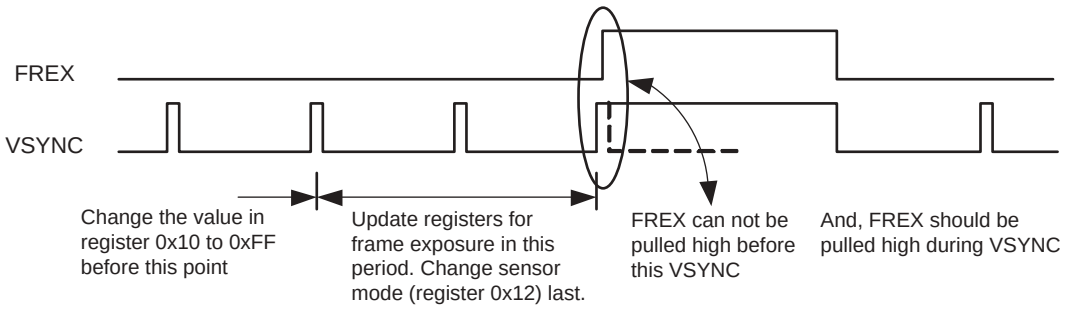
NOTE 1) FREX must stay high long enough to ensure the entire sensor has been reset.
2) Shutter must be closed no later then 4640 tp (3072 tp for XGA) after VSYNC falling edge.

Figure 22 Frame Exposure Mode Control Timing



FREX can be pulled high only when VSYNC is high.

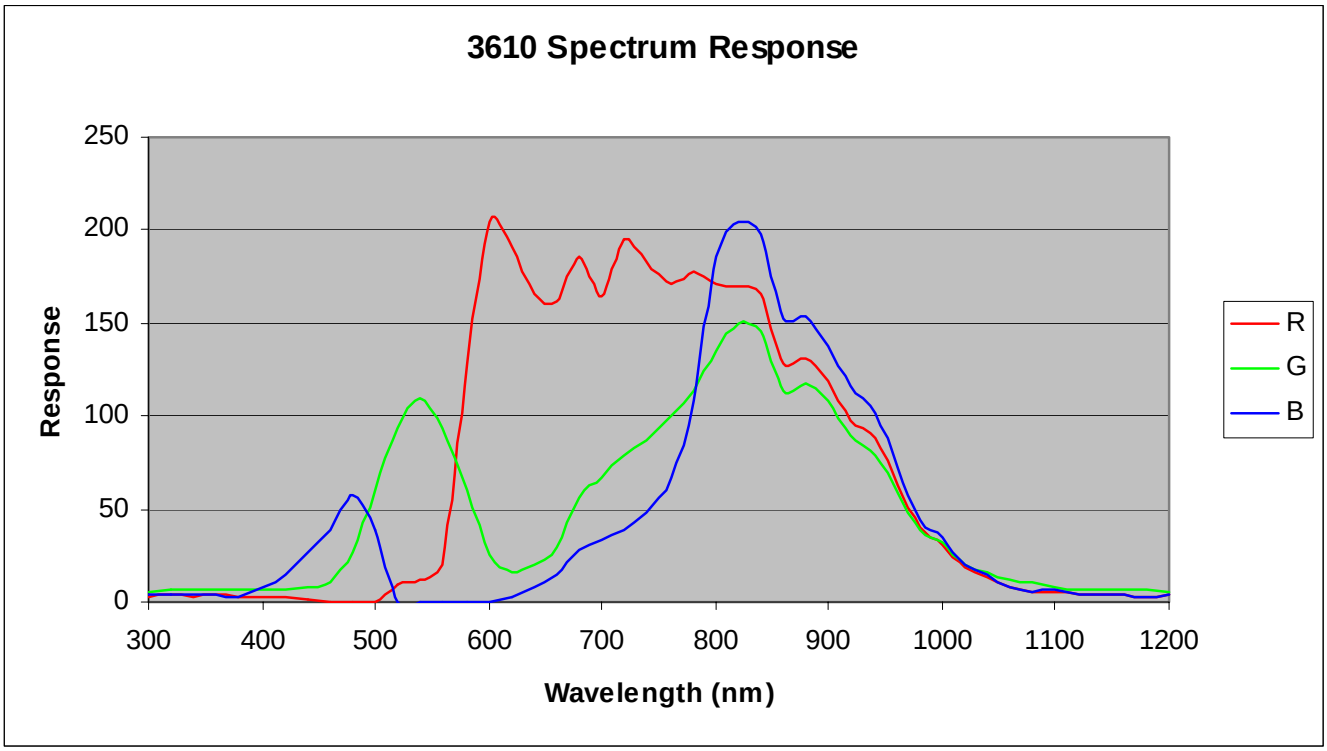
Figure 23 Frame Exposure Mode Register Control Timing



Preliminary

OV3610 Light Response

Figure 24 OV3610 Light Response



Preli

Register Set

Table 11 provides a list and description of the Device Control registers contained in the OV3610. The device slave addresses for the OV3610 are 60 for write and 61 for read.

Table 11 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
00	GAIN	00	RW	AGC Gain control setting Bit[7:6]: Reserved Bit[5:0]: Gain control gain setting • Range: 1x to 8x Gain = (Bit[5]+1) x (Bit[4]+1) x (1+Bit[3:0]/16) ***Note:*** *Set COMI[0] = 0 to disable AGC.*
01	BLUE	80	RW	Blue Gain Control • Range: 1/3x to 3x If BLUE[7] = 1, then Blue gain = 1 + BLUE[6:0]/64 If BLUE[7] = 0, then Blue gain = 1/(1 + BLUE_B[6:0]/64), where BLUE_B[6:0] is the bit reverse of BLUE[6:0].
02	RED	80	RW	Red Gain Control • Range: 1/3x to 3x If RED[9] = 1, then Red gain = 1 + RED[6:0]/64 If RED[9] = 0, then Red gain = 1/(1 + RED_B[6:0]/64), where RED_B[6:0] is the bit reverse of RED[6:0].
03	COMA	4A (41 in HF)	RW	Common Control A Bit[7:4]: AWB update threshold Bit[3:2]: Vertical window end line control 2 LSBs Bit[1:0]: Vertical window start line control 2 LSBs ***Note:*** *1. For maximum output window size of 2054x1540 in QXGA mode, value of this register should be 0x4D.* *2. For maximum output window size of 1032x768 in XGA mode, value of this register should be 0x45.* *3. For maximum output window size of 1032x510 in DV mode, value of this register should be 0x45.* *4. For maximum output window size of 1032x190 in HF mode, value of this register should be 0x45.*

Preliminary

Table 11 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
04	COMB	00	RW	Common Control B Bit[7:6]: AWB Step Selection 00: 255 steps 01: 64 steps 10: 128 steps 11: 64 steps Bit[5:4]: AWB Update Speed Selection 00: Slow 01: Slowest 10: Fast 11: Fast Bit[3]: Reserved Bit[2:0]: AEC lower 3 bits – AEC[2:0]
05	BAVG	00	RW	B Channel Average
06	GbAVG	00	RW	G Channel Average - Picked G pixels in the same line with B pixels.
07	GrAVG	00	RW	G Channel Average - Picked G pixels in the same line with R pixels.
08	RAVG	00	RW	R Channel Average
09	COMC	01	RW	Common Control C Bit[7:5]: Reserved Bit[4]: Sleep mode enable 0: Normal mode 1: Sleep mode Bit[3:2]: Sensor sampling reset timing selection 00: Normal reset time 01: Long reset time 10: Longer reset time 11: Longest reset time Bit[1:0]: Output drive current select 00: Weakest 01: Double capability 10: Double capability 11: Triple drive current
0A	PIDH	36	R	Product ID Number MSB (Read only)
0B	PIDL	10	R	Product ID Number LSB (Read only)

Preliminary

Table 11 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
0C	COMD	28	RW	Common Control D Bit[7]: Reserved Bit[6]: Swap MSB and LSB at the output port Bit[5:3]: Reserved Bit[2]: Output average ON/OFF 0: Output normal 1: Output average of 2 to 4 pixels depending on COME[7] setting Bit[1]: Sensor precharge voltage selection 0: Selects internal reference as precharge voltage 1: Selects SVDD as precharge voltage Bit[0]: Snapshot option 0: Enable live video output after snapshot sequence 1: Output single frame only
0D	COME	00	RW	Common Control E Bit[7]: Output average option If COMD[2] = 1, then: 0: Output average of 2 pixels 1: Output average of 4 pixels If COMD[2] = 1, then output normal Bit[6]: Anti-blooming control 0: Anti-blooming ON 1: Anti-blooming OFF Bit[5:3]: Reserved Bit[2]: Clock output power-down pin status 0: Tri-state data output pin at power-down 1: Data output pin hold at last status before power-down Bit[1]: Data output pin status selection at power-down 0: Tri-state VSYNC, PCLK, HREF and CHSYNC pins upon power-down 1: VSYNC, PCLK, HREF and CHSYNC hold on last states before power-down Bit[0]: Auto zero circuit ON/OFF select 0: OFF 1: ON
0E	COMF	15	RW	Common Control F Bit[7]: System clock selection 0: Use 24 MHz system clock 1: Use 48 MHz system clock Bit[6:4]: Reserved Bit[3]: Manual/auto negative offset canceling selection 0: Auto detect negative offset and cancel it 1: Manual set negative offset compensation ON/OFF. Negative offset bias stored in register OFCC and compensation ON/OFF in register NOFC. Bit[2:0]: Reserved

Preliminary

Table 11 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
0F	COMG	47	RW	Common Control G Bit[7]: Optical black output selection 0: Disable 1: Enable Bit[6]: Black level calibrate selection 0: Use electrical black reference 1: Use optical black pixels to calibrate Bit[5:4]: Reserved Bit[3]: Channel offset adjustment 0: Disable offset adjustment 1: Enable offset adjustment. B/Gb/Gr/R channel offset levels stored in registers BBIAS, GbBIAS, GrBIAS, and RBIAS Bit[2]: ADC black level calibration option 0: Use B/G line and G/R line to calibrate each channel's black level 1: Use only B/G line black level to calibrate all channels Bit[1]: Reserved Bit[0]: ADC black level calibration enable 0: Disable 1: Enable
10	AEC	43	RW	Automatic Exposure Control Most Significant 8 bits for AEC[10:3] (least significant 3 bits in register COMB[2:0]). Bit[10:0]: Exposure time (range in hex) QXGA: 0x01 - 0x60E XGA: 0x01 - 0x30C DV: 0x01 - 0x208 HF: 0x01 - 0xC8 $T_{EX} = t_{LINE}$ x AEC[10:0] ***Note:*** *Set COMI[2] to 0 to disable the AEC. Maximum exposure is 1048 x* T_{line}
11	CLKRC	00	RW	Clock Rate Control Bit[7]: Internal frequency doublers ON/OFF selection 0: OFF 1: ON Bit[6]: Digital video port master/slave selection 0: Master mode, sensor provides PCLK 1: Slave mode, external PCLK input from XCLK1 pin Bit[5:0]: Clock divider CLK = XCLK1/(decimal value of CLKRC[5:0] + 1)

Preliminary

Table 11 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
12	COMH	20	RW	Common Control H Bit[7]: SRST 1: Initiates soft reset. All register are set to factory default values after which the chip resumes normal operation Bit[6:4]: Resolution selection 000: QXGA 001: High Frame rate (HF) mode 010: Digital video (DV) mode 100: XGA Bit[3]: Master/slave selection 0: Master mode 1: Slave mode Bit[2]: Internal B/R channel option 0: B/R use same channel 1: B/R use different channels Bit[1]: Color bar test pattern 0: OFF 1: ON Bit[0]: Reserved
13	COMI	C7	RW	Common Control I Bit[7]: AEC speed selection 0: Normal 1: Faster AEC correction Bit[6]: AEC speed/step selection 0: Small steps, slow 1: Big steps, fast Bit[5]: Banding filter ON/OFF 0: OFF 1: ON, set minimum exposure to 1/120s Bit[4]: Banding filter option 0: Set to 0, if main clock is 48 MHz and the PLL is ON. 1: Set to 1, if main clock is 24 MHz with the PLL ON or the main clock is 48 MHz with the PLL OFF. Bit[3]: Reserved Bit[2]: AGC auto/manual control selection 0: Manual 1: Auto Bit[1]: AWB auto/manual control selection 0: Manual 1: Auto Bit[0]: Exposure control 0: Manual 1: Auto

Preliminary

Table 11 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
14	COMJ	40	RW	Common Control J Bit[7:6]: AGC gain ceiling 00: 2x 01: 4x 10: 8x 11: 8x Bit[5:4]: Reserved Bit[3]: Auto banding filter 0: Banding filter is always ON/OFF depending on COMI[5] setting. 1: Automatically disable the banding filter if light is low Bit[2]: VSYNC drop option 0: VSYNC is always output 1: VSYNC is dropped if frame data is dropped Bit[1]: Frame data drop 0: Disable data drop 1: Drop frame data if exposure is not within tolerance. In AEC mode, data is normally dropped when data is out of range. Bit[0]: Reserved
15	COMK	00	RW	Common Control K Bit[7]: CHSYNC pin output swap 0: CHSYNC 1: HREF Bit[6]: HREF pin output swap 0: HREF 1: CHSYNC Bit[5]: PCLK output selection 0: PCLK always output 1: PCLK output qualified by HREF Bit[4]: PCLK edge selection 0: Data valid on PCLK falling edge 1: Data valid on PCLK rising edge Bit[3]: HREF output polarity 0: Output positive HREF 1: Output negative HREF, HREF negative for data valid Bit2]: Reserved Bit[1]: VSYNC polarity 0: Positive 1: Negative Bit[0]: HSYNC polarity 0: Positive 1: Negative
16	OFCC	00	RW	Offset Canceling Control Bit[7:4]: ADBLC negative offset bias. If ADBLC value is lower than this bias value, chip will add a positive offset to AD input if COMF[3] = 1. Bit3:0]: Reserved

Preliminary

Table 11 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
17	HREFST	10 (1F in XGA, HF)	RW	Horizontal Window Start most significant 8 bits, 3 least significant bits in COMM[2:0] Bit[10:0]: Select beginning of horizontal window, each LSB represents two pixels ***Note:*** *1. For maximum output window size of 2054x1540 in QXGA mode, minimum value of this register is 0x10.* *2. For maximum output window size of 1032x768 in XGA mode, minimum value of this register is 0x1F.* *3. For maximum output window size of 1032x510 in DV mode, minimum value of this register is 0x1F.* *4. For maximum output window size of 1032x190 in HF mode, minimum value of this register is 0x1F.*
18	HREFEND	90 (5F in XGA, HF)	RW	Horizontal Window End most significant 8 bits, 3 least significant bits in COMM[5:3] Bit[10:0]: Select end of horizontal window, each LSB represents two pixels ***Note:*** *1. For maximum output window size of 2054x1540 in QXGA mode, minimum value of this register is 0x90.* *2. For maximum output window size of 1032x768 in XGA mode, minimum value of this register is 0x5F.* *3. For maximum output window size of 1032x510 in DV mode, minimum value of this register is 0x5F.* *4. For maximum output window size of 1032x190 in HF mode, minimum value of this register is 0x5F.*
19	VSTRT	00	RW	Vertical Window line start most significant 8 bits, 2 LSBs in register COMA[1:0] Bit[9:0]: Selects the start of the vertical window, each LSB represents two scan lines. ***Note:*** *1. For maximum output window size of 2054x1540 in QXGA mode, minimum value of this register is 0x00.* *2. For maximum output window size of 1032x768 in XGA mode, minimum value of this register is 0x00.* *3. For maximum output window size of 1032x510 in DV mode, minimum value of this register is 0x00.* *4. For maximum output window size of 1032x190 in HF mode, minimum value of this register is 0x00.*

Preliminary

Table 11 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
1A	VEND	C0 (68 in XGA and 18 in HF)	RW	Vertical Window line end most significant 8 bits, 2 LSBs in register COMA[3:2] Bit[9:0]: Selects the end of the vertical window, each LSB represents two scan lines. ***Note:*** *1. For maximum output window size of 2054x1540 in QXGA mode, minimum value of this register is 0xD0.* *2. For maximum output window size of 1032x768 in XGA mode, minimum value of this register is 0x60* *3. For maximum output window size of 1032x510 in DV mode, minimum value of this register is 0x40.* *4. For maximum output window size of 1032x190 in HF mode, minimum value of this register is 0x18.*
1B	PSHFT	00	RW	Pixel Shift Bit[7:0]: Pixel delay count - provides a method to fine tune the output timing of the pixel data relative to the HREF pulse. It physically shifts the video data output time in units of pixel clock counts. The largest delay count is [FF] and is equal to 255 x PCLK.
1C	MIDH	7F	R	Manufacturer ID Byte – High (Read only = 0x7F)
1D	MIDL	A2	R	Manufacturer ID Byte – Low (Read only = 0xA2)
1E-1F	RSVD	XX	–	Reserved
20	BOFF	80	RW	B Channel Offset Adjustment - auto controlled by internal circuit if COMG[0] = 1 Bit[7]: Offset direction 0: Add BOFF[6:0] to B channel 1: Subtract BOFF[6:0] from B channel Bit[6:0]: B channel offset adjustment value
21	GbOFF	80	RW	Gb Channel Offset Adjustment - auto controlled by internal circuit if COMG[0] = 1 Bit[7]: Offset direction 0: Add GbOFF[6:0] to Gb channel 1: Subtract GbOFF[6:0] from Gb channel Bit[6:0]: Gb channel offset adjustment value
22	GrOFF	80	RW	Gr Channel Offset Adjustment - auto controlled by internal circuit if COMG[0] = 1 Bit[7]: Offset direction 0: Add GrOFF[6:0] to Gr channel 1: Subtract GrOFF[6:0] from Gr channel Bit[6:0]: Gr channel offset adjustment value
23	ROFF	80	RW	R Channel Offset Adjustment - auto controlled by internal circuit if COMG[0] = 1 Bit[7]: Offset direction 0: Add ROFF[6:0] to R channel 1: Subtract ROFF[6:0] from R channel Bit[6:0]: R channel offset adjustment value

Preliminary

Table 11 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
24	AEW	78	RW	Luminance Signal High Range for AEC/AGC operation AEC/AGC value decreases in auto mode when average luminance is greater than AEW[7:0]
25	AEB	68	RW	Luminance Signal Low Range for AEC/AGC operation AEC/AGC value increases in auto mode when average luminance is less than AEB[7:0]
26	VV	D4	RW	Fast Mode Large Step Range Thresholds - effective only in AEC/AGC fast mode Bit[7:4]: High threshold Bit[3:0]: Low threshold AEC/AGC may change in larger steps when luminance average is greater than VV[7:4] or less than VV[3:0]
27	BBIAS	80	RW	B Channel Offset Manual Adjustment Value - effective only when COMG[3] = 1 Bit[7]: Offset direction 0: Add BBIAS[6:0] to B channel 1: Subtract BBIAS[6:0] from B channel Bit[6:0]: B channel offset manual adjustment value
28	GbBIAS	80	RW	Gb Channel Offset Manual Adjustment Value - effective only when COMG[3] = 1 Bit[7]: Offset direction 0: Add GbBIAS[6:0] to Gb channel 1: Subtract GbBIAS[6:0] from Gb channel Bit[6:0]: Gb channel offset manual adjustment value
29	GrBIAS	80	RW	Gr Channel Offset Manual Adjustment Value - effective only when COMG[3] = 1 Bit[7]: Offset direction 0: Add GrBIAS[6:0] to Gr channel 1: Subtract GrBIAS[6:0] from Gr channel Bit[6:0]: Gr channel offset manual adjustment value
2A	COML	00	RW	Common Control L Bit[7]: Reserved - must be set to "0" Bit[6:4]: Line interval adjust value MSB 3 bits, LSBs in register FRARL[7:0] Bit[3:2]: HSYNC timing end point adjustment MSB 2 bits Bit[1:0]: HSYNC timing start point adjustment MSB 2 bits
2B	FRARL	00	RW	Line Interval Adjustment Value LSB 8 bits The frame rate will be adjusted by changing the line interval. Each LSB will add 1/2320 T_{frame} in QXGA and 1/1536 T_{frame} in XGA mode to the frame period. For the maximum dummy pixel number: COML[6:4] : FRARL[7:0] = 110 : 11110001 = 1777

Preliminary

Table 11 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
2C	RBIAS	80	RW	R Channel Offset Manual Adjustment Value - effective only when COMG[3] = 1 Bit[7]: Offset direction 0: Add RBIAS[6:0] to R channel 1: Subtract RBIAS[6:0] from R channel Bit[6:0]: R channel offset manual adjustment value
2D	ADDVSL	00	RW	VSYNC Pulse Width LSB 8 bits Bit[7:0]: Line periods added to VSYNC width. Default VSYNC output width is 4 x t_{line}. Each LSB count will add 1 x t_{line} to the VSYNC active period.
2E	ADDVSH	00	RW	VSYNC Pulse width MSB 8 bits Bit[7:0]: Line periods added to VSYNC width. Default VSYNC output width is 4 x t_{line}. Each MSB count will add 256 x t_{line} to the VSYNC active period.
2F	YAVG	00	RW	Luminance Average Average luminance is calculated from the B/Gb/Gr/R channel average as follows: B/Gb/Gr/R channel average = (BAVG[7:0] + GbAVG[7:0] + GrAVG[7:0] +RAVG[7:0]) x 0.25
30	HSDY	08	RW	HSYNC Position and Width Start LSB 8 bits This register and COML[1:0] define the HSYNC start position. Each LSB will shift HSYNC starting point by a 2 pixel period.
31	HEDY	30	RW	HSYNC Position and Width End LSB 8 bits This register and COMLL[3:2] define the HSYNC end position. Each LSB will shift HSYNC end point by a 2 pixel period.
32	COMM	36 (29 in XGA, DV, HF)	RW	Common Control M Bit[7:6]: Pixel clock divide option 00: No effect on PCLK 01: No effect on PCLK 10: PCLK frequency divide by 2 11: PCLK frequency divide by 4 Bit[5:3]: Horizontal window end position LSBs Bit[2:0]: Horizontal window start position LSBs ***Note:*** *1. For maximum output window size of 2054x1540 in QXGA mode, value of this register should be 0x3C.* *2. For maximum output window size of 1032x768 in XGA mode, value of this register should be 0x3B.* *3. For maximum output window size of 1032x510 in DV mode, value of this register should be 0x3B.* *4. For maximum output window size of 1032x190 in HF mode, value of this register should be 0x3B.*

Preliminary

Table 11 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
33	CHLF	C0	RW	Current Control Bit[7:6]: Sensor current control • Range: [00] minimum to [11] maximum Bit[5]: Sensor current range control 0: CHLF[7:6] current control at normal range 1: CHLF[7:6] current control at half range Bit[4]: Sensor current double ON/OFF 0: Normal 1: Double current Bit[3]: Sensor buffer current control 0: Normal 1: Half current Bit[2]: Column buffer current control 0: Normal 1: Half current Bit[1]: Analog DSP current control 0: Normal 1: Half current Bit[0]: ADC current control 0: Normal 1: Half current
34	VBLM	1B	RW	Blooming Control Bit[7]: Hard/soft reset switch 0: Hard reset 1: Soft reset Bit[6:4]: Blooming voltage selection • Range: [000] lowest voltage to [111] highest voltage Bit[3:0]: Sensor current control
35	VREF	E0	RW	Reference Voltage Control Bit[7:5]: Column high reference control 000: Lowest voltage 011: Highest voltage 1xx: Column high reference connect to VDD Bit[4:2]: Column low reference control 000: Lowest voltage 011: Highest voltage 1xx: Column low reference connect to GND Bit[1:0]: Reserved
36	VCHG	17	RW	Sensor Precharge Voltage Control Bit[7]: Reserved Bit[6:4]: Sensor precharge voltage control • Range: [000] lowest voltage to [111] highest voltage Bit[3:0]: Sensor array common reference • Range: [000] lowest voltage to [111] highest voltage

Preliminary

Table 11 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
37	ADC	04	RW	ADC Reference Control Bit[7:4]: Reserved Bit[3]: ADC input signal range 0: Input signal x1 1: Input signal x0.7 Bit[2:0]: ADC range control • Range: [000] minimum to [111] maximum
38	ACOM	12	RW	Analog Common Control Bit[7]: Analog gain control 0: Normal 1: Increase gain 2x Bit[6]: Analog black level calibration control 0: Analog BLC ON 1: Analog BLC OFF Bit[5:0]: Reserved
39	NOFC	00	RW	Negative Offset Compensation ON/OFF Bit[7]: Gb negative compensation ON/OFF 0: OFF 1: ON Bit[6]: Gr negative compensation ON/OFF 0: OFF 1: ON Bit[5]: B negative compensation ON/OFF 0: OFF 1: ON Bit[4]: R negative compensation ON/OFF 0: OFF 1: ON Bit[3:0]: Sensor array current control • Range: [000] minimum to [111] maximum
3A	FREFA	00	RW	Internal Reference Adjustment • Range: [00] to [FF]
3B	FREFB	00	RW	Internal Reference Adjustment • Range: [00] to [FF]
3C	FVOPT	00	RW	Internal Reference Adjustment • Range: [00] to [FF]

Preliminary

Package Specifications

The OV3610 uses a 48-pin ceramic package. Refer to Figure 25 for package information and Figure 26 for the array center on the chip.

Figure 25 OV3610 Package Specifications

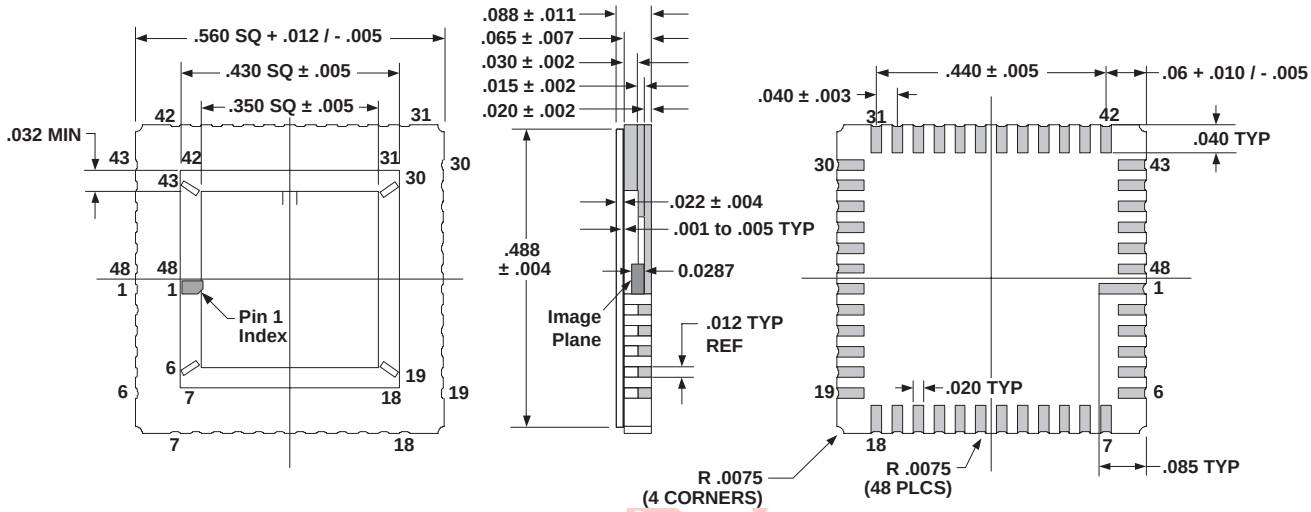


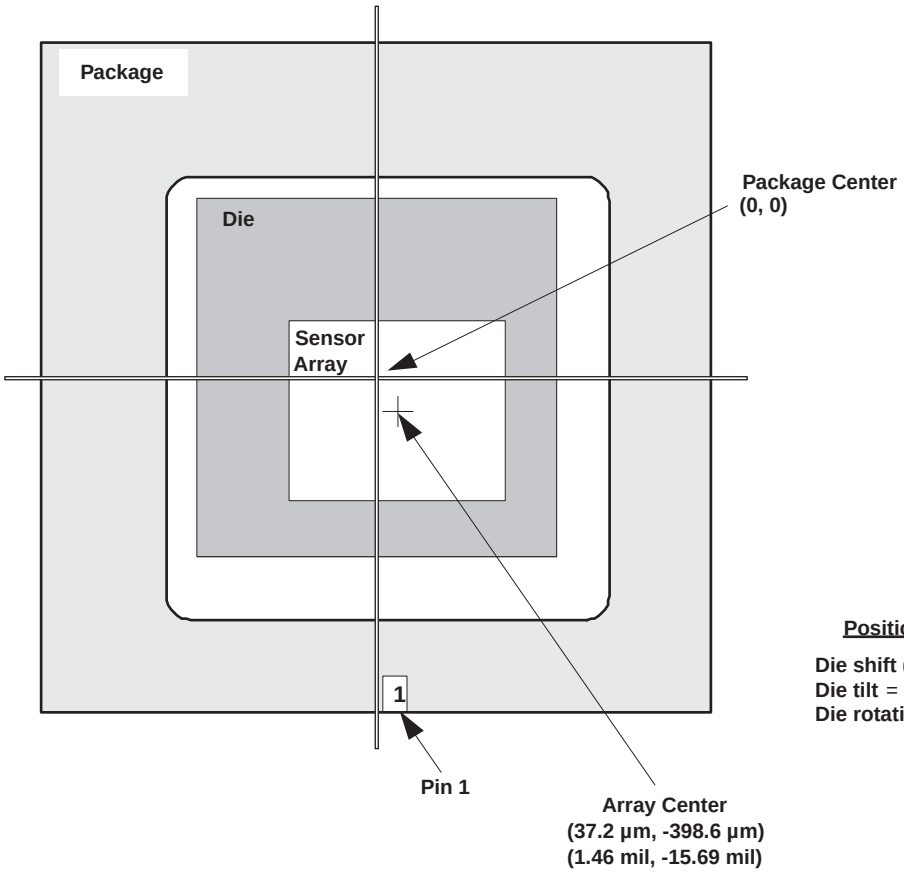
Table 12 OV3610 Package Dimensions

Dimensions	Millimeters (mm)	Inches (in.)
Package Size	14.22 + 0.30 / -0.13 SQ	.560 + .012 / - .005 SQ
Package Height	2.23 ± 0.28	.088 ± .011
Substrate Height	0.51 ± 0.05	.020 ± .002
Cavity Size	8.89 ± 0.13 SQ	.350 ± .005 SQ
Castellation Height	1.14 ± 0.13	.045 ± .005
Pin #1 Pad Size	0.51 x 2.16	.020 x .085
Pad Size	0.51 x 1.02	.020 x .040
Pad Pitch	1.02 ± 0.08	.040 ± .003
Package Edge to First Lead Center	1.524 + 0.25 / -0.13	.06 + .010 / - .005
End-to-End Pad Center-Center	11.18 ± 0.13	.440 ± .005
Glass Size	12.40 ± 0.10 SQ / 13.00 ± 0.10 SQ	.488 ± .004 SQ / .512 ± .004 SQ
Glass Height	0.55 ± 0.05	.022 ± .002

Preliminary

Sensor Array Center

Figure 26 OV3610 Sensor Array Center



Positional Tolerance s

Die shift (x,y) = 0.15 mm (6 mils) max.
Die tilt = 1 degrees max.
Die rotation = 3 degrees max.

Important: Most optical systems invert and mirror the image so the chip is usually mounted on the board with pin 1 (SVDD) down as shown.

NOTE: Picture is for reference only, not to scale.

The recommended lens chief ray angle for the OV3610 is 10.6 degrees.

PRELIMINARY

Note:

- *All information shown herein is current as of the revision and publication date. Please refer to the OmniVision web site (http://www.ovt.com) to obtain the current versions of all documentation.*

- *OmniVision Technologies, Inc. reserves the right to make changes to their products or to discontinue any product or service without further notice (It is advisable to obtain current product documentation prior to placing orders).*

- *Reproduction of information in OmniVision product documentation and specifications is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations and notices. In such cases, OmniVision is not responsible or liable for any information reproduced.*

- *This document is provided with no warranties whatsoever, including any warranty of merchantability, non-infringement, fitness for any particular purpose, or any warranty otherwise arising out of any proposal, specification or sample. Furthermore, OmniVision Technologies Inc. disclaims all liability, including liability for infringement of any proprietary rights, relating to use of information in this document. No license, expressed or implied, by estoppels or otherwise, to any intellectual property rights is granted herein.*

- *'OmniVision', 'CameraChip' are trademarks of OmniVision Technologies, Inc. All other trade, product or service names referenced in this release may be trademarks or registered trademarks of their respective holders. Third-party brands, names, and trademarks are the property of their respective owners.*

For further information, please feel free to contact OmniVision at info@ovt.com.

Preliminary

OmniVision Technologies, Inc.
1341 Orleans Drive
Sunnyvale, CA USA
(408) 542-3000