Agilent Technologies
Innovating the HP Way

Infrared IrDA® Compliant 4 Mb/s 3.3 V Transceiver

Technical Data

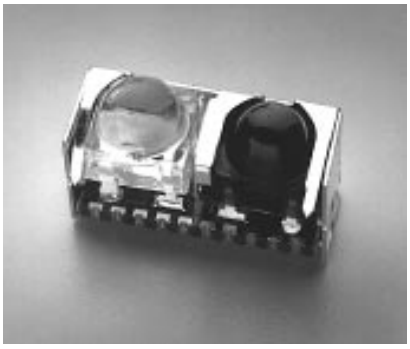
HSDL-2300

Features

- **Fully Compliant to IrDA 1.0/1.1 Specifications**
  - **115.2 kb/s to 4 Mb/s Operation**
  - **Excellent Nose-to-Nose Operation**
- **Compatible with HP-SIR and TV Remote**
- **Backward Compatible to Slower Speed**
- **IEC825-Class 1 Eye Safe**
- **3.3 V Performance**
- **Complete Shutdown**
  - **TXD, RXD, PIN Diode**
- **Low Shutdown Current**
  - **10 nA Typical**
- **Adjustable Optical Power Management**
  - **Adjust LED Drive Current to Maintain Link Integrity**
- **Single RX Data Output**
  - **FIR Select Pin Switch to FIR**
- **Small 3.3 V Module Package**
  - **Height of 5.5 mm Maximum**
- **Integrated EMI Shield**
  - **Excellent Noise Immunity**
- **Minimum Number of Passive Components**
  - **One RLED Resistor and Two Bypass Capacitors**
- **Enhanced Reliability Performance**
- **Designed to Accommodate Light Loss with Cosmetic Window**
- **Interfaces to Various Super I/O and Controller Devices**
- **Edge Detection Input**
  - **To Prevent LED from Long Turn-On Time**
- **Typical Link Distance > 1 m at 4 Mb/s**

Applications

- **Data Communication**
  - **Notebook Computers**
  - **Sub-Notebook Computers**
  - **Desktop PCs**
  - **Printers**
  - **Personal Digital Assistance (PDAs)**
  - **Fax/Photocopiers**
- **Digital Imaging**
  - **Digital Cameras**
  - **Photo-Imaging Printers**
- **Industrial and Medical Instrumentation**
  - **General Data Collection Devices**
  - **Patient and Pharmaceutical Data Collection**
- **IR LANs**



Description

The HSDL-2300 is a new generation 3.3 V power supply infrared transceiver module that provides interface between logic and IR signals for through-air, serial, half-duplex IR data link. The module is compliant to IrDA Physical Layer Specifications 1.0/1.1 and is IEC825-Class 1 Eye Safe.

Package

The HSDL-2300 module consists of Optical Sub-Assemblies (OSAs), an Electrical Sub-Assembly (ESA), and an integrated EMI shield. There are two package options: Option #001 with guide pins, and Option #002 without guide pins. Drawings of the two options package are illustrated in Figure 3 and Figure 4.

New Package Benefits

The new package that consists of OSAs and ESA with the combination of integrated EMI shield utilizes existing in-house high-volume assembly processes to ensure high quality and high volume supply. The integrated EMI shield helps to ensure low EMI emission and high immunity to EMI field, thus enhancing reliable performance.

Optical Sub-Assemblies (OSAs)

The Optical Sub-Assemblies include a Transmitter and a Receiver.

The Transmitter has a discrete emitter that utilizes Transparent-Substrate Aluminium Gallium Arsenide (TS AlGaAs) LED technology that offers high-speed and high optical output efficiency performance with an integral lens in a clear molded package.

The Receiver utilizes a discrete silicon PIN photo-diode with an integral lens in a molded package and contains a dye to absorb visible light. The Receiver lens is designed such that it magnifies the effective area of the PIN photo-diode to enhance sensitivity. And the PIN photo-diode and pre-amplifier power supplies are filtered to attenuate noise from external sources.

Electrical Sub-Assembly (ESA)

The Electrical Sub-Assembly (ESA) consists of a double-sided printed circuit board on which a BiCMOS Integrated Circuit (IC) and various surface-mount passive circuit elements are attached. The IC contains an LED driver and a receiver that provides a single output channel, RXD.

Application Information

The Application Engineering group in Agilent's Communications Semiconductor Solution Division is available to assist you with the technical understanding associated with HSDL-2300 infrared transceiver module. You can contact them through your local sales

I/O Pins Configuration Table

Pin	Description	Symbol
1	LED Anode	LEDA
2	Transmitter Data Input	TXD
3	Receiver Data Output	RXD
4	Ground	GND
5	Ground	GND
6	Mode 1	MD1
7	Mode 0	MD0
8	FIR Select	FIR_SEL
9	Analog Ground	AGND
10	Supply Voltage	V_{CC}

CAUTION: The BiCMOS inherent to the design of this component increases the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Transceiver Control Truth Table

Mode 0	Mode 1	FIR_SEL	RX Function	TX Function
1	0	X	Shutdown	Shutdown
0	0	0	SIR	Full Distance Power
0	1	0	SIR	2/3 Distance Power
1	1	0	SIR	1/3 Distance Power
0	0	1	MIR/FIR	Full Distance Power
0	1	1	MIR/FIR	2/3 Distance Power
1	1	1	MIR/FIR	1/3 Distance Power

X = Don't Care.

Transceiver I/O Truth Table

Input		Output		
TXD	**EI**	**IE (LED)**	**SIR[4]**	**MIR/FIR[5]**
V_{IH}	X	High (On)	NV	NV
V_{IL}	EI_H[1]	Low (Off)	Low[3]	NV
V_{IL}	EI_H[2]	Low (Off)	NV	Low[3]
V_{IL}	EI_L	Low (Off)	High	High

X = Don't care
NV = Not Valid

Notes:
1. In-band EI ≤ 115.2 kb/s.
2. In-band EI ≥ 0.576 Mb/s.
3. Logic Low is a pulsed response. The condition is maintained for a duration dependent on pattern and strength of the incident intensity.
4. SIR defined as the data rate from 2.4 kb/s to 115.2 kb/s.
5. MIR/FIR defined as the data rate from 0.576 Mb/s to 4.0 Mb/s.

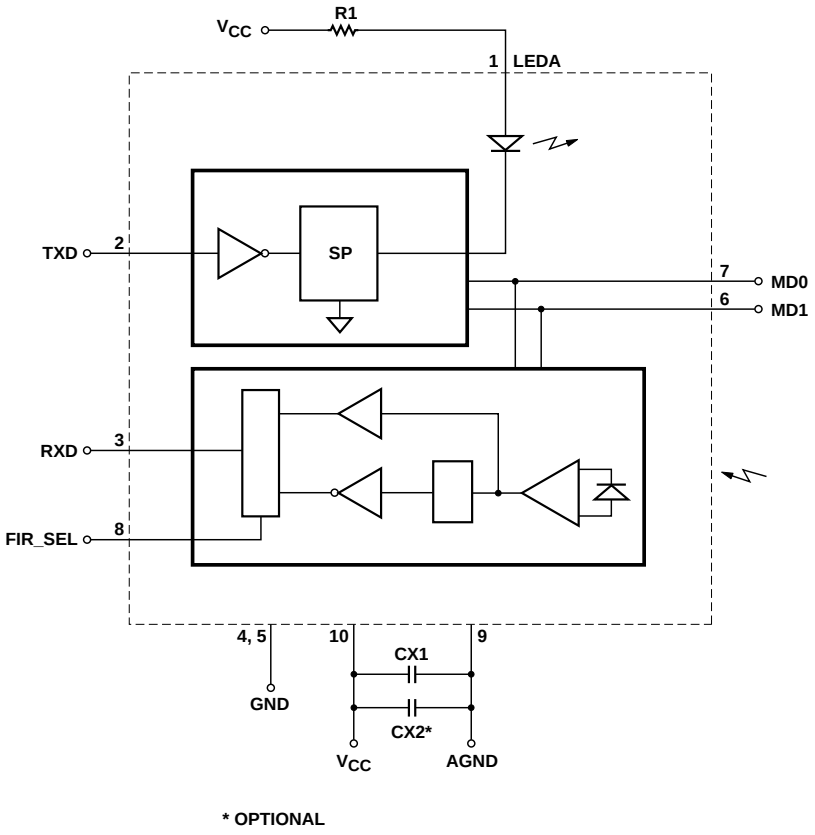


Figure 1. HSDL-2300 Application Circuit Diagram.

Recommended Application Circuit Components

Component	Recommended Value
R1	2.2 Ω, ± 5%, 0.5 Watt, for 3.0 ≤ V_{CC} ≤ 3.6 V operation
CX1[1]	0.47 µF, ± 20%, X7R Ceramic
CX2[2]	6.8 µF, ± 20%, Tantalum

Notes:

1. CX1 must be placed within 0.7 cm of the HSDL-2300 to obtain optimum noise immunity.
2. In environments with noisy power supplies, supply rejection can be enhanced by including CX2 as shown in Application Circuit Diagram, Figure 1.
3. For interface between 5 V endec and HSDL-2300, level shifters or external protection circuits are recommended at all input pins; MD0, MD1, TXD, and FIR_SEL.

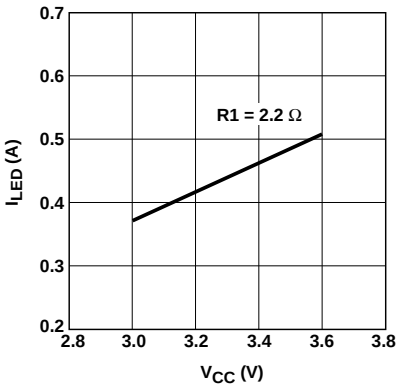


Figure 2. Selection of Resistor R1.

Absolute Maximum Ratings[1]

Parameter	Symbol	Min.	Max.	Units	Conditions
Storage Temperature	T_S	–20	85	°C	
Operating Temperature	T_A	0	70	°C	
Average LED Current	I_{LED} (DC1)		100	mA	
Average LED Current	I_{LED} (DC2)		165	mA	≤ 90 µs Pulse Width, ≤ 25% Duty Cycle
Repetitive Pulsed LED Current	I_{LED} (RP)		650	mA	≤ 90 µs Pulse Width, ≤ 25% Duty Cycle
Peak LED Current	I_{LED} (PK)		750	mA	≤ 2 µs Pulse Width, ≤ 10% Duty Cycle
LED Anode Voltage	V_{LEDA}	–0.5	7	V	
Supply Voltage	V_{CC}	–0.5	7	V	
Transmitter Data Input Current	I_{TXD} (DC)	–12	12	mA	
Receiver Data Output Voltage	V_{RXD}	–0.5	V_{CC}+ 0.5	V	I_O(RXD) = –20 µA

Note:
1. For implementations where case to ambient thermal resistance ≤ 50°C/W.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Conditions
Operating Temperature	T_A	0	70	°C	
Supply Voltage	V_{CC}	3.0	3.6	V	
Logic High Input Voltage (TXD, MD0, MD1, FIR_SEL)	V_{IH}	2 V_{CC}/3	V_{CC}	V	
Logic Low Input Voltage (TXD, MD0, MD1, FIR_SEL)	V_{IL}	0	V_{CC}/3	V	
Logic High Receiver Input Irradiance	EI_H	0.0036 0.0090	500 500	mW/cm^2 mW/cm^2	For in-band signals ≤ 115.2 kb/s[1] 0.576 Mb/s ≤ in-band signals ≤ 4.0 Mb/s[1]
Logic Low Receiver Input Irradiance	EI_L		0.3	$\mu W/cm^2$	For in-band signals[1]
LED (Logic High) Current Pulse Amplitude	I_{LEDA}	400	650	mA	
Receiver Signal Rate – SIR		2.4	115.2	kb/s	
Receiver Signal Rate – MIR/FIR		0.576	4	Mb/s	
Ambient Light					See IrDA Serial Infrared Physical Layer Link Specification, Appendix A for ambient levels.

Note:
1. An in-band optical signal is a pulse/sequence where the peak wavelength, λp, is defined as 850 nm ≤ λp ≤ 900 nm, and the pulse characteristics are compliant with the IrDA Serial Infrared Physical Layer Link Specification.

Electrical and Optical Specifications

Test Conditions represent worst case values for the parameters under test. Specifications hold over the recommended operating conditions unless otherwise noted. Unspecified test conditions may be anywhere in their operating range. All values are at 25°C and 3.3 V unless otherwise noted.

Parameter		Symbol	Min.	Typ.	Max.	Units	Conditions
Receiver Data Output Voltage	Logic Low	V_{OL} (RXD)[1]	0		0.4V	V	I_{OL} (RXD) = 1.0 mA, For in-band EI ≥ 3.6 μW/cm^2, $\theta_{1/2} \leq 15°$
	Logic High	V_{OH} (RXD)	V_{CC}-0.2		V_{CC}	V	I_{OH} (RXD) = –20 μA, For in-band EI ≤ 0.3 μW/cm^2, $\theta_{1/2} \leq 15°$
	Viewing Angle	$2\theta_{1/2}$	30				
Transmitter Radiant Intensity	Logic High Intensity	EI_H	100	177		mW/sr	V_{IH} (TXD) ≥ 2 V_{CC}/3 I_{LEDA} = 400 mA, $\theta_{1/2} \leq 15°$
	Peak Wavelength	λp		875		nm	
	Spectral Line Half Width	σ $\lambda p_{1/2}$		35		nm	
	Viewing Angle	$2\theta_{1/2}$	30		60		
Digital Data Input Current	Logic Low/High	$I_{L/H}$	–1		1	μA	0 ≤ V_I ≤ V_{CC}
LED Anode On State Voltage		V_{ON} (LEDA)			2.4	V	I_{LEDA} = 400 mA, V_I (TXD) ≥ 2 V_{CC}/3
LED Anode Off State Leakage		I_{LK} (LEDA)		1	10	μA	V_{LEDA} = V_{CC} = 3.6 V, V_I (TXD) ≤ V_{CC}/3
Supply Current	Shutdown	I_{CC1}		10	200	nA	V_{CC} = 3.6 V
	Idle	I_{CC2}		2.5	4	mA	V_{CC} = 3.6 V, V_I (TXD) ≤ V_{IL}, EI = 0
	Active Receiver	I_{CC3}		27	30	mA	V_{CC} = 3.6 V, V_I (TXD) ≤ V_{IL} EI ≤ 500 mW/cm^2
Receiver Peak Sensitivity Wavelength		λp		880		nm	

Note:

1. Logic Low is a pulsed response. The condition is maintained for a duration dependent on pattern and strength of the incident intensity.

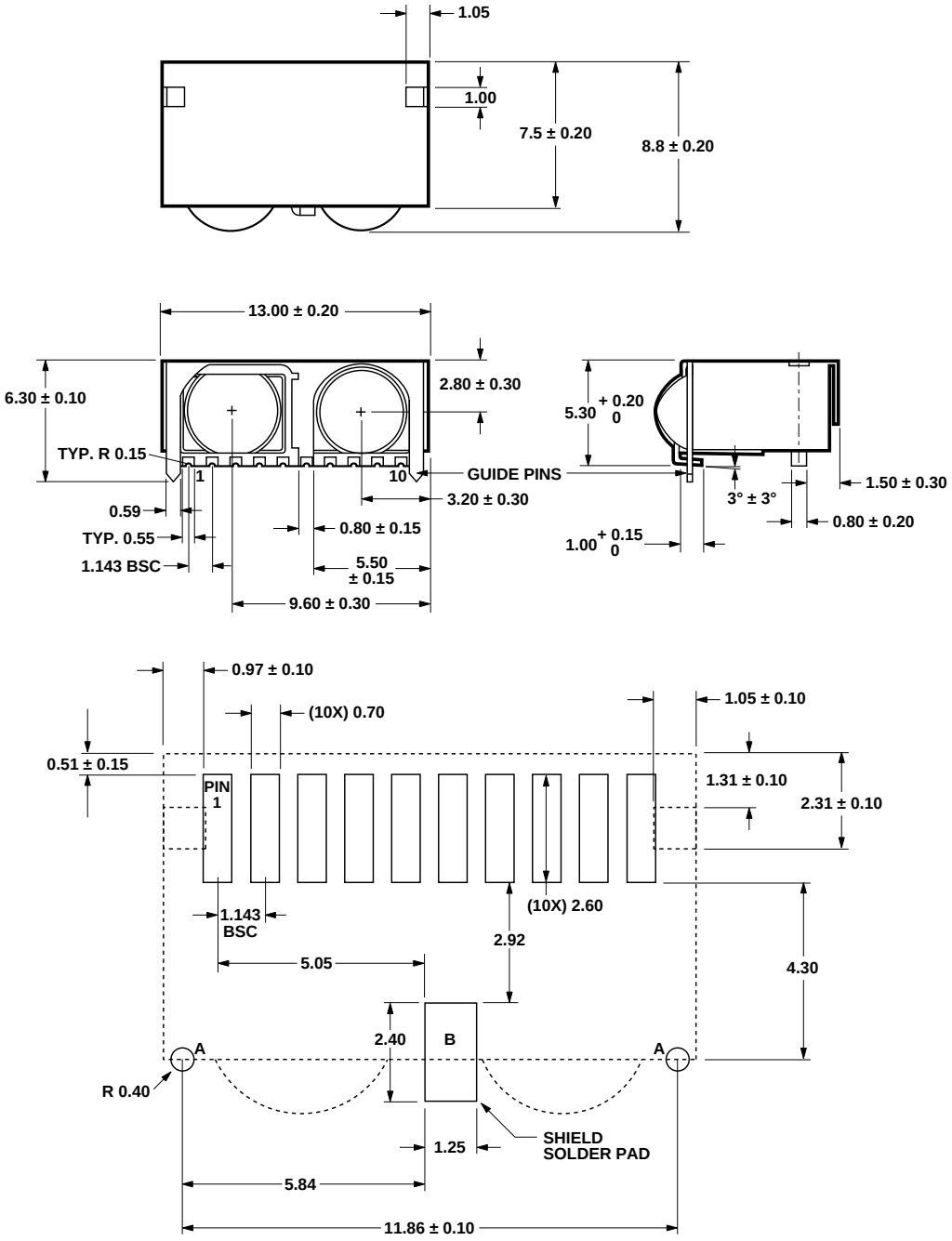
Switching Specifications

Test Conditions represent worst case values for the parameters under test. Specifications hold over the recommended operating conditions unless otherwise noted. Unspecified test conditions may be anywhere in their operating range. All values are at 25°C and 3.3 V unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Transmitter Radiant Intensity Pulse Width	t_{pw} (IE)	1.5	1.6	1.8	µs	t_{pw} (TXD) = 1.6 µs at 115.2 Kpulses/s
		148	217	260	ns	t_{pw} (TXD) = 217 ns at 1.15 Mpulses/s
		115	125	135	ns	t_{pw} (TXD) = 125 ns at 2.0 Mpulses/s
Transmitter Radiant Intensity Rise and Fall Times	$t_{r/f}$			40	ns	t_{pw} (TXD) = 125 ns at 2.0 Mpulses/s
Receiver SIR Pulse Width	t_{pw} (SIR)	2	2.5	3	µs	[1] $\phi_{1/2} \leq 15°$ C_L = 10 pF
Receiver MIR Pulse Width	t_{pw} (MIR)	100		500	ns	[4] $\phi_{1/2} \leq 15°$ C_L = 10 pF
Receiver FIR Pulse Width	t_{pw} (FIR)	85		165	ns	[2] $\phi_{1/2} \leq 15°$ C_L = 10 pF
Receiver ASK Pulse Width	t_{pw} (ASK)		1		µs	[3] 500 kHz/50% duty cycle carrier ASK, C_L = 10 pF
Receiver Rise/Fall Time	$t_{r/f}$ (RXD)		25		ns	C_L = 10 pF
Receiver Latency Time	t_L		20	50	µs	[1] [2]

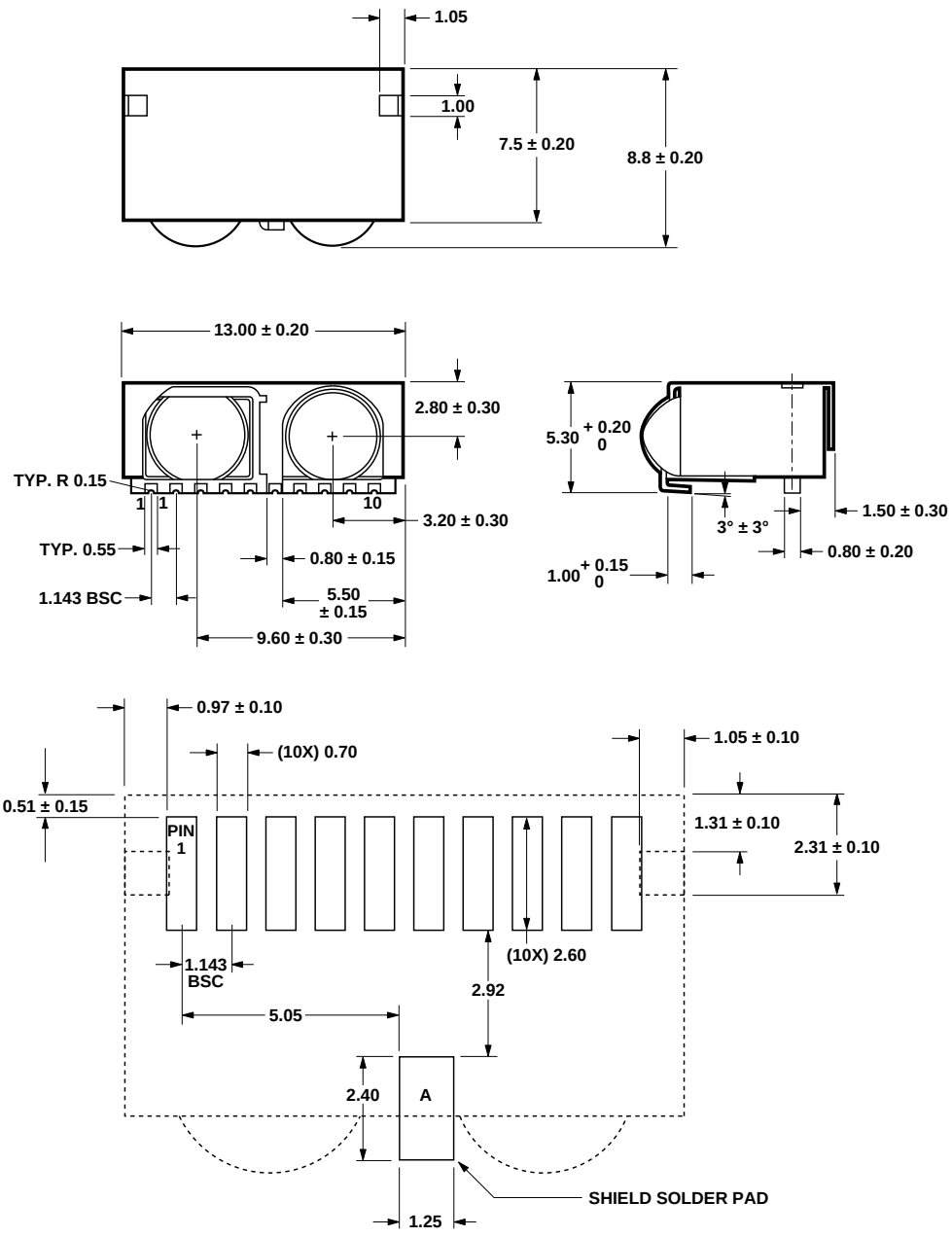
Notes:

1. For in-band signals ≤ 115.2 kb/s where 3.6 µW/cm^2 ≤ EI_L ≤ 500 mW/cm^2.
2. For in-band signals, 125 ns PW, 4 Mb/s, 4 ppm at recommended 400 mA drive current.
3. Pulse width specified is the pulse width of the second 500 kHz carrier pulse received in a data bit. The first 500 kHz carrier pulse may exceed 2 µs in width, which will not affect correct demodulation of the data stream. An ASK and DASK system using the HSDL-2300 has been shown to correctly receive all data bits for 9 µW/cm^2 < EI < 500 mW/cm^2 incoming signal strength. ASK or DASK should use the FIR channel enabled.
4. For in-band signals at 1.15 Mb/s where 9.0 µW/cm^2 ≤ EI ≤ 500 mW/cm^2.



NOTES:
1. RECOMMENDED SOLDER STENCIL TO BE 5 TO 6 MILS THICK.
2. LETTER 'A' INDICATES LOCATION OF THROUGH HOLE FOR SHIELD GUIDE PIN.
2. LETTER 'B' INDICATES LOCATION OF SHIELD SOLDERED GROUNDING PAD.

Figure 3. Package Outline with Dimension and Recommended PC Board Pad Layout. (Integrated EMI Shield with Guide Pins – Part Number: HSDL-2300#001.)



NOTES:
1. RECOMMENDED SOLDER STENCIL TO BE 5 TO 6 MILS THICK.
2. LETTER 'A' INDICATES LOCATION OF SHIELD SOLDERED GROUNDING PAD.

Figure 4. Package Outline with Dimension and Recommended PC Board Pad Layout. (Integrated EMI Shield without Guide Pins – Part Number: HSDL-2300#002.)

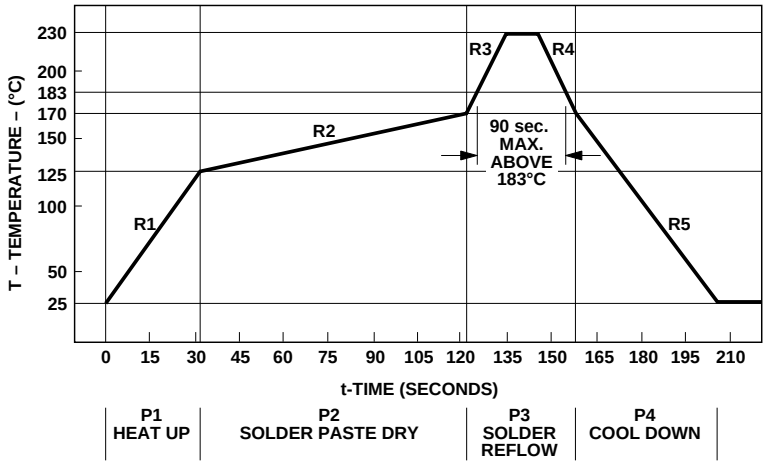


Figure 5. Reflow Profile.

Process Zone	Symbol	ΔT	ΔT/ΔTime
Heat Up	P1, R1	25°C to 125°C	3°C/s max.
Solder Paste Dry	P2, R2	125°C to 170°C	0.5°C/s max.
Solder Reflow	P3, R3 P4, R4	170°C to 230°C (235°C max.) 230°C to 170°C	4.0°C/s typ. –4.0°C/s typ.
Cool Down	P4, R5	170°C to 25°C	–3°C/s max.

Table 1. Reflow Process Zones.

representative for additional details.

Figure 5 is a straight line representation of a nominal temperature profile for a convective IR reflow solder process. The temperature profile is divided into four process zones with four ΔT/Δtime temperature change rates. The ΔT/Δtime temperature change rates are detailed in Table 1. The temperatures are measured at the component to printed-circuit (pc) board connections.

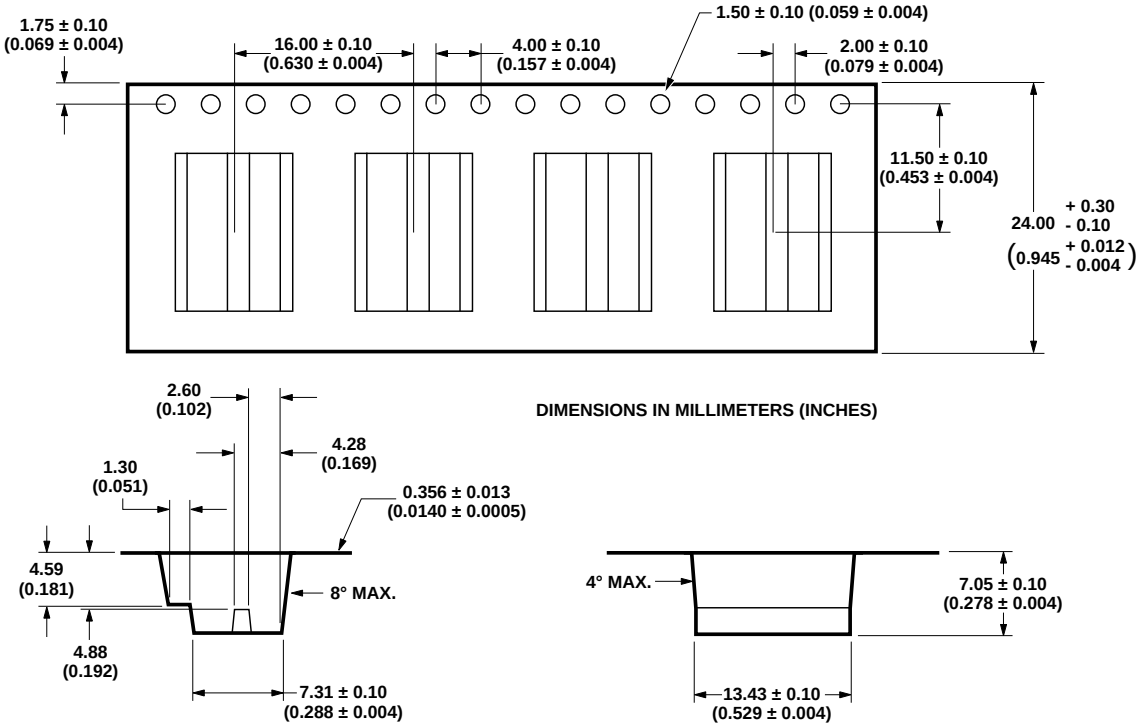
In **process zone P1**, the pc board and HSDL-2300 castellation I/O pins are heated to a temperature of 125°C to activate the flux in the solder paste. The temperature ramp up rate, R1, is limited to 3°C per second to allow for even heating of both the pc board and HSDL-2300 castellation I/O pins.

Process zone P2 should be of sufficient time duration to dry the solder paste. The temperature is raised to a level just below the liquidus point of the solder, usually 170°C (338°F).

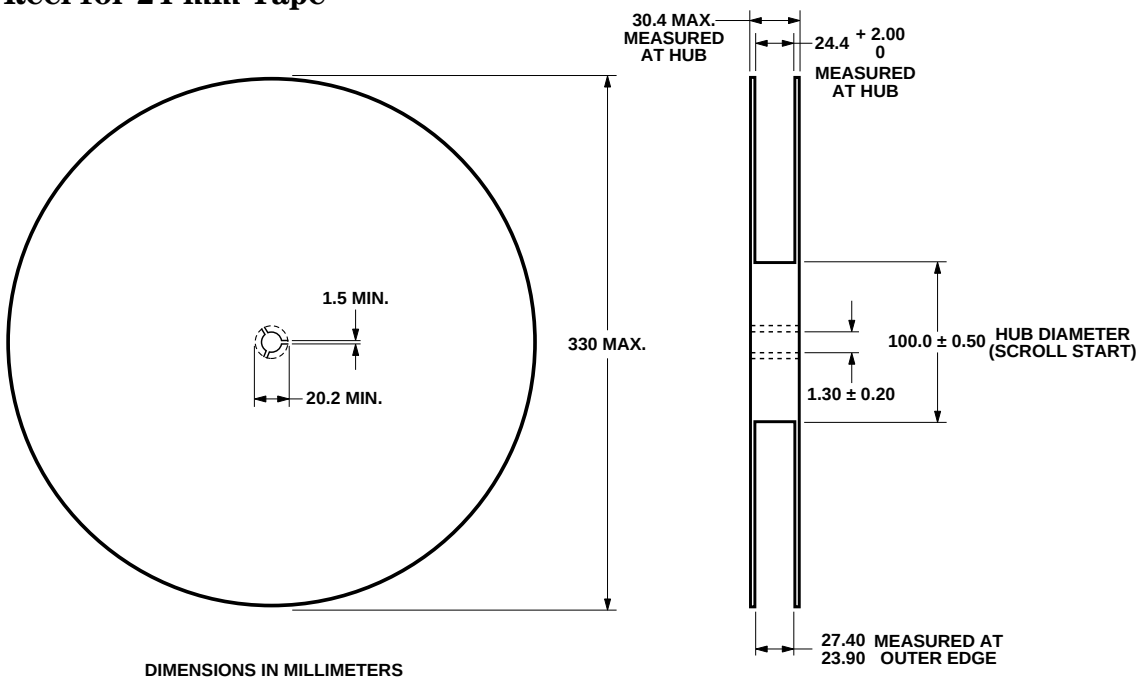
Process zone P3 is the solder reflow zone. In zone P3, the temperature is quickly raised above the liquidus point of solder to 230°C (446°F) for optimum results. The dwell time above the liquidus point of solder should be between 15 and 90 seconds. It usually takes about 15 seconds to assure proper coalescing of the solder balls into liquid solder and the formation of good solder connections. Beyond a dwell time of 90 seconds, the intermetallic growth within the solder connections becomes excessive, resulting in the formation of weak and unreliable connections. The temperature is then rapidly reduced to a point below the solidus temperature of the solder, usually 170°C (338°F), to allow the solder within the connections to freeze solid.

Process zone P4 is the cool down after solder freeze. The cool down rate, R5, from the liquidus point of the solder to 25°C (77°F) should not exceed –3°C (26.6°F) per second maximum. This limitation is necessary to allow the pc board

Tape and Reel Dimensions



Reel for 24 mm Tape



and HSDL-2300 castellation I/O pins to change dimensions evenly, putting minimal stresses on the HSDL-2300 transceiver.

Appendix A. Test Methods

A.1 Background Light and Electromagnetic Field

There are four ambient interference conditions in which the receiver is to operate correctly. The conditions are to be applied separately:

1. Electromagnetic field: 3 V/m maximum (please refer to IEC 801-3, severity level 3 for details).

2. Sunlight: 10 kilolux maximum at the optical port. This is simulated with an IR source having a peak wavelength within the range 850 nm to 900 nm and a spectral width less than 50 nm biased to provide 490 μW/cm^2 (with no modulation) at the optical port. The light source faces the optical port.

   This simulates sunlight within the IrDA spectral range. The effect of longer wavelength radiation is covered by the incandescent condition.

3. Incandescent Lighting: 1000 lux maximum. This is produced with general service, tungsten-filament, gas-filled, inside-frosted lamps in the 60 Watt to 150 Watt range to generate 1000 lux over the horizontal surface on which the equipment under test rests. The light sources are above the test area. The source is expected to have a filament temperature in the 2700 to 3050 degrees Kelvin range and a spectral peak in the 850 nm to 1050 nm range.

4. Fluorescent Lighting: 1000 lux maximum. This is simulated with an IR source having a peak wavelength within the range 850 nm to 900 nm and a spectral width of less than 50 nm biased and modulated to provide an optical square wave signal (0 μW/cm^2 minimum and 0.3 μW/cm^2 peak amplitude with 10% to 90% rise and fall times less than or equal to 100 ns) over the horizontal surface on which the equipment under test rests. The light sources are above the test area. The frequency of the optical signal is swept over the frequency range from 20 kHz to 200 kHz.

   Due to the variety of fluorescent lamps and the range of IR emissions, this condition is not expected to cover all circumstances. It will provide a common floor for IrDA operation.

All IR transceivers operating under the recommended drive conditions are classified as CENELEC EN60825-1 Accessible Emission Limit (AEL) Class 1. This standard is in effect in Europe as of January 1, 1997. AEL Class 1 LED devices are considered eye safe. Please see Application Note 1094 for more information.

Appendix B. SMT Assembly Methods

1.0 Solder Pad, Mask and Metal Stencil

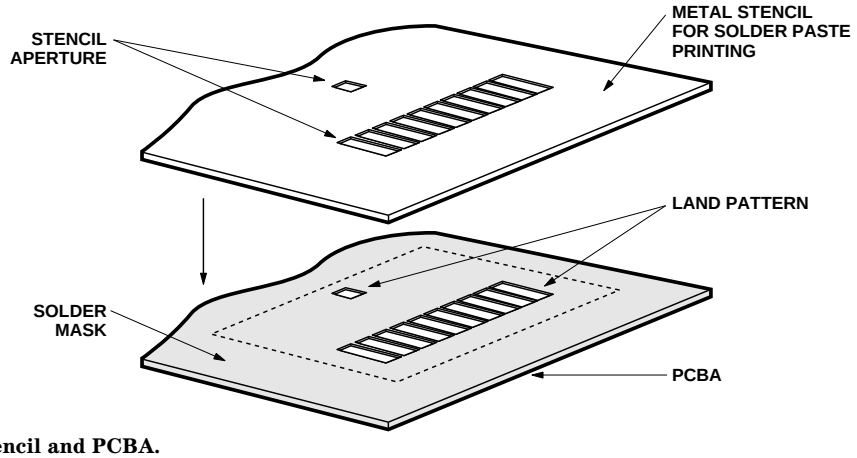
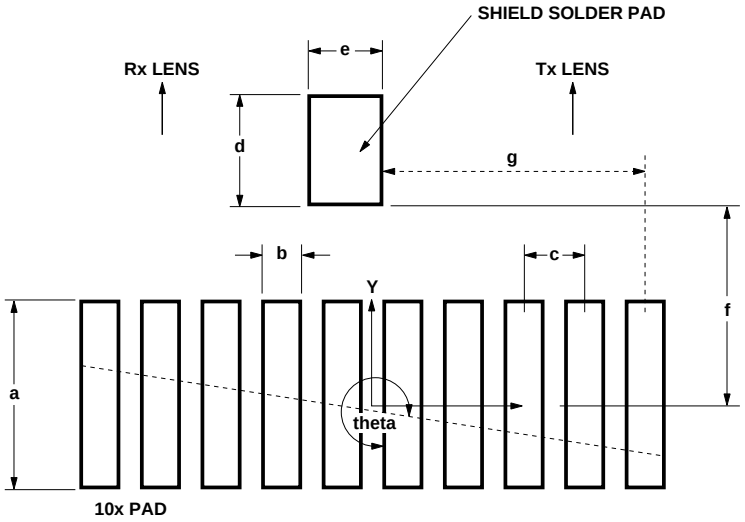


Figure 1.0. Stencil and PCBA.

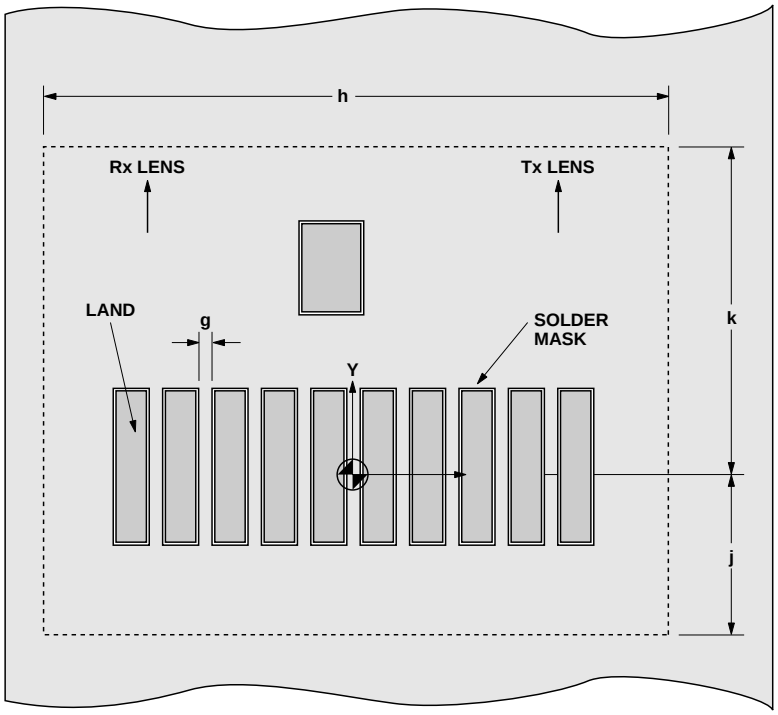
1.1 Recommended Land Pattern for HSDL-2300



DIM.	mm	INCHES
a	2.60	0.102
b	0.70	0.027
c (PITCH)	1.14	0.045
d	2.40	0.094
e	1.25	0.049
f	4.22	0.166
g	5.05	0.198

Figure 2.0. Top View of Land Pattern.

1.2 Adjacent Land Keep-out and Solder Mask Areas



DIM.	mm	INCHES
g	MIN. 0.15	MIN. 0.006
h	13.40	0.528
k	7.20	0.283
j	2.10	0.083

• ADJACENT LAND KEEP-OUT IS THE MAXIMUM SPACE OCCUPIED BY THE UNIT RELATIVE TO THE LAND PATTERN. THERE SHOULD BE NO OTHER SMD COMPONENTS WITHIN THIS AREA.

• "g" IS THE MINIMUM SOLDER RESIST STRIP WIDTH REQUIRED TO AVOID SOLDER BRIDGING ADJACENT PADS.

NOTE: WET/LIQUID PHOTO-IMAGEABLE SOLDER RESIST/MASK IS RECOMMENDED.

Figure 3.0. PCBA – Adjacent Land Keep-out and Solder Mask.

2.0 Recommended Solder Paste/Cream Volume for Castellation Joints.
The printed solder paste volume required per castellation pad is 0.36 cubic mm ± 15% (based on either no-clean or aqueous solder cream types with typically 60 to 65% solid content by volume).

See Figure 4.0			
t, nominal stencil thickness		**l, length of aperture**	
mm	**inches**	**mm**	**inches**
0.127	0.005	3.8 ± 0.1	0.150 ± 0.004
0.152	0.006	3.4 ± 0.1	0.134 ± 0.004
0.203	0.008	2.7 ± 0.1	0.106 ± 0.004
w, the width of aperture is fixed at 0.7 mm (0.028 inches)			

2.1 Recommended Metal Solder Stencil Aperture
To ensure adequate printed solder paste volume, the following combination of metal stencil aperture and metal stencil thickness should be used:

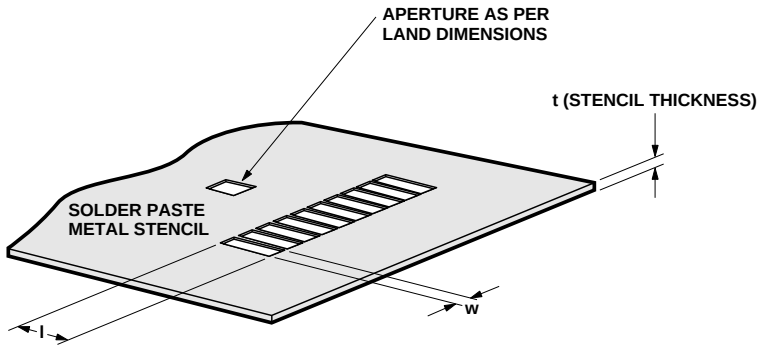


Figure 4.0. Solder Paste Stencil Aperture.

3.0 Pick and Place Misalignment Tolerance and Product Self-Alignment after Solder Reflow
If the printed solder paste volume is adequate, **the HSDL-2300 will self-align** after solder reflow. Units should be properly reflowed in IR-Hot Air convection over using the recommended reflow profile. The direction of board travel does not matter.

3.1 Tolerance for X-Axis Alignment of Castellation
Misalignment of castellation to the land pad should not exceed 0.2 mm or approximately half the width of the castellation during placement of the unit. The castellations will completely self-align to the pads during solder reflow.

Allowable Misalignment Tolerance

x-direction	≤ 0.2 mm (0.008 inches)
theta-direction	± 3°

3.2 Tolerance for Rotational (theta) Misalignment
Unit when mounted should not be rotated more than 3° with reference to center X-Y as specified in Figure 2.0.

Unit with theta misalignment of more than 3° does not completely self-align after reflow. Unit with 3° rotational of theta misalignment self-align completely after solder reflow.

3.3 Y-Axis Misalignment of Castellation

In the y direction, the unit does not self-align after solder reflow. This should not be an issue as the length of the pad (2.6 mm) is sufficient for a misplacement accuracy of +/– 0.2 mm from center of Y-axis as shown in Figure 5.0. There is still more than sufficient space for a proper strong solder fillet to be fully formed on both sides of the castellation joints.

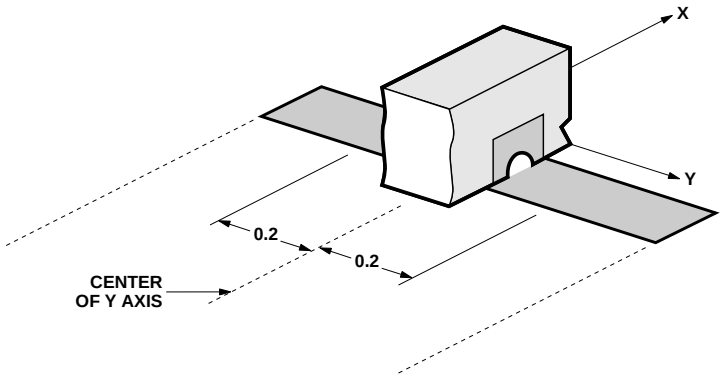


Figure 5.0. Section of a Castellation in Y-Axis.

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Obsoletes 5968-2121E (11/99)
5988-2312EN