Le7922

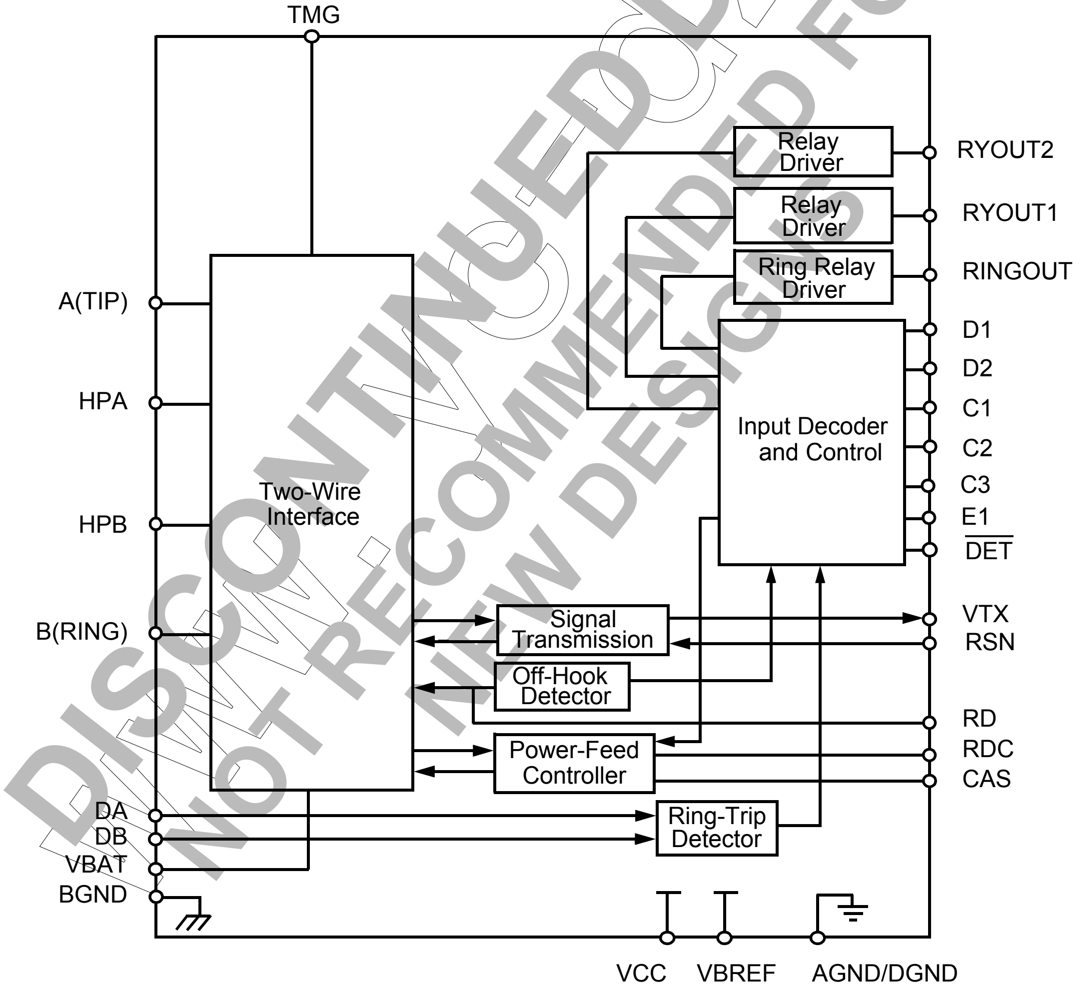
Subscriber Line Interface Circuit

The Le7922 Subscriber Line Interface Circuit implements the basic telephone line interface functions, and enables the design of low cost, high performance, POTS line interface cards.

DISTINCTIVE CHARACTERISTICS

- **Control states: Active, Reverse Polarity, Tip Open, Ringing, Standby, and Open Circuit**
- **Low standby power (35 mW)**
- **–19 V to –58 V battery operation**
- **On-hook transmission**
- **Two-wire impedance set by single external impedance**
- **Available in PLCC and SOIC**
- **Programmable constant-current feed**
- **Programmable loop-detect threshold**
- **Ground-key detector**
- **Programmable ring-trip detect threshold**
- **No –5 V supply required**
- **Current Gain = 500**
- **On-chip Thermal Management (TMG) feature**
- **Three on-chip relay drivers and relay snubbers, 1 ringing and 2 general purpose**
- **Tip Open state for ground-start lines**

BLOCK DIAGRAM



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ORDERING INFORMATION

Standard Products

Legerity standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below

Le7922* **–1** **J** **C**

TEMPERATURE RANGE
C = Commercial (0°C to +70°C)*

PACKAGE TYPE
J = 32-pin Plastic Leaded Chip Carrier (PL 032)
S = 28-pin Small Outline Integrated Circuit (SOW 028)

PERFORMANCE GRADE
–1 52 dB Longitudinal Balance, Polarity Reversal
–2 63 dB Longitudinal Balance, Polarity Reversal
–3 52 dB Longitudinal Balance, No Polarity Reversal
–4 63 dB Longitudinal Balance, No Polarity Reversal

DEVICE NUMBER/DESCRIPTION
Le7922
Subscriber Line Interface Circuit

Valid Combinations		
Le7922*	–1 –2 –3 –4	JC SC

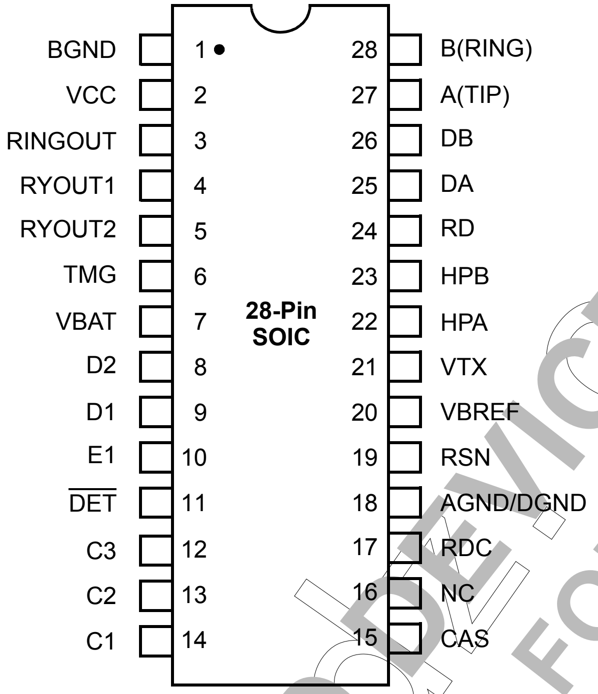
Valid Combinations

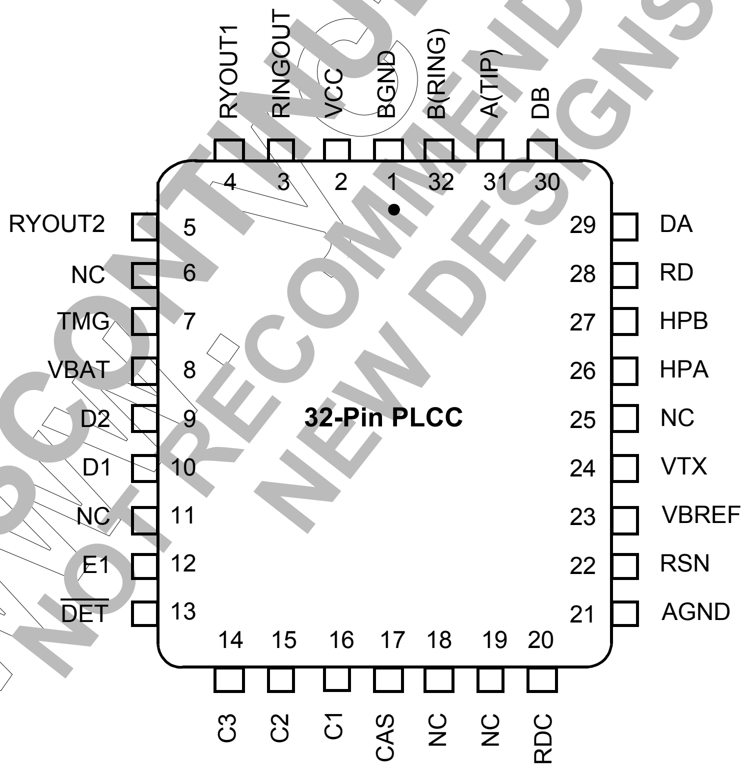
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local Legerity sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on Legerity's standard military grade products.

**Legerity reserves the right to fulfill all orders for this device with parts marked with the "Am" part number prefix, until such time as all inventory bearing this mark has been depleted. It should be noted that parts marked with either the "Am" or the "Le" part number prefix are equivalent devices in terms of form, fit, and function. The only difference between the two is in the part number prefix appearing on the topside mark.*

CONNECTION DIAGRAMS

Top View





Notes:

1. Pin 1 is marked for orientation.

2. NC = No Connect

PIN DESCRIPTIONS

Pin Name	Type	Description
AGND/DGND	Gnd	Analog and digital ground.
A(TIP)	Output	Output of A(TIP) power amplifier.
BGND	Gnd	Battery (power) ground.
B(RING)	Output	Output of B(RING) power amplifier.
C3–C1	Input	Decoder. SLIC control pins. C3 is MSB and C1 is LSB.
CAS	Capacitor	Anti-saturation capacitor. Pin for capacitor to filter reference voltage when operating in anti-saturation region.
D2–D1	Input	Relay driver control. D1 and D2 control the relay drivers RYOUT1 and RYOUT2. Logic Low on D1 activates the RYOUT1 relay driver. Logic Low on D2 activates the RYOUT2 relay driver.
DA	Input	Ring-trip negative. Negative input to ring-trip comparator.
DB	Input	Ring-trip positive. Positive input to ring-trip comparator.
DET	Output	Switchhook detector. A logic Low indicates that selected condition is detected. The detect condition is selected by the logic inputs (C3–C1). The output is open-collector with a built-in 15 kΩ pull-up resistor.
E1	Input	E1 = 1 selects the switchhook detector. E1 = 0 selects the ground-key detector. ***Note**: In the Tip Open state, the ground-key detector is active irrespective of E1.*
HPA	Capacitor	High-pass filter capacitor. A(TIP) side of high-pass filter capacitor.
HPB	Capacitor	High-pass filter capacitor. B(RING) side of high-pass filter capacitor.
NC	—	No connect. This pin is not internally connected.
RD	Resistor	Detect resistor. Detector threshold set and filter pin.
RDC	Resistor	DC feed resistor. Connection point for the DC feed current programming network. The other end of the network connects to the receiver summing node (RSN).
RINGOUT	Output	Ring relay driver. Open-collector driver with emitter internally connected to BGND.
RSN	Input	Receive summing node. The metallic current (both AC and DC) between A(TIP) and B(RING) is equal to 500 times the current into this pin. The networks which program receive gain, two-wire impedance, and feed resistance all connect to this node.
RYOUT1	Output	Relay/switch driver. Open-collector driver with emitter internally connected to BGND.
RYOUT2	Output	Relay/switch driver. Open-collector driver with emitter internally connected to BGND.
TMG	Thermal	Thermal management. External resistor connects between this pin and VBAT to offload power from SLIC.
VBAT	Battery	Battery supply and connection to substrate.
VBREF	—	This is a Legerity reserved pin and must always be connected to the VBAT pin.
VCC	Power	+5 V power supply.
VTX	Output	Transmit audio. This output is a 0.50 gain version of the A(TIP) and B(RING) metallic voltage. VTX also sources the two-wire input impedance programming network.

ABSOLUTE MAXIMUM RATINGS

Storage temperature	–55°C to +150°C
V_{CC} with respect to AGND/DGND	–0.4 V to +7.0 V
V_{BAT} with respect to AGND/DGND:	
Continuous	+0.4 V to –70 V
10 ms	+0.4 V to –75 V
BGND with respect to AGND/DGND	+3 V to –3 V
A(TIP) or B(RING) to BGND:	
Continuous	V_{BAT} to +1 V
10 ms (f = 0.1 Hz)	–70 V to +5 V
1 µs (f = 0.1 Hz)	–80 V to +8 V
250 ns (f = 0.1 Hz)	–90 V to +12 V
Current from A(TIP) or B(RING)	±150 mA
RINGOUT/RYOUT1,2 current	50 mA
RINGOUT/RYOUT1,2 voltage	BGND to +7 V
RINGOUT/RYOUT1,2 transient	BGND to +10 V
DA and DB inputs	
Voltage on ring-trip inputs	V_{BAT} to 0 V
Current into ring-trip inputs	±10 mA
C3–C1, D2–D1, and E1	
Input voltage	–0.4 V to V_{CC} + 0.4 V
Maximum power dissipation, continuous, T_A = 70°C, No heat sink (See note)	
In 32-pin PLCC package	1.7 W
In 28-pin SOIC package	1.4 W
Thermal Data:	θ_{JA}
In 32-pin PLCC package	43°C/W typ
In 28-pin SOIC package	60°C/W typ
ESD immunity/pin (HBM)	1500 V

***Note:** Thermal limiting circuitry on chip will shut down the circuit at a junction temperature of about 165°C. Continuous operation above 145°C junction temperature may degrade device reliability.*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient temperature	0°C to +70°C*
V_{CC}	4.75 V to 5.25 V
V_{BAT}	–19 V to –58 V
AGND/DGND	0 V
BGND with respect to AGND/DGND	–100 mV to +100 mV
Load resistance on VTX to ground	20 kΩ min

The operating ranges define those limits between which the functionality of the device is guaranteed.

** Legerity guarantees the performance of this device over commercial (0 to 70°C) and industrial (-40 to 85 °C) temperature ranges by conducting electrical characterization over each range and by conducting a production test with single insertion coupled to periodic sampling. These characterization and test procedures comply with section 4.6.2 of Bellcore TR-TSY-000357 Component Reliability Assurance Requirements for Telecommunications Equipment.*

ELECTRICAL CHARACTERISTICS

Description	Test Conditions (see Note 1)	Min	Typ	Max	Unit	Note
Transmission Performance						
2-wire return loss	200 Hz to 3.4 kHz	26			dB	1, 4
Analog output (VTX) impedance			3	20	Ω	4
Analog (VTX) output offset voltage		–50		+50	mV	
Overload level, 2-wire	Active state	2.5			Vpk	2a
Overload level	On hook, R_{LAC} = 600 Ω	0.77			Vrms	2b
THD, Total Harmonic Distortion	0 dBm +7 dBm		–64 –55	–50 –40	dB	5
THD, On hook	0 dBm, R_{LAC} = 600 Ω			–36		
Longitudinal Capability (See Test Circuit D)						
Longitudinal to metallic L-T, L-4 200 Hz to 1 kHz	Normal Polarity				dB	
	0°C to +70°C -2,-4	63				
	-40°C to +85°C -2,-4	58				4
	0°C to +70°C -1,-3	52				
	-40°C to +85°C -1,-3	50				4
	Reverse Polarity					
	-40°C to +85°C -2	54				4
	0°C to +70°C -1	52				
	-40°C to +85°C -1	50				4
Longitudinal to metallic L-T, L-4 1 kHz to 3.4 kHz	Normal Polarity					
	0°C to +70°C -2,-4	58				
	-40°C to +85°C -2,-4	53				4
	0°C to +70°C -1,-3	52				
	-40°C to +85°C -1,-3	50				4
	Reverse Polarity					
	-40°C to +85°C -2	53				4
	0°C to +70°C -1	52				
	-40°C to +85°C -1	50				4
Longitudinal signal generation 4-L	200 Hz to 3.4 kHz	40				
Longitudinal current per pin (A or B)	Active state	17	27		mArms	8
Longitudinal impedance at A or B	0 to 100 Hz		25		Ω/pin	4
Idle Channel Noise						
C-message weighted noise	R_L = 600 Ω 0°C to +70°C R_L = 600 Ω –40°C to +85°C		7	+10 +12	dBrnc	4
Psophometric weighted noise	R_L = 600 Ω 0°C to +70°C R_L = 600 Ω –40°C to +85°C		–83	–80 –78	dBmp	
Insertion Loss and Balance Return Signal (See Test Circuits A and B)						
Gain accuracy 4- to 2-wire	0 dBm, 1 kHz	–0.20	0	+0.20	dB	
Gain accuracy 2- to 4-wire, 4- to 4-wire	0 dBm, 1 kHz	–6.22	–6.02	–5.82		
Gain accuracy, 4- to 2-wire	On hook	–0.35		+0.35		4
Gain accuracy, 2- to 4-wire, 4- to 4-wire	On hook	–6.37	–6.02	–5.67		
Gain accuracy over frequency	300 to 3.4 kHz relative to 1 kHz	–0.15		+0.15		
Gain tracking	+3 dBm to –55 dBm relative to 0 dBm	–0.15		+0.15		
Gain tracking On hook	0 dBm to –37 dBm +3 dBm to 0 dBm	–0.15 –0.35		+0.15 +0.35		
Group delay	0 dBm, 1 kHz		4		μs	4, 7

ELECTRICAL CHARACTERISTICS (continued)

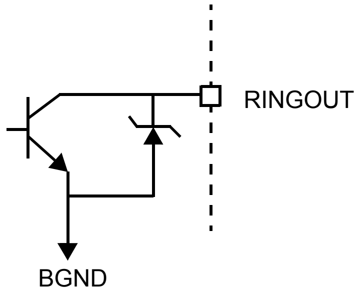
Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Line Characteristics						
I_L, Short Loops, Active state	R_{LDC} = 600 Ω	26.4	30	33.6	mA	
I_L, Long Loops, Active state	R_{LDC} = 1930 Ω, BAT = –42.75 V, T_A = 25°C	18	19			
I_L, Accuracy, Standby state	$I_L = \frac{\lvert BAT\rvert - 3\ V}{R_L + 400}$ $T_A = 25°C$	0.7I_L	I_L	1.3I_L		
	Constant-current region	18	30			
I_L, Loop current, Disconnect state	R_L = 0			100	µA	
I_LLIM	Active, A and B to ground		75	120	mA	
VAB, Open Circuit voltage		38.3	40.3		V	
I_A, Leakage, Tip Open state	R_L = 0			100	µA	
I_B, Current, Tip Open state	B to GND	15	30	56	mA	
V_A, Active	RA to BAT = 7 kΩ, RB to GND = 100 Ω	–7.5	–5		V	4
Power Supply Rejection Ratio						
V_{CC}	50 Hz to 3.4 kHz (V_{RIPPLE} = 100 mVrms)	30	40		dB	5
V_{BAT}	50 Hz to 3.4 kHz (V_{RIPPLE} = 500 mVpp)	28	50			
Effective internal resistance	CAS pin to V_{BAT}	85	170	255	kΩ	4
Power Dissipation						
On hook, Disconnect state			25	70	mW	
On hook, Standby state			35	100		
On hook, Active state			130	210		
Off hook, Standby state	R_L = 600 Ω		860	1200		
Off hook, Active state	R_L = 300 Ω		700	1000		
Supply Currents						
I_{CC}, On-hook V_{CC} supply current	Disconnect state Standby state Active state		1.7 2.2 5.0	4.0 4.0 7.0	mA	
I_{BAT}, On-hook V_{BAT} supply current	Disconnect state Standby state Active state		0.25 0.55 2.2	1.0 1.5 4.0		
RFI Rejection						
RFI rejection	100 kHz to 30 MHz, (See Figure F)			1.0	mVrms	4
Receive Summing Node (RSN)						
RSN DC voltage	I_{RSN} = 0 mA		0		V	4
RSN impedance	200 Hz to 3.4 kHz		10	20	Ω	
Logic Inputs (C3–C1, D2–D1, and E1)						
V_{IH}, Input High voltage (except C3)		2.0			V	
V_{IH}, C3		2.5				
V_{IL}, Input Low voltage				0.8		
I_{IH}, Input High current		–75		40	µA	
I_{IL}, Input Low current		–400				
Logic Output ($\overline{DET}$)						
V_{OL}, Output Low voltage	I_{OUT} = 0.3 mA, 15 kΩ to V_{CC}			0.40	V	
V_{OH}, Output High voltage	I_{OUT} = –0.1 mA, 15 kΩ to V_{CC}	2.4				

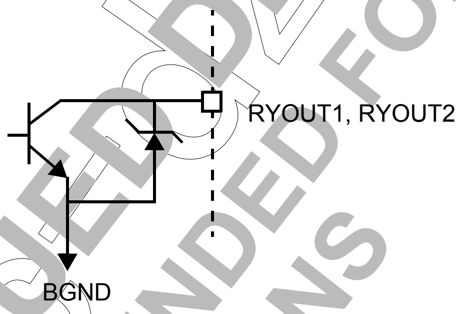
ELECTRICAL CHARACTERISTICS (continued)

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Ring-Trip Detector Input (DA, DB)						
Bias current		–500	–50		nA	
Offset voltage	Source resistance = 2 MΩ	–50	0	+50	mV	6
Loop Detector						
On threshold	R_D = 35.4 kΩ	9.4	11.7	14.0	mA	
Off threshold	R_D = 35.4 kΩ	8.8	10.4	12.0		
Hysteresis	R_D = 35.4 kΩ		1.3			
IGK, Ground-key detector threshold	R_L from BX to GND Active, Standby, and Tip open	5	9	13	mA	
Relay Driver Output (RINGOUT, RYOUT1, RYOUT2)						
On voltage	I_{OL} = 40 mA		+0.3	+0.7	V	
Off leakage	V_{OH} = +5 V			100	µA	
Zener breakover	I_Z = 100 µA	6	7.2		V	
Zener On voltage	I_Z = 30 mA		10			

Note:
** Performance Grade*

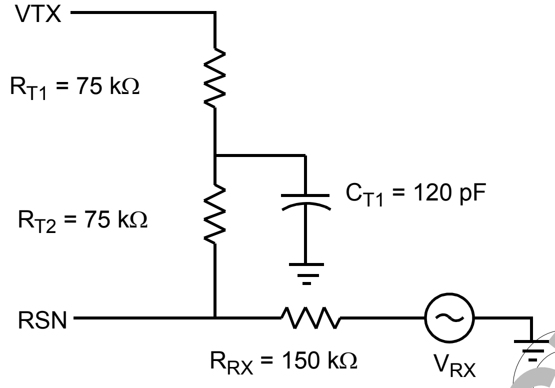
RELAY DRIVER SCHEMATICS





Notes:

1. *Unless otherwise noted, test conditions are BAT = –48 V, V_{CC} = +5 V, R_L = 600 Ω, R_{DC1} = R_{DC2} = 10.4K, R_{TMG} = 1600 Ω, R_D = 35.4 kΩ, no fuse resistors, C_{HP} = 0.22 μF, C_{DC} = 0.33 μF, C_{CAS} = 0.33 μF, D1 = 1N400x, two-wire AC input impedance is a 600 Ω resistance synthesized by the programming network shown below.*



2. *a. Overload level is defined when THD = 1%.*
   b. Overload level is defined when THD = 1.5%.
3. *Balance return signal is the signal generated at V_{TX} by V_{RX}. This specification assumes that the two-wire, AC-load impedance matches the programmed impedance.*
4. *Not tested in production. This parameter is guaranteed by characterization or correlation to other tests.*
5. *This parameter is tested at 1 kHz in production. Performance at other frequencies is guaranteed by characterization.*
6. *Tested with 0 Ω source impedance. 2 MΩ is specified for system design only.*
7. *Group delay can be greatly reduced by using a Z_T network such as that shown in Note 1. The network reduces the group delay to less than 2 μs and increases 2WRL. The effect of group delay on linecard performance also may be compensated for by synthesizing complex impedance with the QSLAC™ or DSLAC™ device.*
8. *Minimum current level guaranteed not to cause a false loop detect.*

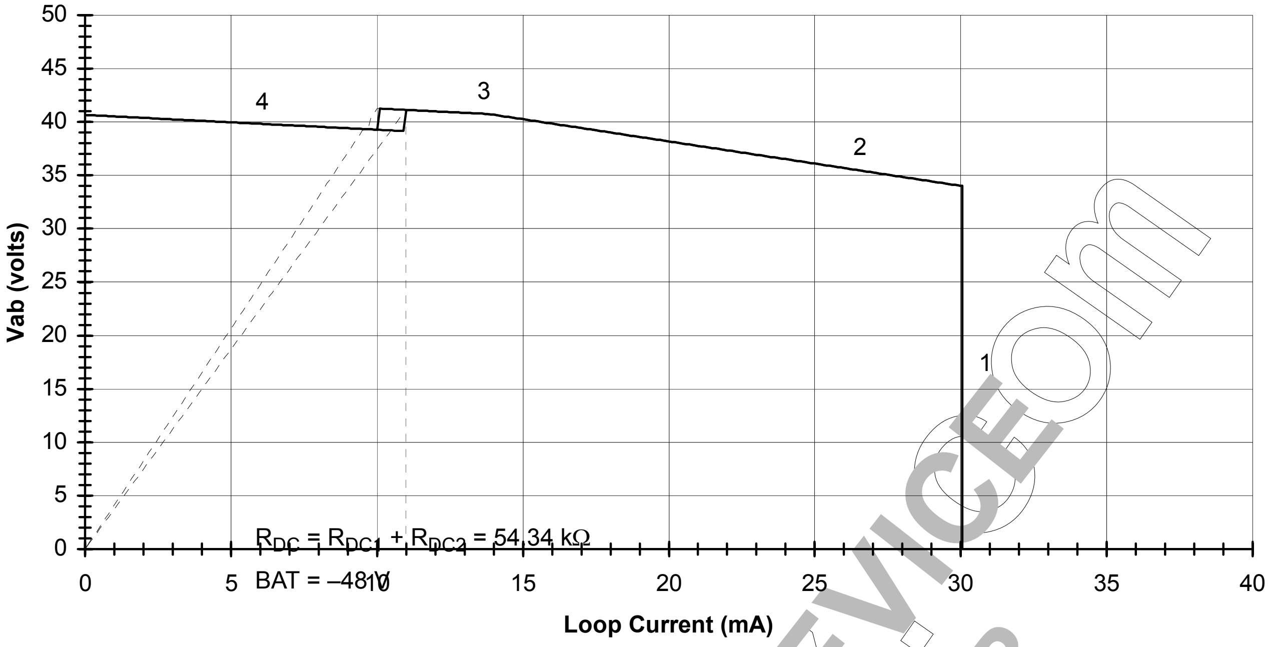
Table 1. SLIC Decoding

					E1 = 1	E1 = 0
State	**C3**	**C2**	**C1**	**Two-Wire Status**	**$\overline{\text{DET}}$ Output**	**$\overline{\text{DET}}$ Output**
0	0	0	0	Reserved	X	X
1	0	0	1	Reserved	X	X
2	0	1	0	Active Polarity Reversal	Loop detector	Ground Key
3	0	1	1	Tip Open	Ground Key	Ground Key
4	1	0	0	Open Circuit	Ring trip	Ring Trip
5	1	0	1	Ringing	Ring trip	Ring Trip
6	1	1	0	Active	Loop detector	Ground Key
7	1	1	1	Standby	Loop detector	Ground Key

Table 2. User-Programmable Components

$Z_T = 250(Z_{2WIN} - 2R_F)$	Z_T is connected between the VTX and RSN pins. The fuse resistors are R_F, and Z_{2WIN} is the desired 2-wire AC input impedance. When computing Z_T, the internal current amplifier pole and any external stray capacitance between VTX and RSN must be taken into account.
$Z_{RX} = \frac{Z_L}{G_{42L}} \bullet \frac{500Z_T}{Z_T + 250(Z_L + 2R_F)}$	Z_{RX} is connected from VRX to RSN. Z_T is defined above, and G_{42L} is the desired receive gain.
$R_{DC1} + R_{DC2} = \frac{625}{I_{LOOP}}$ $C_{DC} = 1.5\ \text{ms} \bullet \frac{R_{DC1} + R_{DC2}}{R_{DC1} \bullet R_{DC2}}$	R_{DC1}, R_{DC2}, and C_{DC} form the network connected to the R_{DC} pin. R_{DC1} and R_{DC2} are approximately equal. I_{LOOP} is the desired loop current in the constant-current region.
$RD_{ON} = \frac{390}{I_T}$, $RD_{OFF} = \frac{355}{I_T}$, $C_D = \frac{0.5\ \text{ms}}{R_D}$	R_D and C_D form the network connected from R_D to AGND/DGND and I_T is the threshold current between on hook and off hook.
$C_{CAS} = \frac{1}{3.4 \bullet 10^5 \pi f_c}$	C_{CAS} is the regulator filter capacitor and f_c is the desired filter cut-off frequency.
$I_{STANDBY} = \frac{\lvert V_{BAT}\rvert - 3\ \text{V}}{400\ \Omega + R_L}$	Standby loop current (resistive region).
Thermal Management Equations (Normal Active and Tip Open States)	
$R_{TMG} \ge \left(\frac{\lvert V_{BAT}\rvert - 6\ \text{V}}{I_{LOOP}} - 70\ \Omega\right)$	R_{TMG} is connected from TMG to VBAT and saves power within the SLIC in Active and Polarity Reversal states only.
$P_{RTMG} = \frac{(\lvert V_{BAT}\rvert - 6\ \text{V} - (I_L \bullet R_L))^2}{(R_{TMG} + 70\ \Omega)^2} \bullet R_{TMG}$	Power dissipated in the TMG resistor, R_{TMG}, during Active and Polarity Reversal states.
$P_{SLIC} = \lvert V_{BAT}\rvert \bullet I_L - P_{RTMG} - R_L(I_L)^2 + 0.13\ \text{W}$	Power dissipated in the SLIC while in Active and Polarity Reversal states.

DC FEED CHARACTERISTICS



$R_{DC} = R_{DC1} + R_{DC2} = 10.4K$

BAT = 48 V

Notes:

1. *Constant current region:* $V_{AB} = I_L R_L' = \frac{625}{R_{DC}} R_L'$, where $R_L' = R_L + 2R_F$

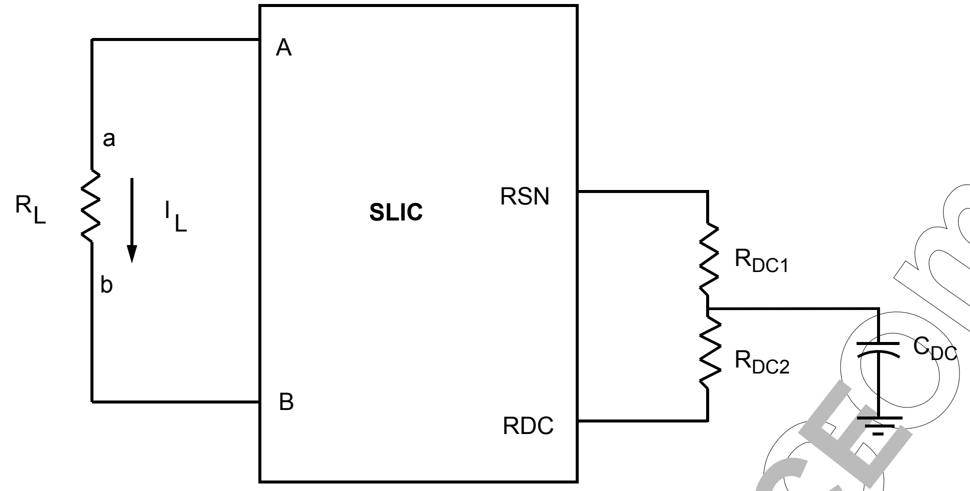
2. *Battery-independent anti-sat:* $V_{AB} = 47\ V - I_L \frac{R_{DC}}{50}$

3. *Battery tracking anti-sat (off hook):*
   a) $V_{AB} \geq 34.5\ V$ $\quad V_{AB} = 0.67|V_{BAT}| + 10.5 - I_L \frac{R_{DC}}{150}$
   b) $V_{AB} < 34.5\ V$ $\quad V_{AB} = |V_{BAT}| - 1.7 - I_L \frac{R_{DC}}{200}$

4. *Battery tracking anti-sat (on hook):*
   a) $V_{AB} \geq 34.5\ V$ $\quad V_{AB} = 0.67|V_{BAT}| + 8.5 - I_L \frac{R_{DC}}{150}$
   b) $V_{AB} < 34.5\ V$ $\quad V_{AB} = |V_{BAT}| - 4.4 - I_L \frac{R_{DC}}{200}$

a. Load Line (Typical)

DC FEED CHARACTERISTICS (continued)

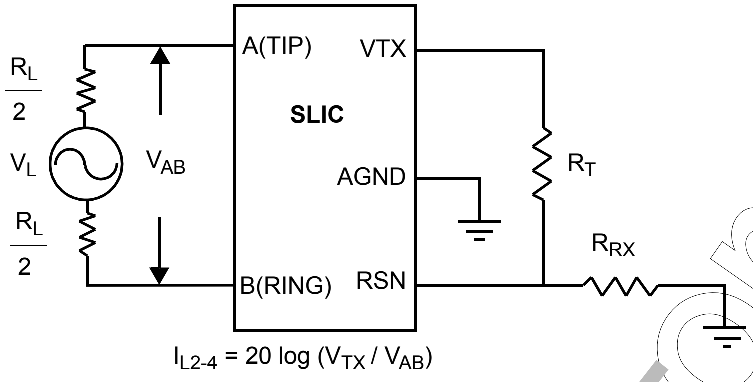


Feed current programmed by R_{DC1} and R_{DC2}

b. Feed Programming

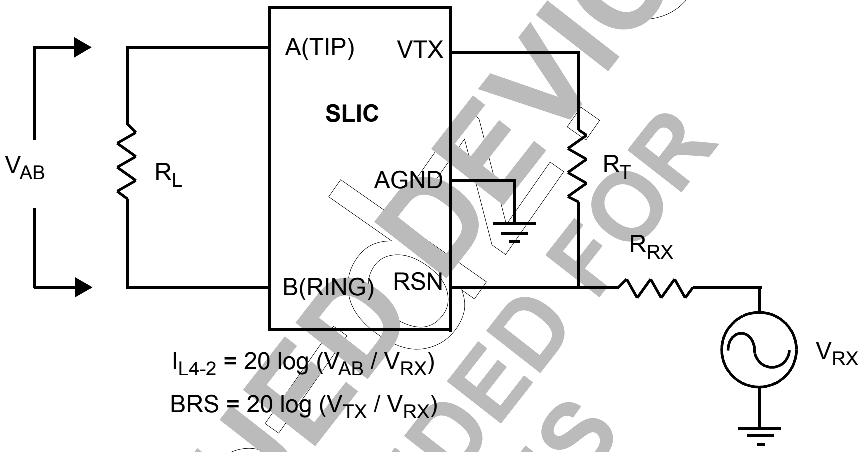
Figure 1. DC Feed Characteristics

TEST CIRCUITS



$I_{L2-4} = 20 \log (V_{TX} / V_{AB})$

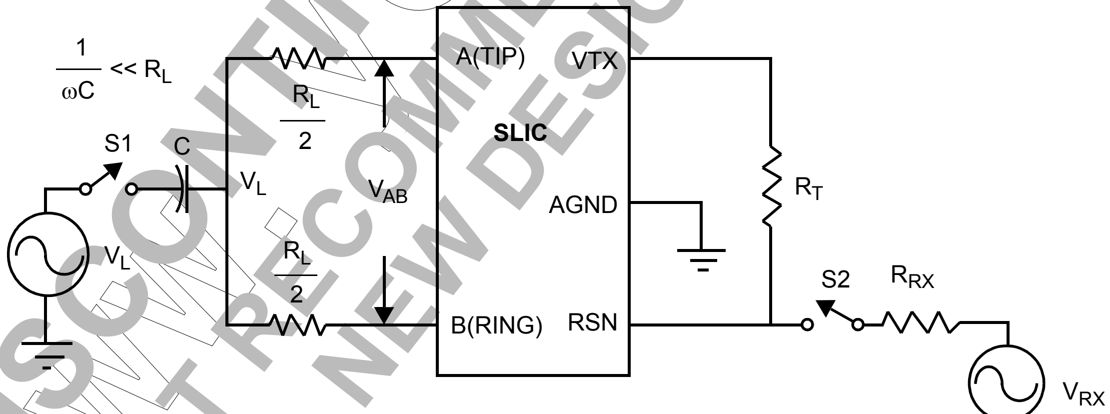
A. Two- to Four-Wire Insertion Loss



$I_{L4-2} = 20 \log (V_{AB} / V_{RX})$

$BRS = 20 \log (V_{TX} / V_{RX})$

B. Four- to Two-Wire Insertion Loss and Balance Return Signal

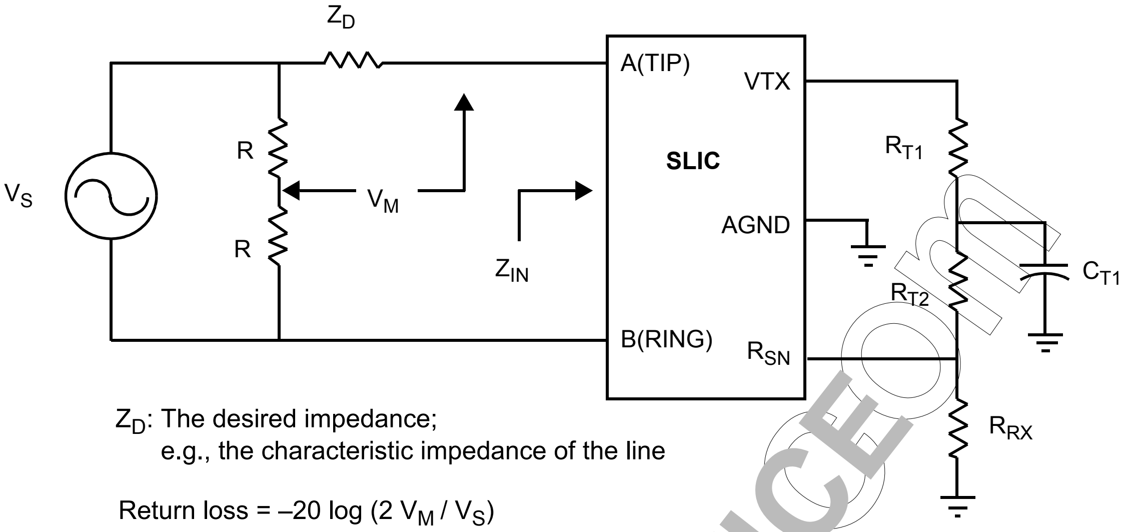


S2 Open, S1 Closed
L-T Long. Bal. = $20 \log (V_{AB} / V_L)$
L-4 Long. Bal. = $20 \log (V_{TX} / V_L)$

S2 Closed, S1 Open
4-L Long. Sig. Gen. = $20 \log (V_L / V_{RX})$

C. Longitudinal Balance

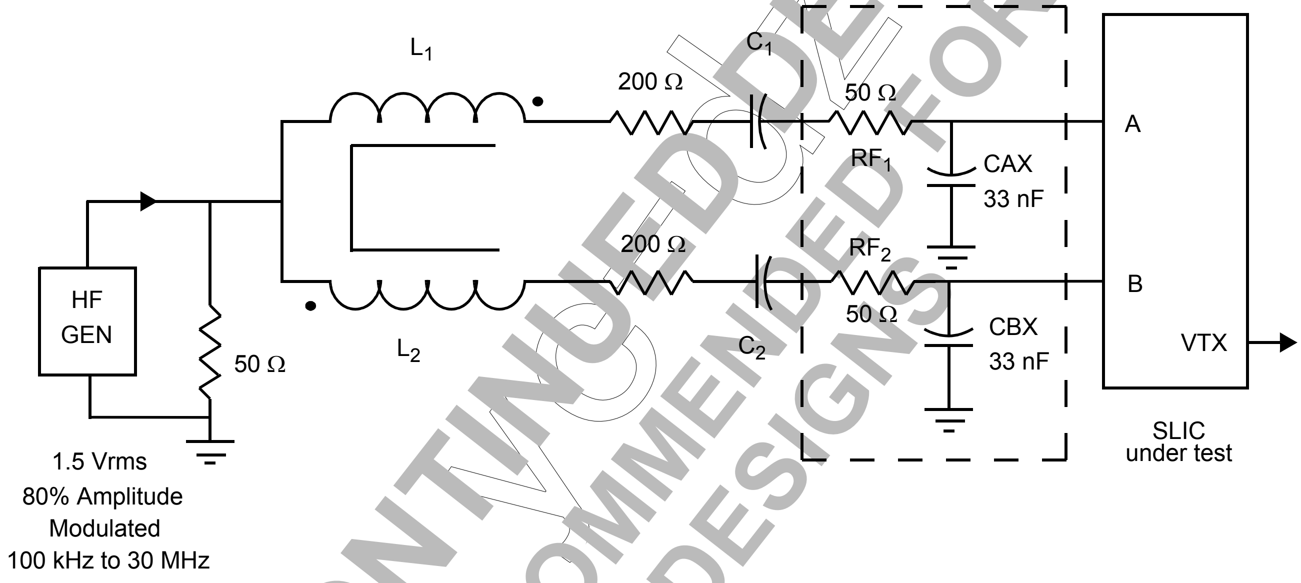
TEST CIRCUITS (continued)



Z_D: The desired impedance;
e.g., the characteristic impedance of the line

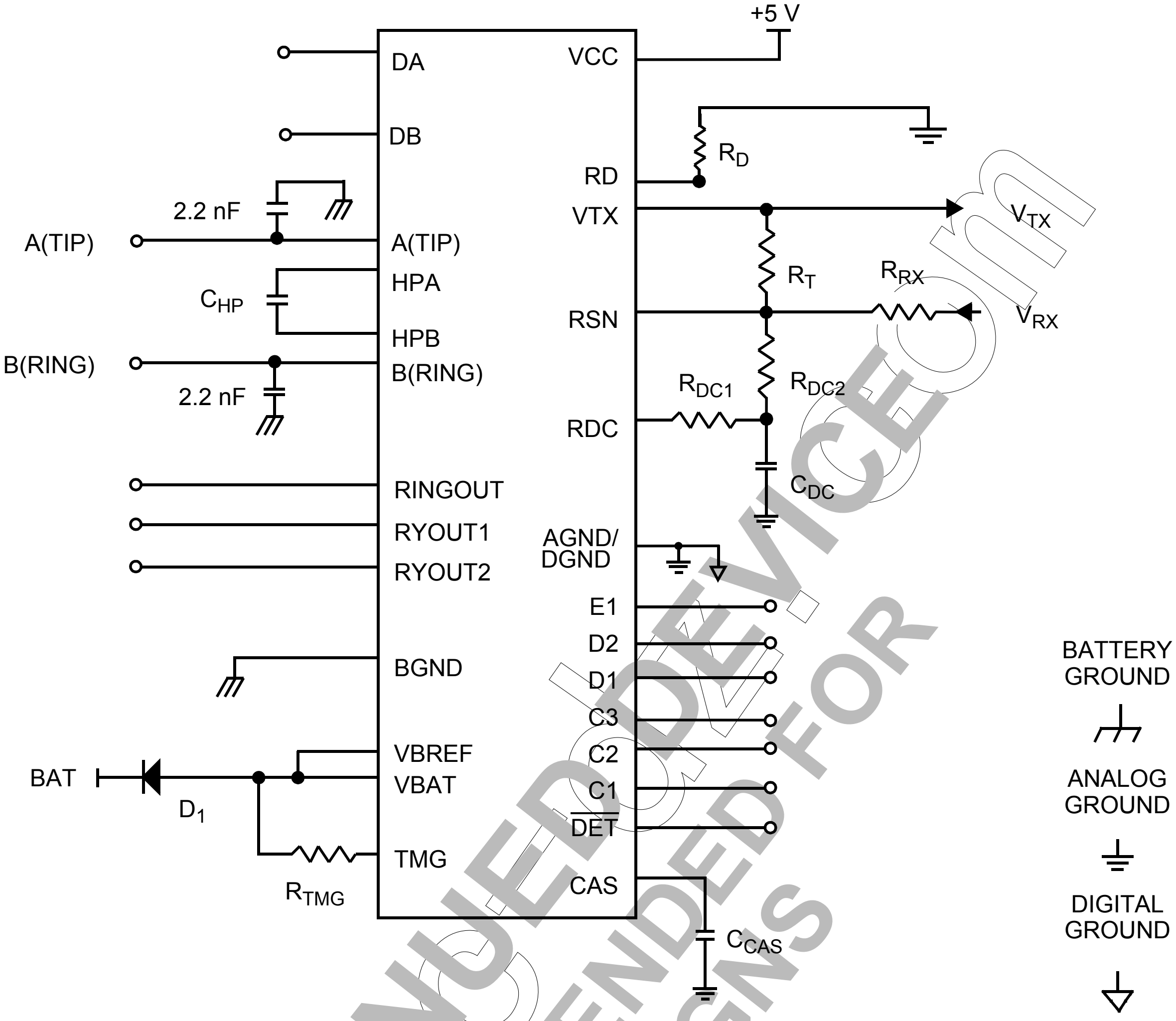
Return loss = –20 log (2 V_M / V_S)

D. Two-Wire Return Loss Test Circuit



E. RFI Test Circuit

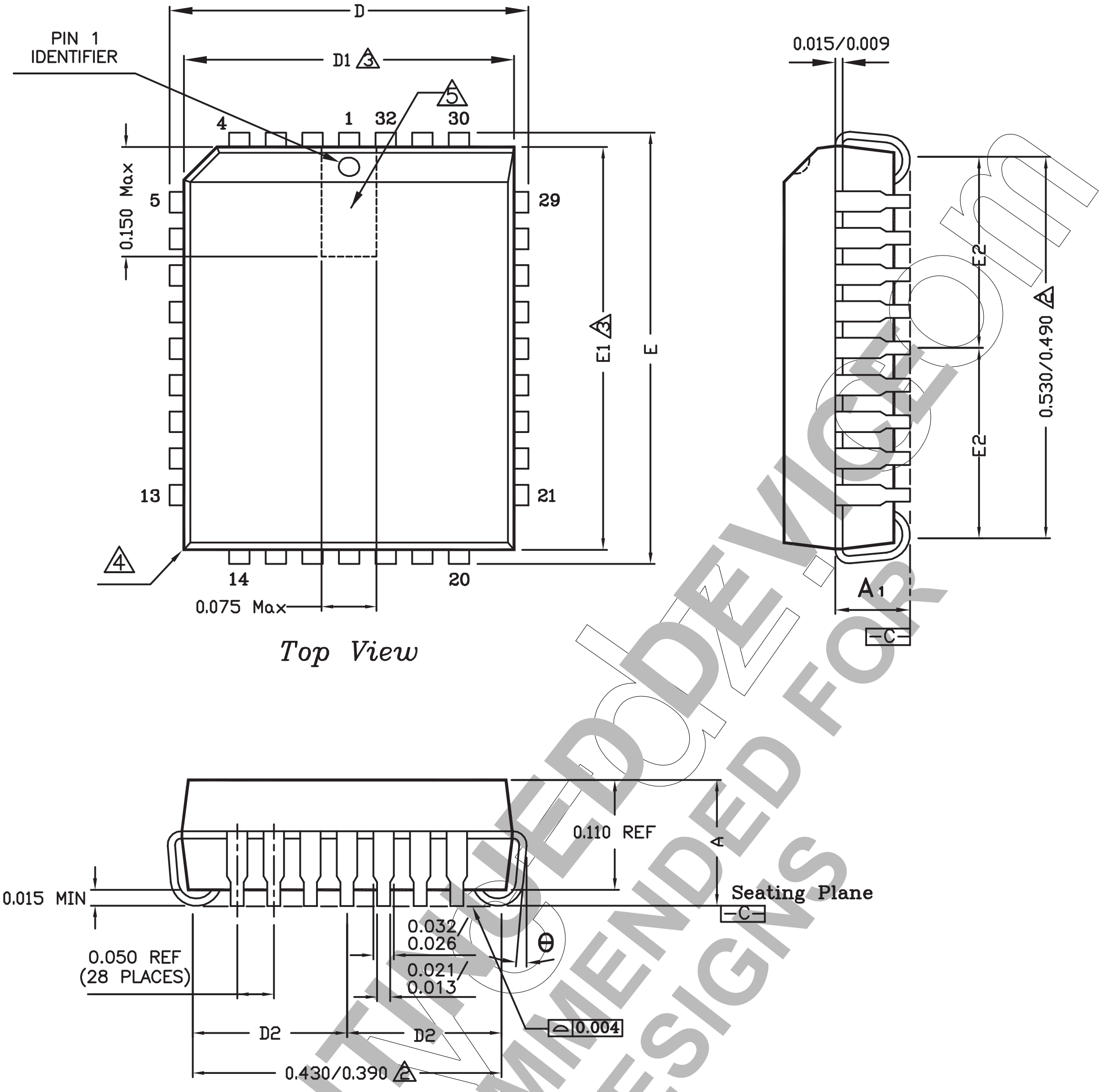
TEST CIRCUITS (continued)



F. Le7922 Test Circuit

PHYSICAL DIMENSIONS

32-Pin PLCC



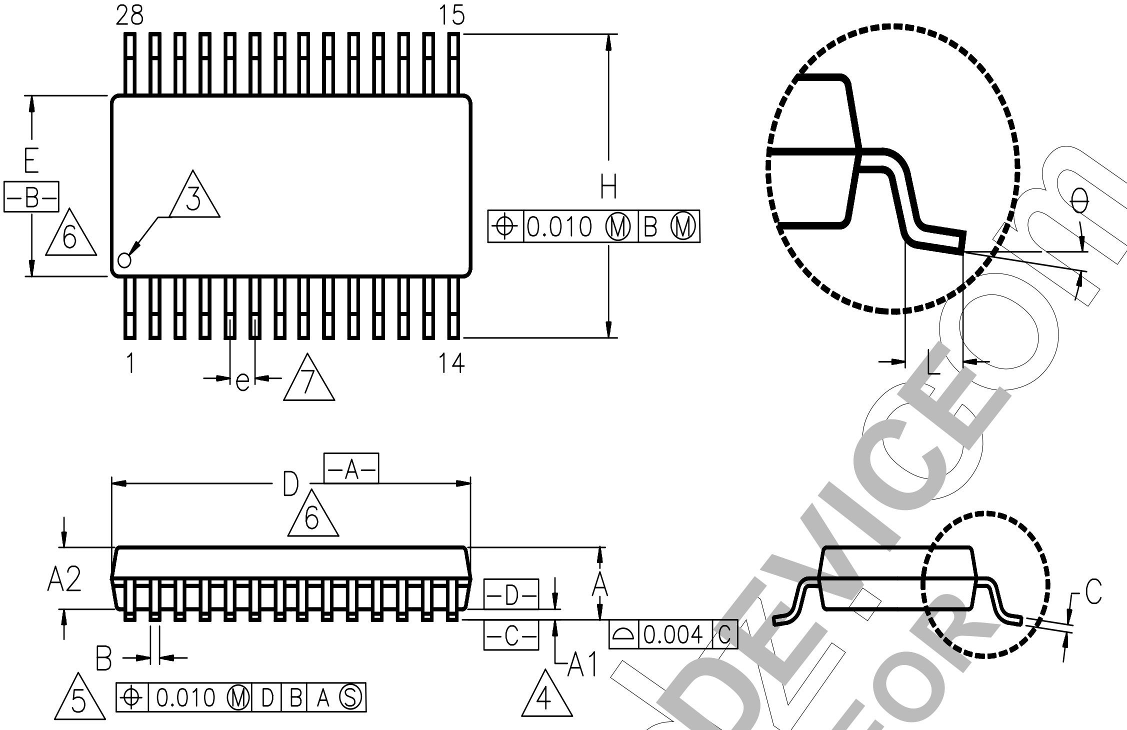
NOTE :

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14,5M–1994.
2. TO BE MEASURED AT SEATING PLANE -C- CONTACT POINT.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTURSION IS 0.010 IN PER SIDE. DIMENSIONS D, AND E, INCLUDE MOLD MISMATCH AND DETERMINED AT THE PARTING LINE; THAT IS D1 AND E1 ARE MEASURED AT THE EXTREME MATERIAL CONDITION AT THE UPPER OR LOWER PARTING LINE.
4. EXACT SHAPE OF THIS FEATURE IS OPTIONAL.
5. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
6. SUM OF DAM BAR PROTRUSIONS TO BE 0.007 MAX PER LEAD.
7. CONTROLLING DIMENSION : INCH.
8. REFERENCE DOCUMENT : JEDEC MS–016

Symbol	Dimension in inch		
	Min	Nom	Max
A	0.125	—	0.140
A1	0.075	0.090	0.095
D	0.485	0.490	0.495
D1	0.447	0.450	0.453
D2	0.205 REF		
E	0.585	0.590	0.595
E1	0.547	0.550	0.553
E2	0.255 REF		
θ	0°	—	10°

BSC is an ANSI standard for Basic Centering. Dimensions are measured in inches.

28-Pin SOIC



Dwg rev AC; 11/99

PACKAGE	SOW 028		
JEDEC	MO–059 (B) AC		
SYMBOL	MIN.	NOM.	MAX.
A	.080	.095	.100
A1	.002	.007	.014
A2	.086	.088	.090
B	.014	.016	.020
C	.006	.008	.0125
D	.697	.714	.728
E	.324	.346	.350
e	.050 BSC		
H	.453	.470	.500
L	.016	.031	.050
θ	0°	4°	8°

NOTES:

1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M – 1982.
3. I.D. MARK SHALL BE LOCATED ADJACENT TO PIN 1.
4. DIMENSION A1 IS MEASURED FROM THE BASE PLANE OF CONTACT THAT IS MADE WHEN THE PACKAGE IS ALLOWED TO REST FREELY ON A FLAT HORIZONTAL SURFACE. (SEATING PLANE).
5. DIMENSION "B" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT EXCEED 0.006 INCHES PER SIDE.
6. DIMENSIONS "D" AND "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DO INCLUDE MOLD MISMATCH AS MEASURED AT THE MOLD PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
7. DIMENSION "e" IS MEASURED AT THE CENTERLINE OF THE LEADS.
8. LEAD COPLANARITY SHALL BE WITHIN 0.004 INCHES AS MEASURED FROM THE SEATING PLANE.

REVISION SUMMARY

Revision A to B

- Updated OPN (Ordering Part Number) throughout document.
- Absolute Maximum Ratings: Notes updated to standard.
- Operating Ranges: Temperature statement updated to standard.
- Updated "Sales Office Listing."
- Updated physical dimension drawings.

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