8-BIT MCU BASED SPEECH/MELODY CONTROLLER WITH LCD DRIVER

General Description

MS36300 series MCU is an integrated system with an 8-bit microprocessor, LCD driver, 32.768 KHz crystal for real time clock, PLL, speech/melody peripherals, I/O ports, low voltage reset function(LVR), 4-channel ADC, voltage comparator, UART, Serial memory access, watch dog timer and random number generator. Up to 160 seconds of speech can be play or up to 503K bytes program ROM(without speech or melody) can be accessed via the controller inside MS36300. Besides, MS36300 offers users lots of flexibility in designing speech/melody products such as intelligent educational toys with LCD and high-quality LCD games.

Microcontroller Core Features

- Operating voltage range:
  - 2.4V to 5.0V@4MHz
  - 3.0V to 5.0V@6MHz
  - 3.6V to 5.0V@8 MHz
- Dual clock oscillation circuits:
  - Up to 8MHz Crystal/Resonator/PLL or 4MHz RC oscillation
  - 32.768 KHz Crystal for real time
- 8-bit MPU core
- Support 3 switchable banks (16K bytes per bank) for program.
- 503K bytes internal mask ROM: A single ROM contains all program codes, speech and melody.
- 4864 bytes SRAM for MS36316; (8960 bytes SRAM for MS36308)
  - 160 bytes general purpose RAM
  - 256 bytes stack
  - 480 bytes LCD RAM (144 bytes can be general purpose RAM when SEG96-73 are set as I/O mode)
  - 4096 bytes general purpose RAM for MS36316; (8192 bytes general purpose RAM for MS36308)
- Power saving modes to reduce power consumption
  - Halt mode and stop mode
  - Software programmable CPU clock and peripheral clock
- Twenty interrupt sources with four interrupt levels

Peripheral Features:

- Provide both PWM & DAC audio output with volume programmable
  - Four sound channels for DAC: 2 for speech and 2 for melody
  - Six sound channels for PWM: 4 for speech and 2 for melody
- Ten 8-bit timers: four speech timers, one melody timer, two general purpose timers can be cascaded as a 16-bit counter, one clock timer, one RTC timer, and one watch dog timer(or random number generator)
- I/O ports
  - 4 input pads PI (with wake up and interrupt function)
  - 8 I/O pads PA (with wake up function)
    - ☆ PA[7,6] support UART function
    - ☆ PA[5,4] support external serial memory function
    - ☆ PA[3..0] support auto-key-scan function
  - SEG96-73 can be programmed as I/O pads

- Support auto-key-scan function (comprise COM[32..1] and PA[3,0])
- PI[1,0] can be programmed as the input of voltage comparator.
- PI[3..0] can be programmed as the input of ADC.
- Four channels speech and dual channels melody can be simultaneously played out
- Speech length: 160 seconds (based on 6K sampling rate, 4-bit ADPCM)
- Provide software algorithms for different sound quality requirements
  - 4-bit a-law ADPCM, and 8-bit PCM
- LCD driver
  - LCD power: 1.5*Vdd or 2*Vdd or 3*Vdd voltage booster
  - LCD type: Type B
  - Bias mode: 1/6 ~ 1/9 bias
  - Duty mode: Software programmable 1/32, 1/40, 1/48 duty
  - Display mode: 32Com*96Seg, 40Com*80Seg, 48Com*72Seg mode, and 48Com*64Seg folding mode
  - Frame frequency: software programmable
  - Built-in LCD current regulator
  - Adjustable LCD brightness by external resister
- Serial memory
  - Support two general types of serial memory

Special Microcontroller Features:

- Provide PWM audio output for hand held game application
  - Software programmable 16 levels of volume control and output buffer control
- Two indepentent 8-bit audio DAC could be used as sterio output
- Software programmable CPU clock
- Built-in voltage comparator (16 level) can be used as general voltage comparator or low battery detector.
- Built-in 4-channel, 8-bit AD converter.
- Built-in watchdog timer, which can also be configured as random number generator alternatively
- Build-in LVR(low voltage reset)

Application Field:

- High flexibility educational toy
- High resolution LCD game
- Hand held electric appliance controller

1.0 Pad Description

TABLE 1-1: Pad Description – MS36316

Designation	I/O	Description
PVDD/PGND	Power	Positive/Negative power supply for PWM output
AVDD/AGND	Power	Positive/Negative power supply for analog circuit
AVDD/AGND	Power	Positive/Negative power supply for analog circuit
VDD/GND	Power	Positive/Negative power supply
OSCI	I	Oscillation input pad Oscillation source can be Crystal/Resonator or RC **Note.** If PLL is selected as the system clock source, then this pad must be connectted to VDD or GND to reduce power consumption
OSCO	O	Oscillation output pad or PLL input pad. **Note.** If PLL is selected as the system clock source, this pad must connect a 0.1uF ceramic capacitor to ground.
PI3 – 0	I	General purpose input pads with pull-high resistors. With interrupt function and Built-in Schmitt trigger circuit for all PI3-0 pads. PI3 ~ 0 can also be programmed as 4 channel, 8 bit ADC. PI1 and PI0 can also be programmed as voltage comparator input pad.
PA7 - 0	I/O	General purpose input/output pads with software programmable pull-high resistors and input/output mode. With wake up function when configured as input pads. PA7 can also be as RXD pad when UART function was enabled PA6 can also be as TXD pad when UART function was enabled PA5 can also be as SMA(serial data) pad when SMA function was enabled PA4 can also be as SCK(serial clock) pad when SMA function was enabled PA3 can also be used as SMA address clock pad PA3 ~ PA0 can also be programmed as input pads of the auto-key-scan
AU1/AU2	O	Audio signal output pads for both DAC and PWM
RESETB	I	Reset signal input pad. A logic zero on this pad forces the MCU entering a known start-up state. A Schmitt trigger circuit and pull-high resistor (100K ohm) are built-in
*TEST	I	For evaluation purpose(floating for normal operation)
XTLI	I	Input pad for 32.768KHz oscillator
XTLO	O	Output pad for 32.768KHz oscillator
CAP11, CAP12 CAP21, CAP22 CAP31, CAP32	O	Capacitors connection pads for internal voltage booster VBO = n * VDD voltage booster, n = 1.5, 2, 3 CAP32~CAP11 can also be programmed as general output ports CAP32 can also be programmed as frequency/duty programmable clock output pad for external voltage booster
VBO	O	Voltage booster output pad (VBO is the highest voltage for LCD signal)
COM32-1	O	COMmon signal output pads of LCD driver
SEG96-1	O	SEGment signal pads of LCD driver. SEG[16..1] can also be programmed as COM[48..33] SEG[96..73] can also be programmed as general I/O ports (PD/PC/PB)
VLCD1~6	I	LCD Bias voltage output pads
REXT	I	By connecting a resistor to ground to adjust bias current of LCD current regulator
VREF	I	Reference voltage input for ADC; A 0.1uF capacitor should be connected despite internal/external reference voltage.

*TEST pad: for test purpose only

Totally 171 pads for MS36316 chip

TABLE 1-2: Pad Description – MS36300 EV

Designation	I/O	Description
PVDD/PGND	Power	Positive/Negative power supply for PWM output
AVDD/AGND	Power	Positive/Negative power supply for analog circuit
AVDD/AGND	Power	Positive/Negative power supply for analog circuit
AVDD/AGND	Power	Positive/Negative power supply for analog circuit
VDD/GND	Power	Positive/Negative power supply
VDD/GND	Power	Positive/Negative power supply
OSCI	I	Oscillation input pad Oscillation source could be Crystal/Resonator or RC **Note.** If PLL is selected as the system clock source, then this pad must be connectted to VDD or GND to reduce power consumption
OSCO	O	Oscillation output pad or PLL input pad. **Note.** If PLL is selected as the system clock source, this pad must connect a 0.1uF ceramic capacitor to ground.
PI3 – 0	I	General purpose input pads with pull-high resistors (100K ohm Typ.). With interrupt function and Built-in Schmitt trigger circuit for all PI3-0 pads. PI3 ~ 0 can also be programmed as 4 channel, 8 bit ADC. PI1 and PI0 can also be programmed as voltage comparator input pad.
PA7 - 0	I/O	General purpose input/output pads with software programmable pull-high resistors and input/output mode. With wake up function when configured as input pads. PA7 can also be as RXD pad when UART function was enabled PA6 can also be as TXD pad when UART function was enabled PA5 can also be as SMA(serial data) pad when SMA function was enabled PA4 can also be as SCK(serial clock) pad when SMA function was enabled PA3 can also be used SMA address clock pad PA3 ~ PA0 can also be programmed as input pads of the auto-key-scan
AU1/AU2	O	Audio signal output pads for both DAC and PWM
RESETB	I	Reset signal input pad. A logic zero forces the MCU to a known start-up state. A Schmitt trigger circuit and pull-high resistor (100K ohm) are built-in
*TEST	I	For evaluation purpose(floating for normal operation)
XTLI	I	Input pad for 32.768KHz oscillator
XTLO	O	Output pad for 32.768KHz oscillator
CAP11, CAP12 CAP21, CAP22 CAP31, CAP32	O	* Capacitor connection pads for internal voltage booster VBO = n * VDD voltage booster, n = 1.5, 2, 3 (Refer to section of “LCD driver interface”) * CAP32 can also be programmed as clock output pad for external voltage booster
VBO	O	Voltage booster output
COM32-1	O	COMmon signal pads of LCD driver
SEG96-1	O	SEGment signal pads of LCD driver. SEG[16..1] can also be programmed as the COM[48..33] SEG[96..73] can be programmed as general I/O ports (PD/PC/PB)
VLCD1~6	I	LCD Bias voltage output pads
A18-A0	O	External ROM/RAM address bus (max. 512K bytes external ROM)
D7-D0	I/O	External ROM/RAM data bus
RDB	O	External ROM/RAM read signal
WRB	O	External ROM/RAM write signal

(…CONTINUE)

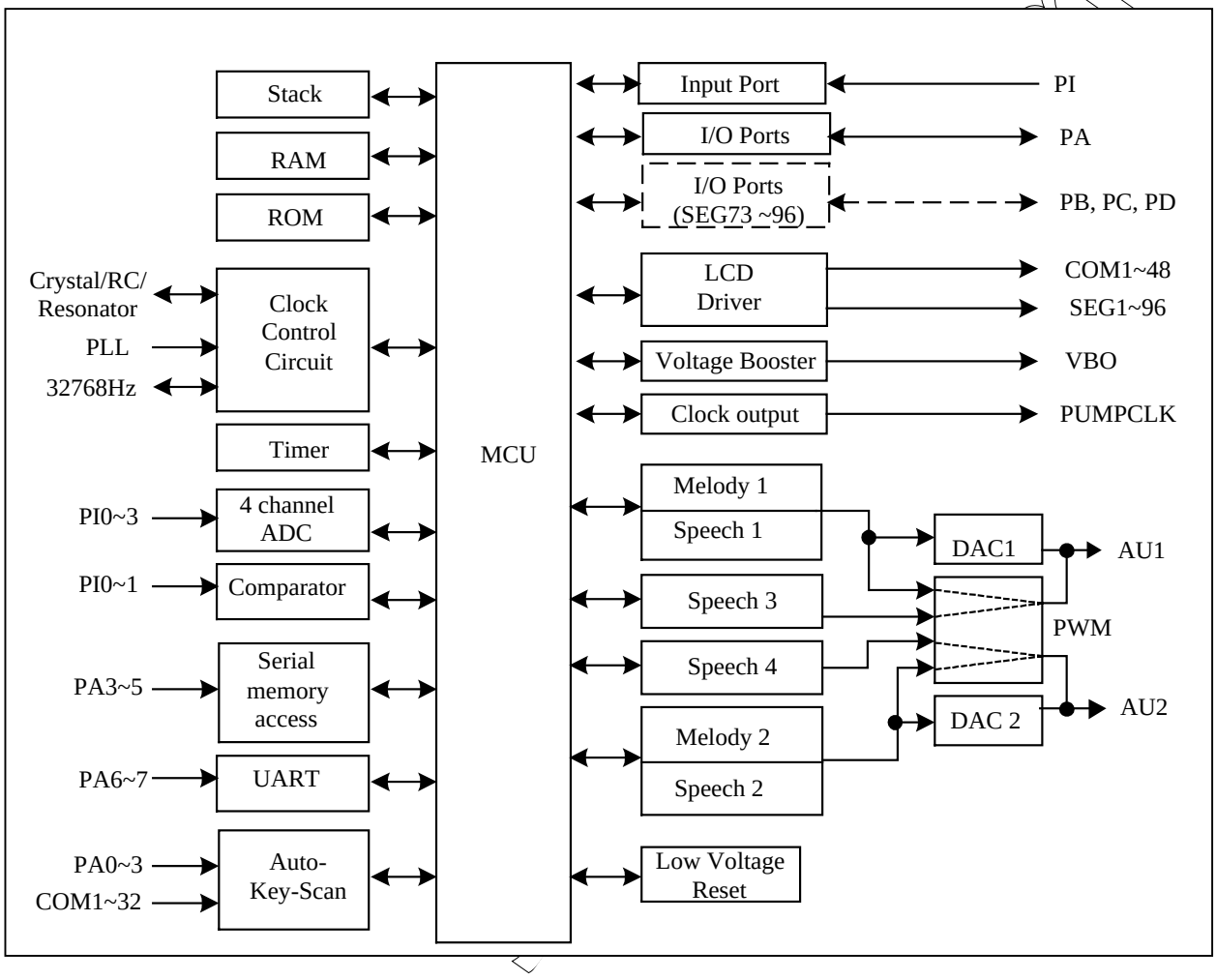
EVROMCSB	O	ROM/RAM (for EV/DVP mode) CS signal
BDM_SCLK	O	BDM Serial clock
BDM_SDI	I	BDM Serial data input
BDM_SDO	O	BDM Serial data output
BDM_EMU	O	CPU operating mode indication 1: CPU is in Background Debug Mode (CPU is halted) 0: CPU is in Normal Function Mode (CPU is running)
BDM_RSTB	I	BDM on-chip circuit reset pin
REXT	I	By connecting a resistor to ground to adjust current of LCD regulator
OSC_SEL1~0	I	Crystal/RC/PLL selection pads OSC_SEL[1,0] = [0,0] , RC mode [0,1] , Crystal/Resonator mode [1,0] , PLL mode [1,1] , don't care
VR_SEL2~0	I	LVR(Low voltage reset) voltage option pads. LVR_SEL[2,1,0] = [0,0,0], V_{LVR} = 2.1 Volt [0,0,1], V_{LVR} = 2.2 Volt [0,1,0], V_{LVR} = 2.3 Volt [0,1,1], V_{LVR} = 3.1 Volt [1,0,0], V_{LVR} = 3.2 Volt [1,0,1], V_{LVR} = 3.3 Volt Others ➔ LVR is disabled
ADC_VREF	I	Reference voltage input for ADC; A 0.1uF capacitor should be connected despite internal/external reference voltage
MODE_SEL	I	= 0, 36300 EV chip is in 36316 mode = 1, 36300 EV chip is in 36308 mode (see TABLE 3-1 for detail)

*TEST pad: for test purpose only

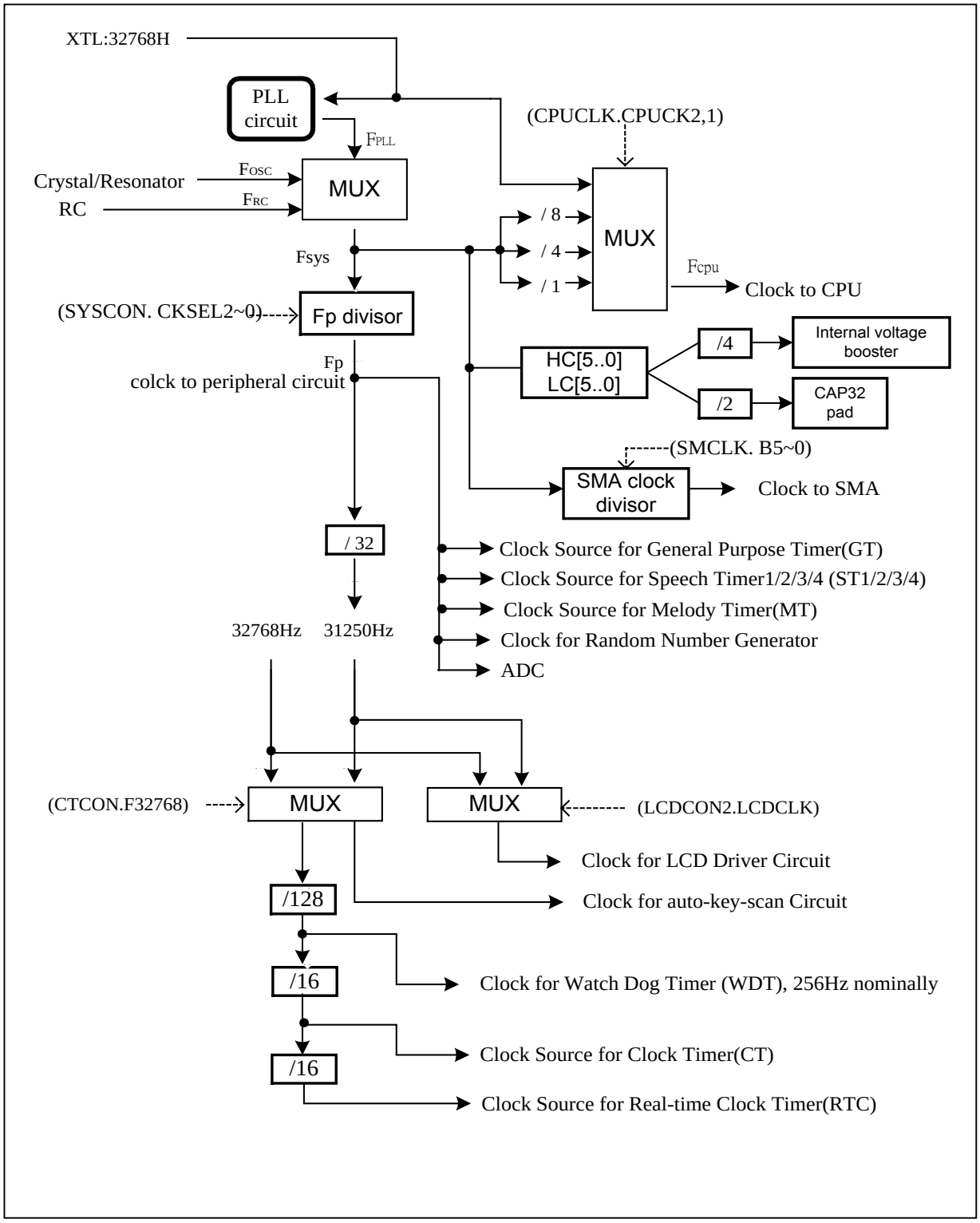
Totally 216 pads for MS36300 EV chip

2.0 Architectural overview

Block Diagram



System Clock

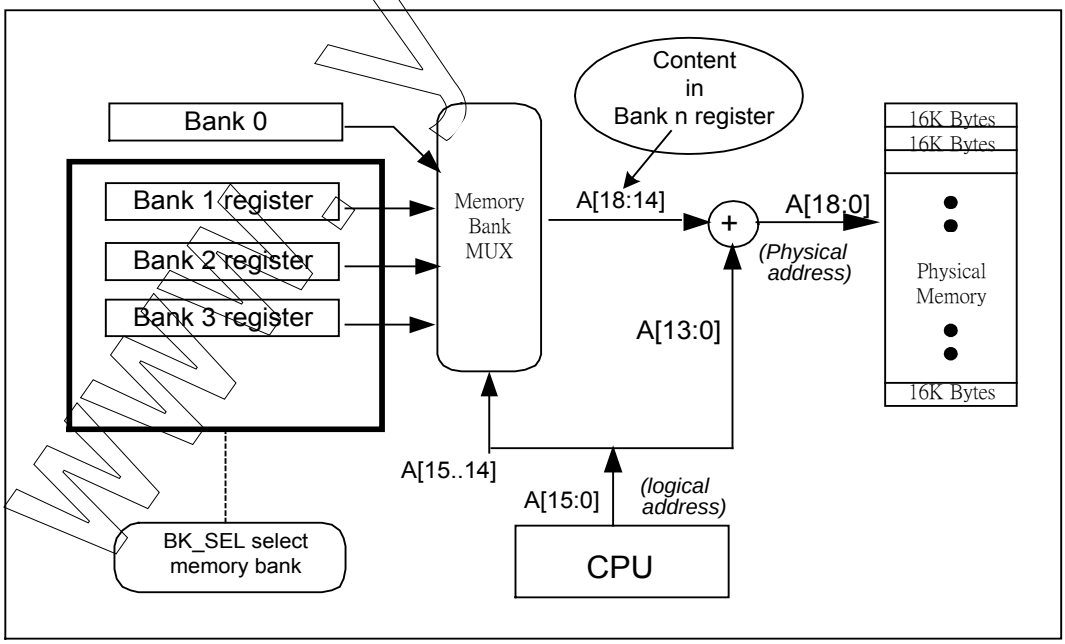


3.0 Memory Organization

Memory MAP

Programming Address		Description
0000H – 005FH		Memory mapped I/O
0060H – 00FFH		General purpose RAM, 160 bytes
0100H – 01FFH		Stacks, 256 bytes, can be used as general purpose RAM
0200H – 03DFH		LCD display registers, 480 bytes
03E0H – 03FFH		Reserved
MS36316	0400H – 13FFH	General purpose RAM, 4096 bytes for MS36316
	1400H – 3FFFH	Program ROM , 11264 bytes
MS36308	0400H – 23FFH	General purpose RAM, 8192 bytes for MS36308
	2400H – 3FFFH	Program ROM , 7168 bytes
4000H – 7FFFH		Program ROM , 16K bytes; used for swappable memory
8000H – BFFFH		Program ROM , 16K bytes; used for swappable memory
C000H – FFFFH		Program ROM , 16K bytes; used for swappable memory
MS36316	10000H – 7EFFFH	Program ROM, 444K bytes for MS36316
	7F000H – 7FFFFH	**Reserved for test program, 4K bytes**
MS36308	10000H – 3EFFFH	Program ROM, 188K bytes for MS36308
	3F000H – 3FFFFH	**Reserved for test program, 4K bytes**

Memory Expansion



LCD Display Registers

- LCD display memory space: there are four kinds of LCD display modes
  - 32COM*96SEG mode
  - 40COM*80SEG mode
  - 48COM*72SEG mode
  - 48COM*64SEG folding mode (folding up to 2 blocks of 48COM*32SEG(COM1~48/SEG17~48, COM1~48/SEG49~80)
- LCD SEG96-73 pads can be programmed as general purpose I/O port (PD7-0, PB7-0 and PC7-0).
  - SEG80-73 can be configured to be PB7-0
  - SEG88-81 can be configured to be PC7-0
  - SEG96-89 can be configured to be PD7-0

Auto-Access Circuit

The auto-access circuit can access entire memory space. It needs only one CPU instruction time to access one byte of data. When CPU access one byte, the auto-access circuit will increase the address pointer by one automatically. Generally, auto-access circuit is used to access Speech/LCD data to reduce software loading. With auto-access circuit, data-access can cross banks without changing bank.

4.0 I/O PORT

This chip has several I/O ports:

- Input-only port (PI): 4 pins (with wakeup and interrupt function)
- Input/Output port (PA): 8 pins (with wakeup function)
- Optional I/O port (PB): 8 pins from SEG1-8 pads
- Optional I/O port (PC): 8 pins from SEG9-16 pads
- Optional I/O port (PD): 8 pins from SEG17-24 pads

Input-only Port : PI Port (PI0-3)

PI[3..0] can be programmed as input pads of ADC or general I/O pads.
PI[1,0] also can be programmed as input pads of Comparator.

Bi-directional I/O pads : PA Port (PA0-7)

PA[7..0] pads are multi-function pads:
PA[7,6] can be programmed as RXD/TXD or general I/O pads
PA[5,4] can be programmed as for SMA function or general I/O pads
PA[3..0] can be programmed as for key-matrix function or general I/O pads

Optional Bi-directional I/O pads : PB Port, PC Port and PD Port

There are 16 LCD segment pins can be programmed as bi-directional I/O pads if programmer needn't so many segments for LCD panel.

- SEG80-73 can be programmed as PB7-0
- SEG88-81 can be programmed as PC7-0
- SEG96-89 can be programmed as PD7-0

5.0 Timers

There are ten timers: two general purpose timers can be cascaded as a 16-bit counter, 4 speech timers, one melody timer, one clock timer, one RTC timer, and one watch dog timer. General purpose timer is for general purpose usage, e.g., keyboard de-bounce, silence control in speech connection, elapse time counting, ..., etc. Usually, speech timers are for controlling speech sampling rate; melody timer is for controlling melody rhythm and clock timer is for real time clock.

Although speech and melody timers are very appropriate for speech sampling rate and melody rhythm control, they can be used as general-purpose timers, too. In fact, these timers do not have any relation to speech or melody generating hardware.

Clock and RTC timer are for real time counter.

General Purpose Timers

These two 8-bit up-count timers can be cascaded as a 16-bit timer. As the counting rolls over from all 1s to all 0s, the timer overflow flag GTHIF/ GTLIF will be set. In **auto-reload mode**, GTCTL will be reloaded with contents of GTCTH (as loader of GTCTL) preset by software while GTLOF is set. The reloading leaves GTCTH unchanged. When GTEN is setting to 1, the timer (in any mode) will start to count.

Speech Timer1, Timer2

ST1 and ST2 are 8-bit up-count timers with **auto-reload** function, and are designed to be speech sampling rate generators. As the count rolls over from all 1s to all 0s, the speech timer overflow flag STOF will be set. At the same time, the counter will be reloaded with contents of STLD which is preset by software. The reload leaves STLD unchanged.

Melody Timer

This is an 8-bit up-count timer and is designed for melody rhythm control or silence control in speech connection. After loading data to the counter, it will begin up counting. When it up counts to FFH, it will generate an overflow flag MTOF and automatically stop counting.

Clock Timer

This is an 8-bit up-count timer with **auto-reload** function and is designed to be a real time clock. As the counter rolls over from all 1s to all 0s, the timer overflow flag CTOF will be set. At the same time, the counter will be reloaded with contents of CTLD which is preset by software. The reload leaves CTLD unchanged. Note that when a data is written to CTLD, the value is also write to the 8-bit counter.

RTC Timer with Alarm Function

This timer performs most clock functions (second, minute, hour and day) with alarm. After setting RTCEN bit on, it will begin counting (second) up and carry to minute / hour automatically and keep counting (forever) unless be disabled. It counts from user set value to HOUR=17h (23), MINUTE=3Bh (59), SECOND= 3Bh (59) then reset all the RTC registers (in next clock) and keep counting from 000, 00:00:00.

When a programmer sets alarm active, a comparator will compare the RTC registers with the alarm registers. When contents of these registers are equal, a flag ALMOF is generated and automatically clears ALMEN bit.

Random Number Generator / Watch Dog Timer

There is a 8 bit non-sequence counter build in MS36100. This counter can be programmed to be random number generator or watch dog timer by setting the related control bits.

The 8 bit Watch Dog / Random number Timer ***is not a sequence up counter!!*** So it can be configured as a random number generator using free-run mode with higher clock source. This random number generator is similar to general 8-bit pseudo-random generator-- the data will repeat after a particular number of clocks. To get a real time clock-independent Random number, the user should include real time variable, e.g. RTC timer, key-press input.

6.0 Interrupt

There are twenty interrupt sources with four priority levels. The priority order is: Priority #1 > #2 > #3 > #4. An enabled interrupt with higher priority can interrupt a lower priority interrupt; for interrupts with the same priority can not interrupt each other.

- Priority #1: PI(high to low or low to high), Key-scan, SMA(including LENGTH, ERROR interrupt sources)
- Priority #2: Speech timer 1~4 (overflow), ADC(data input), Comparator(CMPCON.RESULT transition), RTCSEC(overflow)
- Priority #3: Melody timer(overflow), UART(including OVER, SHIFT, RX, TX interrupt sources)
- Priority #4: General purpose timerGTL,GTH(overflow), Clock timer (overflow), Alarm(time up), RTCHOUR(overflow), RTCMIN(overflow), RTCDAY(overflow)

7.0 Speech and Melody

There are 2 programmable audio output: one is DAC output and another is PWM output. DAC output produces high sound quality, but consumes more power. In the other hand, PWM output consumes less power, but produces lower sound quality. For PWM output, there are 4 speech channels and dual tone melody which can be simultaneously played out. For DAC output, there are 2 speech channels and dual tone melody which can be simultaneously played out. AUDIO1 is the combined output of speech 1 and melody 1; AUDIO2 is the combined output of speech 2 and melody 2.

MS36300 PWM output provide also software programmable 16 modes output ratio control (PMOD3-0) and output buffer size control (PBUF3-0) feature for imporving output sound quality.

PWM Output Volume Control

This chip provides advanced PWM output control mode :

- Software programmable PWM speech/melody volume-ratio control(PMOD3-0)
- Software programmable PWM output buffer control(PVOL3-0)

This advanced PWM output was in current mode. Higher input impedance of speaker will make the PWM output saturation.

PWM VOLUME OPTION

PMOD3~0 Value	Output Volume
1111	silence
1110	silence
1101	attenuate the volume to 1/28
1011	attenuate the volume to 1/14
1001	attenuate the volume to 3/28
0111	attenuate the volume to 1/7
0101	attenuate the volume to 5/28
0011	attenuate the volume to 3/14
0001	attenuate the volume to 1/4
1100	attenuate the volume to 1/7
1010	attenuate the volume to 2/7
1000	attenuate the volume to 3/7
0110	attenuate the volume to 4/7
0100	attenuate the volume to 5/7
0010	attenuate the volume to 6/7
0000	maximize the volume(base unit)

PWM SPEECH/MELODY VOLUME RATIO OPTION

Audio Channel Volume ratio (PMOD3~0)	Melody Channel 1	Melody Channel 2	Speech Channel 1	Speech Channel 2	Speech Channel 3	Speech Channel 4
0000b	1	1	4	4	4	N/A
0001b	1	1	4	4	2	2
0010b	6	2	N/A	N/A	N/A	N/A
0011b	4	4	N/A	N/A	N/A	N/A
0100b	N/A	N/A	6	6	4	N/A
0101b	2	2	8	N/A	N/A	N/A
0110b	2	2	4	4	N/A	N/A
0111b	2	1	10	N/A	N/A	N/A
1000b	2	1	6	4	N/A	N/A
1001b	1	1	12	N/A	N/A	N/A
1010b	N/A	N/A	4	4	4	4
1011b	1	1	6	6	N/A	N/A
1100b	N/A	N/A	8	8	N/A	N/A
1101b	N/A	N/A	14	2	N/A	N/A
1110b	N/A	N/A	12	2	2	N/A
1111b	N/A	N/A	16	N/A	N/A	N/A

Dual Channel Speech

There are two DACs that can be used to generate current-source speech signals. DAC1 is sent to AU1 to combine melody 1; DAC2 is sent to AU2 to combine melody 2. Other related details are listed as below.

- Simply two 8-bit DACs. All the decompression tasks are done by software.
- Two layers of latch for DAC. The first latch is directly written by CPU and the second latch is directly connected to DAC. Timing for data flow from first latch to second latch can be selected to be speech timer overflow duration or completely transparent.
- Sampling rate can be programmed through the related speech timer registers.
- Silence length control in speech connection can be done by using melody timer or general purpose timer.
- High quality melody can be generated through proper speech sampling and playing.
- To prevent noise interference, audio output should be isolated from high-speed digital circuit in application board layout.

Dual Tone Melody

Quality of MS36100's dual tone melody is comparable to M-SQUARE's high-end dual tone melody chip. Some related details are listed as below.

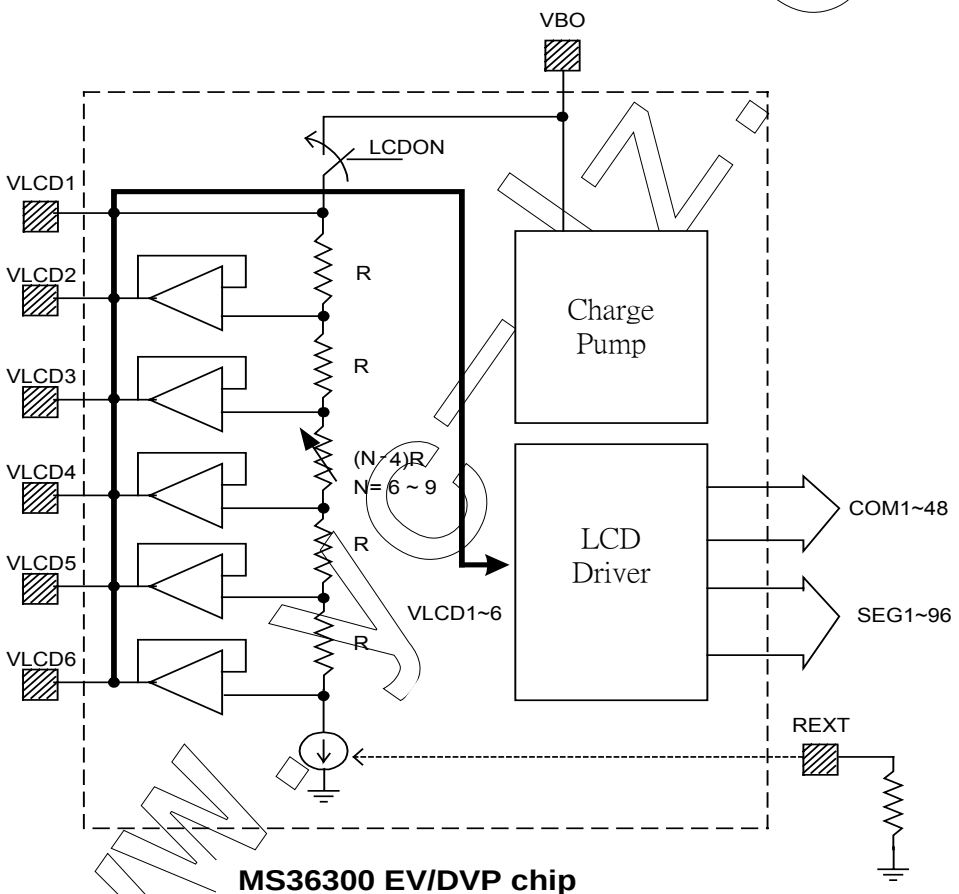
- Each channel can be individually played out by programming ML1EN and ML2EN.
- The melody data to be output to which channel is programmed by software. Melody codes are stored in ROM memory and are viewed as same as program code.
- Rhythm of each song is programmed by software (usually by programming melody timer. MS36100 library also provides subroutine to update melody rhythm).

8.0 LCD Driver Interface

The characteristics of LCD driver circuit are:

- Common driver pads: 32
- Segment driver pads: 96, (SEG[96..73] can be programmed as I/O pads, SEG[16..1] can be programmed as COM[48-33])
- Duty mode: 1/32, 1/40, 1/48 duty, software programble
- Bias mode: 1/6 ~ 1/9 bias
- Frame scheme: Type B.
- Frame Frequency (FF): programmed by bits 3~0 of LCDCON1, see Table 8-2 *"LCD frame frequency".*
- built-in 1.5*Vdd, 2*Vdd, 3*Vdd voltage booster and constant current regulator

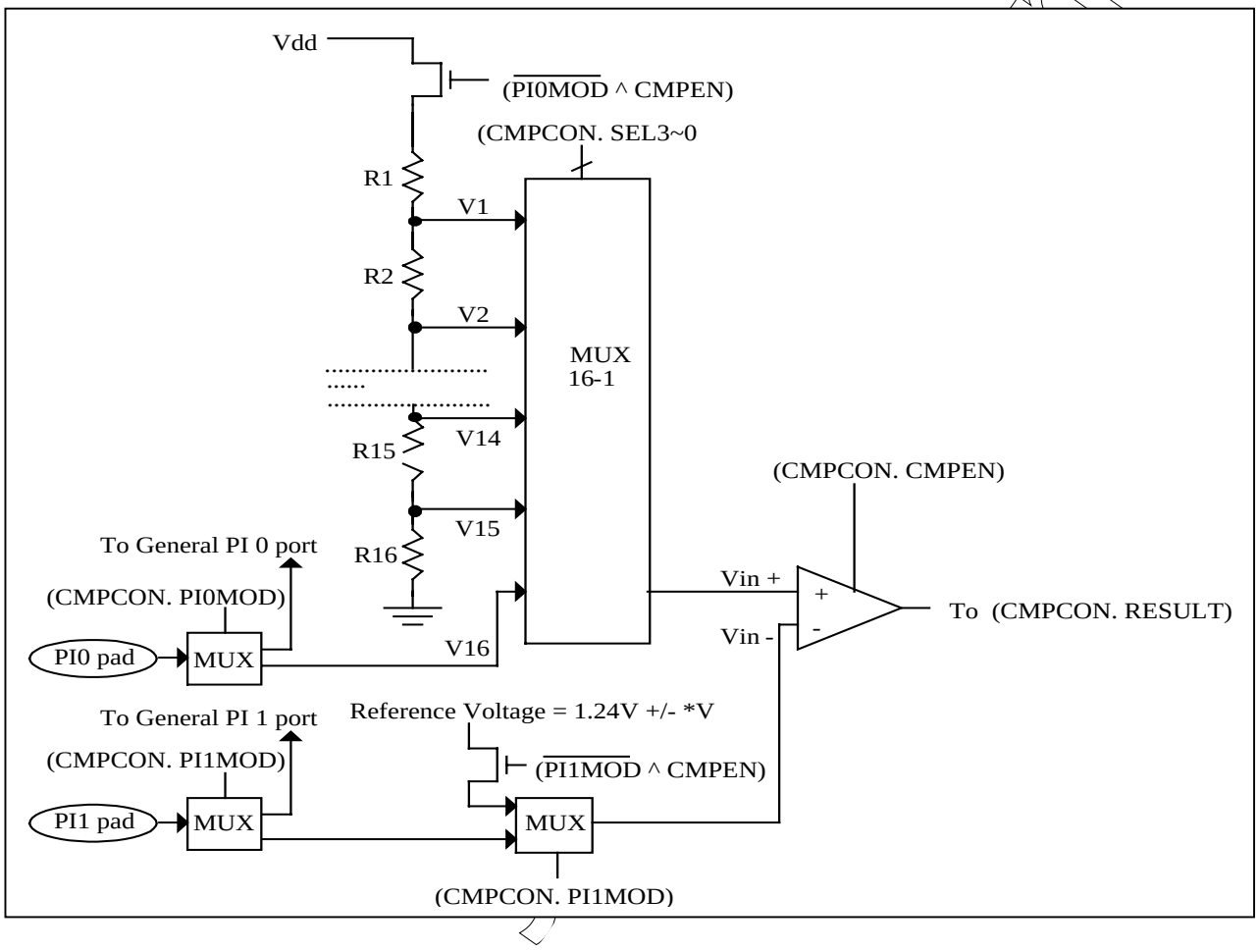
FIGURE 8-1: POWER & BIAS CIRCUIT FOR LCD DRIVER



9.0 Comparator / Low Battery Detector

This comparator circuit can be programmed as general 2-bit comparator or Low battery detector.

FIGURE 9-1: COMPARATOR / LOW BATTERY DETECTOR DIAGRAM



10.0 Analog to Digital Converter (ADC)

MS36300 performs a 4-channel, 8-bit A/D conversion via successive approximation. This ADC is connected to PI[3..0] which allow each pad to be an analog input for this ADC. There is a sample-and-hold amplifier in the ADC to ensure the input voltage is held at a constant level during conversion process.

This ADC can operate in two modes: single-run mode & auto-run mode.
In single-run mode, a complete A/D conversion must be initiated manually.
In auto-run mode, the ADC constantly samples & generates the result to ADC data registers (ADCDATA) until ADC was disabled.

The self-calibrated circuit is also built in this chip to correct the shift error. The calibration procedure is started by setting CALEN and then starts an A/D conversion. After completing conversion, the offset (calibrated) value is moved to ADCDATA.

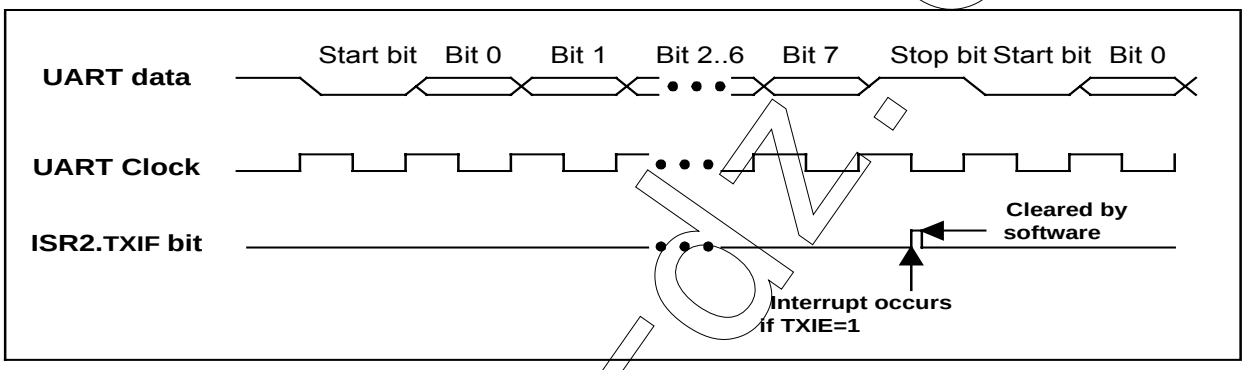
The conversion rate (2K~16K Hz) is programmable by pre-scale of ADC clock (ADCPR0,1). The following diagram shows the ADC clock source.

11.0 UART

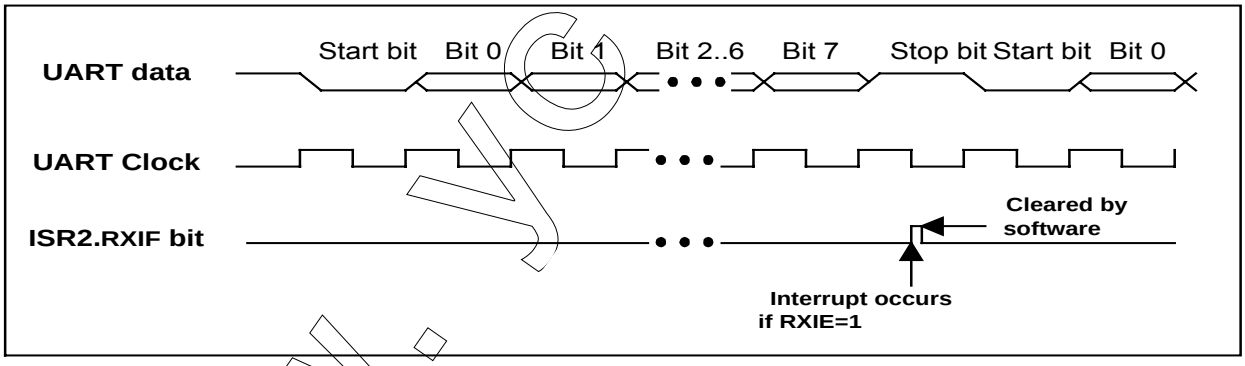
This is a simplified Universal Asynchronous Receiver/Transmitter with programmable Baud rate.

- Data structure of frames:
  - 1 start bit
  - 8 data bits
  - 1 stop bit
- With over-run and shift error interrupt functions

DATA TRANSMISSION



DATA RECEIVING



12.0 Auto-Key-Scan

This function is by associating COM32~1 with PA3~0 to scan key-press. COM32~1 are simultaneously the LCD COMmon signal output pads. This auto-key-scan circuit uses PA ports to detect COM signal. If the COM signal was detected by PA port, then, the corresponding button should have been pressed. The auto-key-scan mechanism will automatically scan the key-matrix. After key de-bounced, the key code will be written into KEYCODE register and an interrupt will be triggered (if IER2.SCANIE is set).

13.0 Serial Memory Access (SMA)

The serial memory access circuit can read/write continuous data from/to external serial memory via SMA buffer. By cooperating with auto-access function, the user can read data continuously from internal memory and store it to external serial-memory, or read data from external serial-memory and store it to internal memory.

This SMA circuit supports two types of general serial memory protocols (Please contact with MST for details)

14.0 Electrical Characteristics

(T_A=25°C)

14.1 Absolute Maximum Rating

Parameters	Symbol	Min.	Max.	Unit
Operating voltage	VDD	2.4	5.5	V
	VLCD	2.4	5.5	V
Input voltage	VIL	GND-0.3	0.3Vdd	V
	VIH	0.7Vdd	Vdd	
Operating temperature	To	-10	60	°C
Storage temperature	Ts	-50	125	°C
Output Driving current	IOH	--	3.5	mA (Vdd=4.5V, VOH=3.8V)
Output Sink current	IOL	--	-8	mA (Vdd=4.5V, VOL=0.8V)

14.2 DC Electrical Characteristics

Parameters	Symbol	Test Condition			Min.	Typ.	Max.	Unit
Input Levels								
Input high voltage	Vih	PA, PI, RESETB			0.7* VDD	--	VDD+ 0.3	V
Input low voltage	Vil	PA, PI, RESETB			GND- 0.3	--	0.3* VDD	V
Pull-high resistance (PI, PA,….)	Ripu	PA, PI	100K	VDD=4.0V	--	111	--	KΩ
				VDD=3.0V	--	165	--	
			300K	VDD=4.0V	--	223	--	
				VDD=3.0V	--	335	--	
Output Levels								
Output high voltage	Voh	PA			0.8* VDD	--	--	V
Output low voltage	Vol	PA			--	--	0.2* VDD	V

14.3 AC Electrical Characteristics

Parameters	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Clock rate (Fsys)	Fosc	Using Crystal, VDD=4.5V	--	--	8	MHz
	FRC	Using RC , VDD=4.5V	--	--	4	
	FPLL	Using PLL, VDD=4.5V	--	--	8	
RC frequency deviation		RC=4MHz, VDD=2.4~5.0	--	5	10	%
Min. working VDD 1.Power-on-Reset success 2.Speech(1KHz, 50% duty, full-scale square wave) playing with max. Volume	VDDmin	4MHz	--	2.4	--	Volt
		6MHz	--	2.8	--	
		8MHz	--	3.4	--	

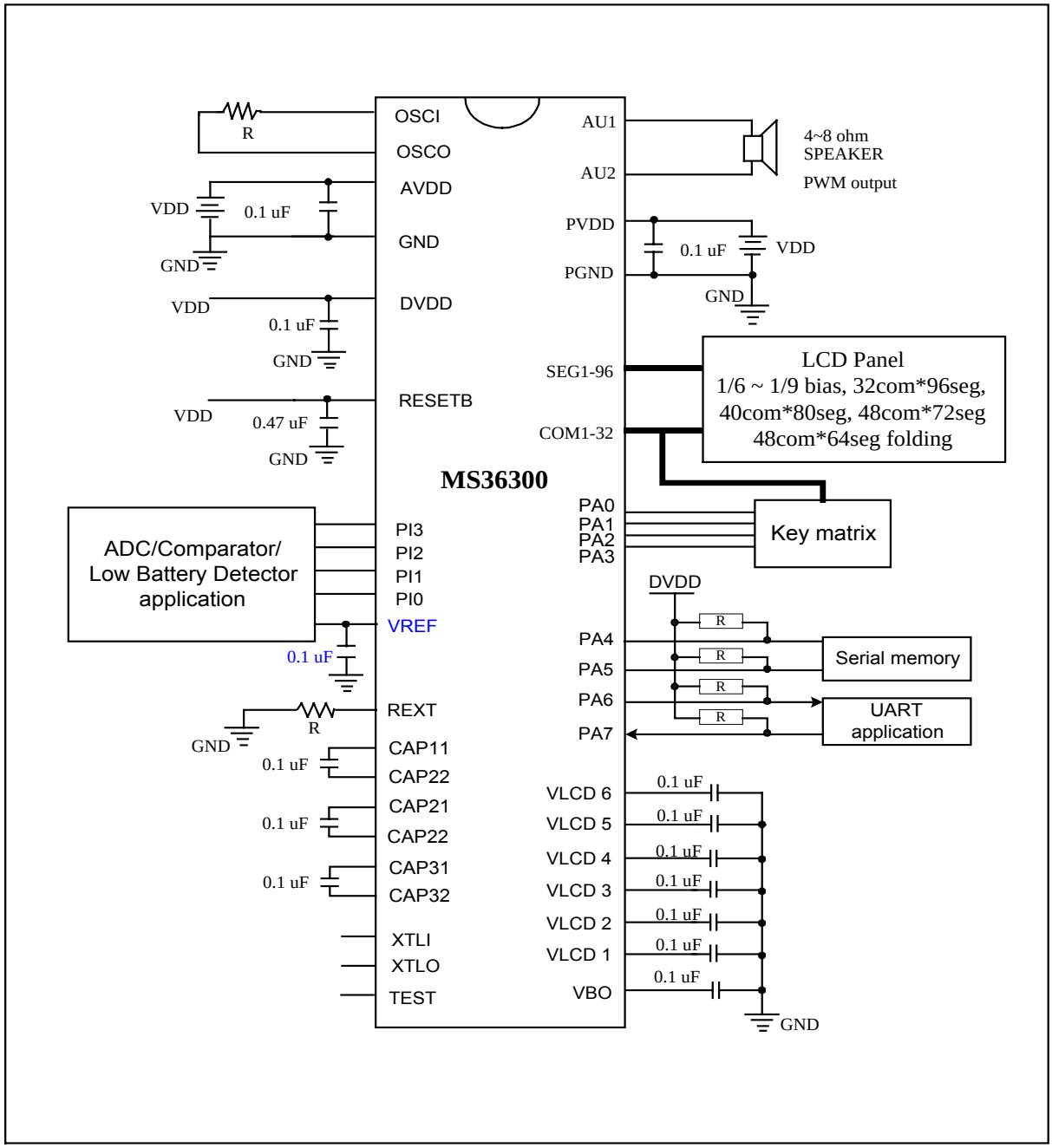
Power Consumption						
Stop current	Istp	32768 & LCD off @Vdd=4.5V	--	--	**1**	uA
Standby current with LCD off (Lowest CPU speed)	Istd1	32768 on, Vdd=4.5V, OSC off, LCD/OP off,	--	15	--	uA
Standby current with LCD on (Lowest CPU speed)	Istd2	32768 on, Vdd=4.5V, OSC off, LCD/OP on, REXT= 100KΩ, VBO=2VDD LCDCON3 = 33H	--	400	--	uA
Operating Current (Fastest CPU speed)	Idd	32768 on, Vdd=4.5V OSC=4MHz, LCD on, REXT = 100KΩ, VBO=2VDD LCDCON3=11H, OP off	--	7.7	--	mA
		OP on	--	8.0	--	
LCD						
VBO range	V_{BO}	--	--	7	--	V
Audio						
PWM Output Current (I_PVDD) (PWMVOL=0FH) **(*1)**	Ipwm	Output 1K Hz square wave @Vdd=3V, load=8ohm	--	120	--	mA
		Output 1K Hz square wave @Vdd=4.5V, load=8ohm	--	200	--	mA
DAC Operating Current (I_PVDD) (DACVOL1=0FH) **(*1)**	Idac	Output 1K Hz sine wave @Vdd=3V, load=1k ohm	--	2.7	--	mA
		Output 1K Hz sine wave @Vdd=4.5V, load=1k ohm	--	5.0	--	mA
Comparator						
ADCCON.RESULT transition time **(*2)**	Tadc1_0	VDD=2.4~5.0V	--	--	10	ms
	Tadc0_1	VDD=2.4~5.0V	--	--	10	ms
ADC						
Full-scale Input voltage range	V_{ADC}	--	0	--	V_{REF}	Volt
External V_{REF} input voltage range	--	VDD=2.4~5.0V	2	--	VDD	Volt
Internal V_{REF} voltage output range	--	VDD=2.4~5.0V	2.1	--	2.3	Volt
DNL	--	VDD=4.0V	--	+/-0.3	--	LSB
INL	--	VDD=4.0V	--	+/- 0.5	+/- 1	LSB
Conversion rate	--	VDD=2.4~5.0V	2	--	16	KHz

*1. When comparison is based on chip current, PWM consume more current than DAC. But when based on current of total circuit(include 8 ohm speaker), generally DAC consume more current than PWM.

*2. Tadc1_0: time interval from Vin+/Vin- changing status to VADCCON.RESULT transferring from 1 to 0
Tadc0_1: time interval from Vin+/Vin- changing status to VADCCON.RESULT transferring from 0 to 1

15.0 Application Circuits

15.1 **Application 1** (RC, VBO = 3*VDD, Serial memory of type 1)



15.2 **Application 2** (PLL, VBO = 2*VDD, Serial memory of type 2)